



National University
of computer and emerging sciences

Subject:

- Digital Logic Design (DLD)

Instructor Name:

- Shakir-Ullah Shah

Project Name:

- Tasbih Counter

Group Members:

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Simulator Name:

❖ Proteus

Simulator Download Link:

❖ Download Link: [Download Proteus](#)

Project Download Link:

- Download Link: [GOOGLE DRIVE LINK](#)
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Project Explanation:

In the project we made the tasbeh counter. In this we have used two Decade Synchronous Counter both the counter give output up-to nine. There are eight flip-flops in the Tasbeh Counter. The first Flip-Flop will go up-to the nine when the first flip-flop reaches up to nine the first flip-flop will recycle and the second flip-flop will run one time. Same as when the first flip-flop reaches to nine then the second flip-flop run one time when the first flip-flop generate the binary value of nine. The Tasbeh counter will run up to ninety-nine and at ninety-nine it will recycle and both the segment will be zero and the Tasbeh counter will start again.

TIDS AND BITS OF PROJECT:

➤ Analysis:

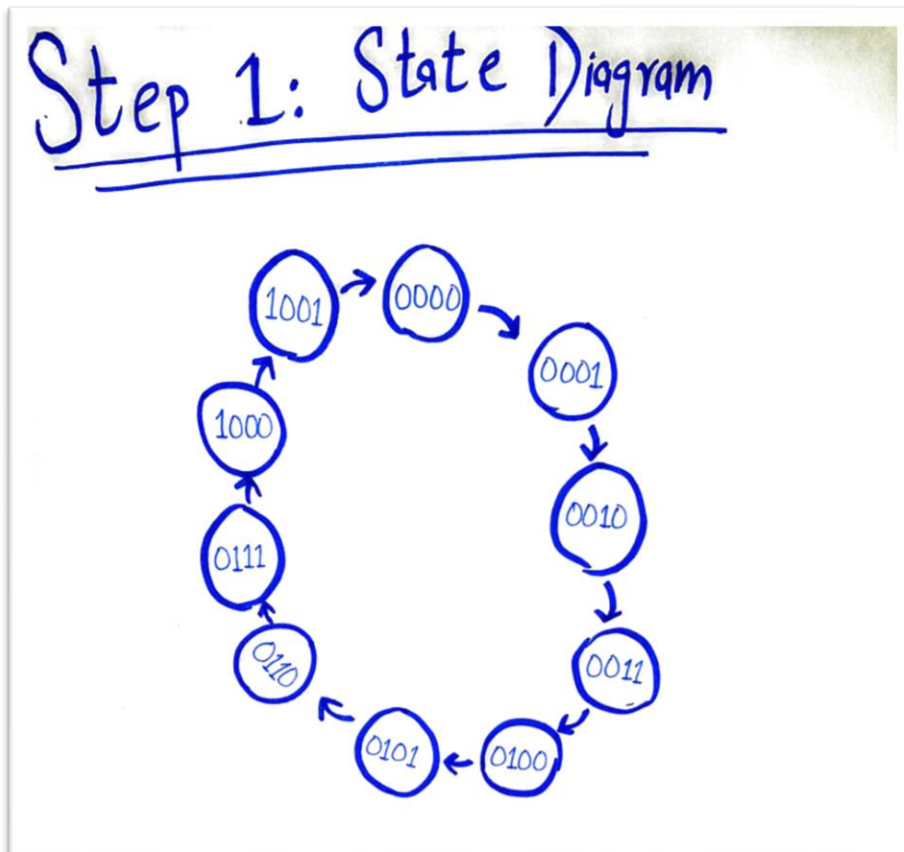
In the Tasbeh Counter we have used two synchronous Decade Counters. We have used 4 input And gate that will give high input if all input are high. When Q1 and Q2 low and Q3 and Q0 are high the second flip flop will produce output.

➤ Truth Table:

Button	Q0	Q1	Q2	Q3
0	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1
1	0	1	0	0
1	0	1	0	1
1	0	1	1	0
1	0	1	1	1
1	1	0	0	0
1	1	0	0	1
1	0	0	0	0

➤ Boolean Expression:

• Step 1:



STEP 2: NEXT STATE TABLE

Step 2: Next State Table

Present State				Next state			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

STEP 3: TRANSITION TABLE

Step 3 : Transition Table

Output Transitions		Flip-Flop Inputs	
Q_N	Q_{N+1}	J	K
0	→ 0	0	X
0	→ 1	1	X
1	→ 0	X	1
1	→ 1	X	0

Q_N : Present State
 Q_{N+1} : Next state
X : "don't Care"

STEP 4: KARNAUGH MAP

Step #4:

Karnaugh Maps

* For J_0 & K_0

$Q_3 Q_2$	$Q_1 Q_0$			
	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	X	X	X	X
10	1	X	X	X

$$J_0 = 1$$

$Q_3 Q_2$	$Q_1 Q_0$			
	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	X	X

$$K_0 = 1$$

For J_1 & K_1

$Q_3 Q_2$	$Q_1 Q_0$			
	00	01	11	10
00		1	X	X
01		1	X	X
11	X	X	X	X
10			X	X

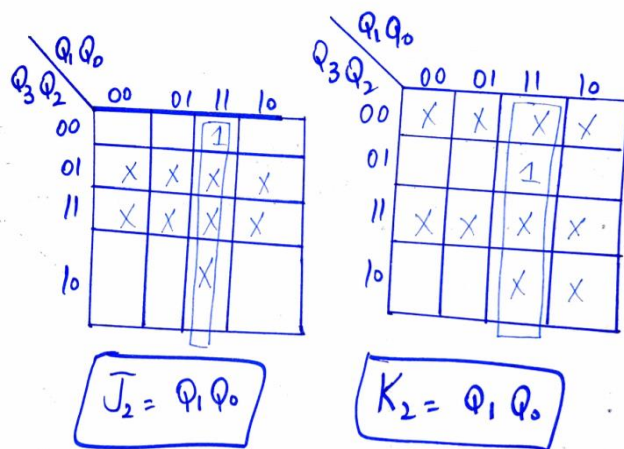
$$J_1 = \overline{Q_3} \cdot Q_0$$

$Q_3 Q_2$	$Q_1 Q_0$			
	00	01	11	10
00	X	X	1	
01	X	X	1	
11	X	X	X	X
10	X	X	X	X

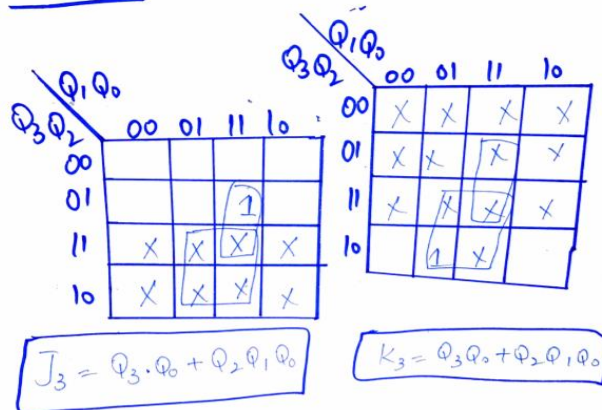
$$K_1 = \overline{Q_3} \cdot Q_0$$

* For J_2 & K_2

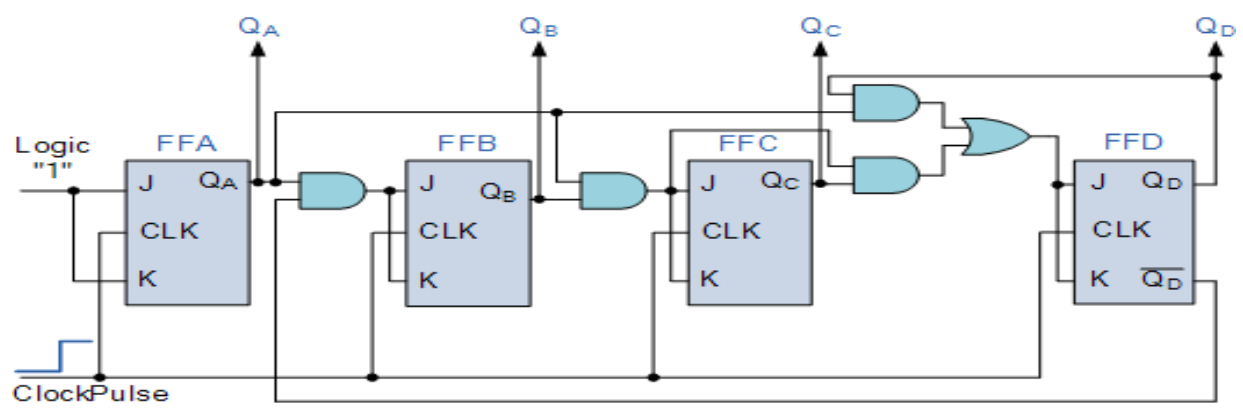
②



For J_3 & K_3



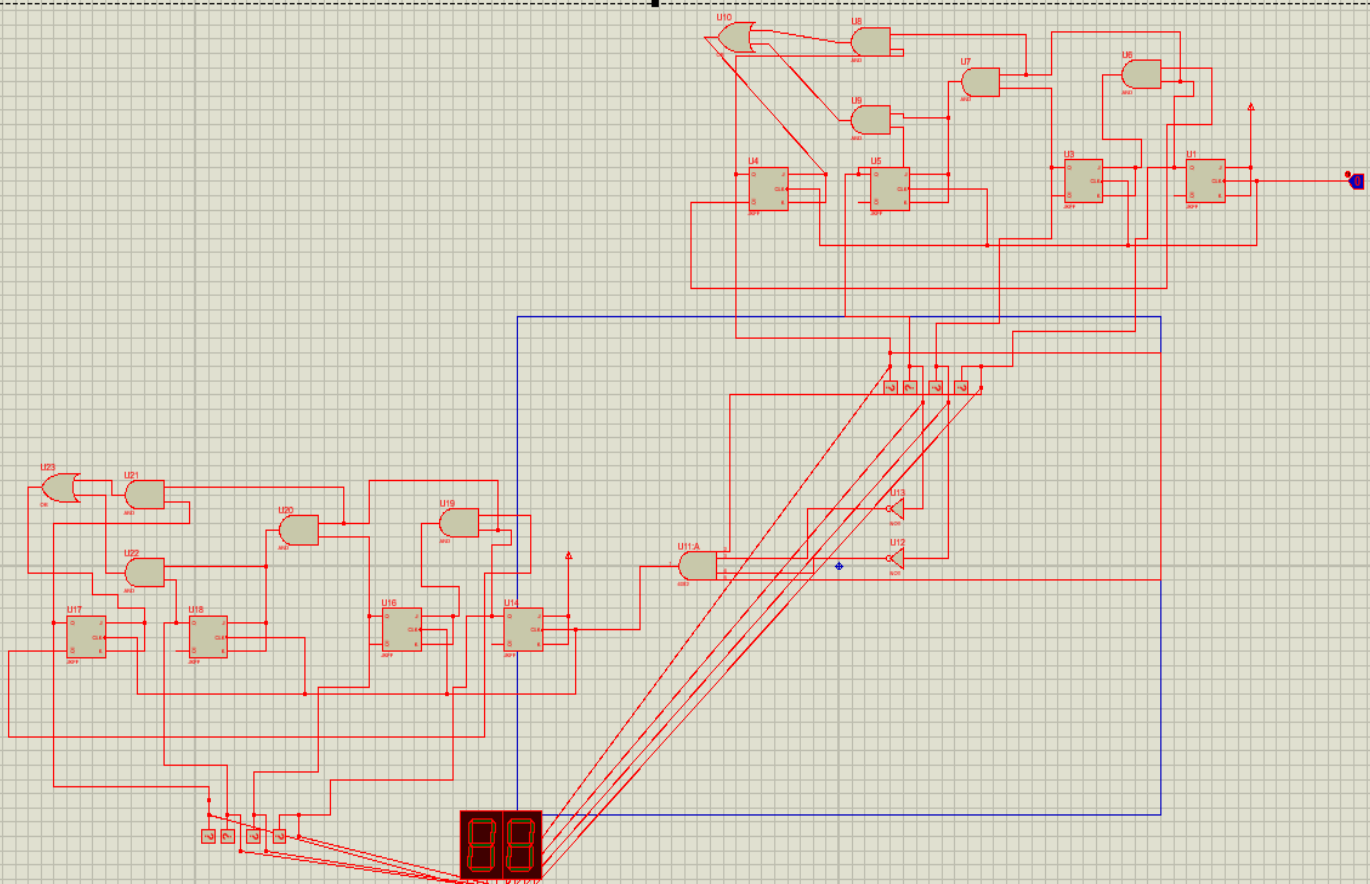
STEP 5: Circuit Diagram



Optimization Technique:

We have used K-Map to optimize the Circuit.

Circuit Diagram of Tasbeeh Counter:



THANKS!!!