深圳市一众显示科技有限公司

SHEN ZHEN TEAM SOURCE DISPLAY TECH. CO, LTD.

TFT-LCD Module Specification

Module NO.: TST055HDBS-04

Version: V1.0

☐ APPROVAL FOR SPECIFICATION ☐ APPROVAL FOR SAMPLE

For Customer's Acceptance:	
Approved by	**Comment**

Team Source Display:		
Presented by	**Reviewed by**	**Organized by**

Version No.	Date	Content	Remark
V1.0	2020-04-21	Initial Release	

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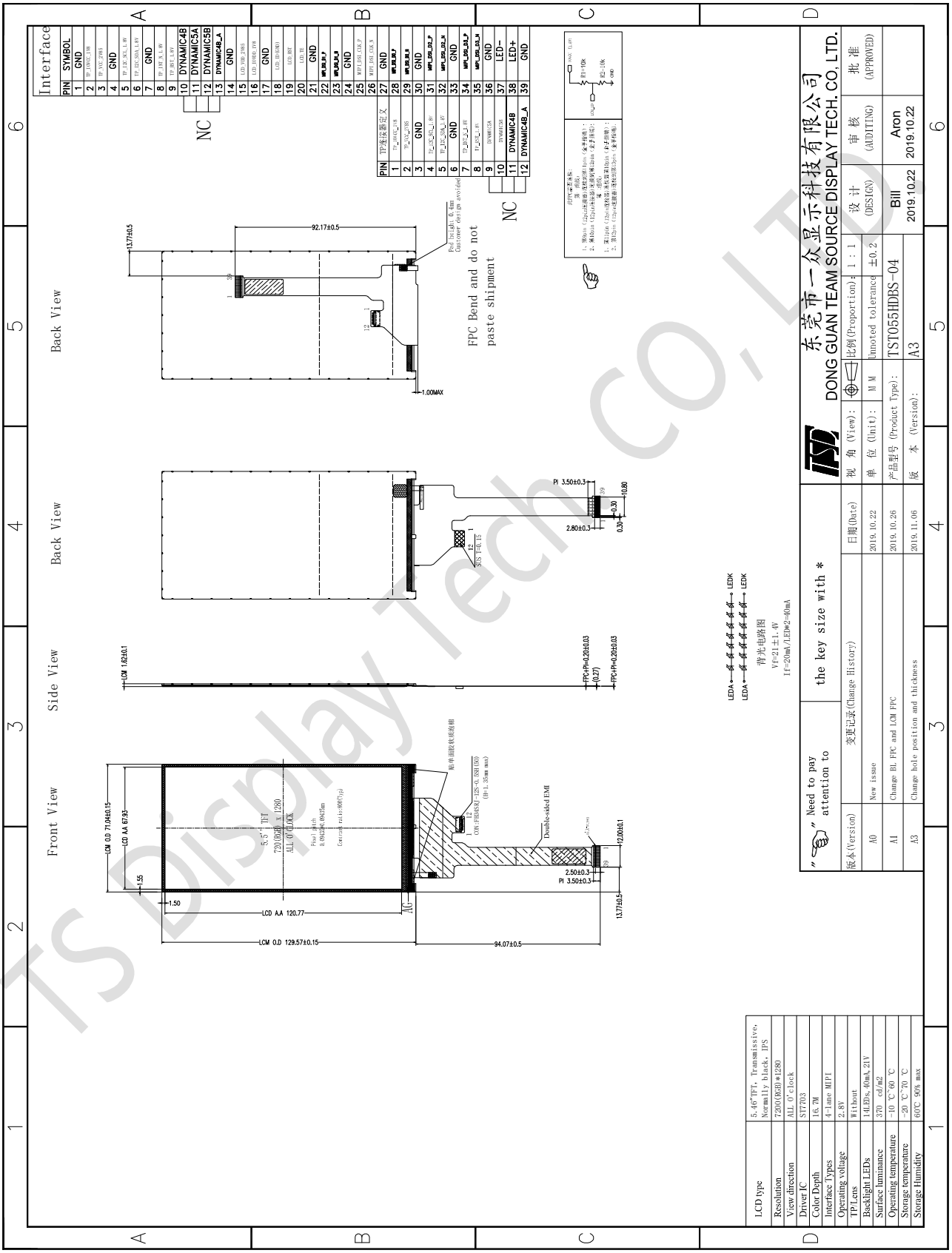
1 General Characteristics

ITEM	Specification	Unit
LCD Type	a-si TFT,Transmissive,Normally black,IPS	-
LCD Size	5.5	inch
Resolution (W x H)	720 x (RGB) × 1280	pixel
LCM (W × H × D)	71.04(W) x 129.57(H) x 1.62(D)	mm
Active Area (W × H)	67.93 (W) x 120.77(H)	mm
Pixel Pitch	0.09435 x 0.09435	mm
Viewing Direction	ALL o'clock	-
Gray Scale Inversion Direction	ALL o'clock	-
Viewing Angle	Top:80,Bottom:80; Left/ Right:80	deg.
Color Depth	16.7M	-
Pixel Arrangement	RGB-stripe	-
Backlight Type	14 LEDs	-
Surface Luminance	370	cd/m2
Surface Treatment	-	-
Polarizer	-	-
Driver IC	ST7703	-
Interface Type	MIPI	-
Input Voltage	2.8	V
With/Without TP	without	-
Weight	TBD	g

Note 1: RoHS compliant
Note 2: LCM weight tolerance: ± 5%.

2 Product drawings



3 Interface description

Pin No.	Symbol	I/O	Description	Note
1	GND	P	Ground	
2	TP_1V8	P	CTP Power supply 1.8V	
3	TP_2V85	P	CTP Power supply 2.85V	
4	GND	P	Ground	
5	TP_SCL	I	CTP I^2C clock input	
6	TP_SDA	I/O	CTP I^2C data input/output	
7	GND	P	Ground	
8	TP_INT	O	CTP interrupt signal output pin	
9	TP_RST	I	CTP reset signal input pin	
10	C4B	-	Not connect	
11	C5A	-	Not connect	
12	C5B	-	Not connect	
13	C4B_A	-	Not connect	
14	GND	P	Ground	
15	2V85	P	Power supply 2.85V	2.8V
16	1V8	P	Power supply for I/O interface, 1.8V	1.8V/2.8V
17	GND	P	Ground	
18	ID	P	LCD Identification pin	
19	RST	P	Reset signal	
20	TE	O	Frame Sync signal	
21	GND	P	Ground	
22	D1P	I/O	Data differential signal input pins.(Data lane 1)	
23	D1N	I/O	Data differential signal input pins.(Data lane 1)	
24	GND	P	Ground	
25	CLKP	I/O	Clock differential signal input pins	
26	CLKN	I/O	Clock differential signal input pins	
27	GND	P	Ground	
28	D0P	I/O	Data differential signal input pins.(Data lane 0)	
29	D0N	I/O	Data differential signal input pins.(Data lane 0)	
30	GND	P	Ground	
31	D2P	I/O	Data differential signal input pins.(Data lane 2)	
32	D2N	I/O	Data differential signal input pins.(Data lane 2)	
33	GND	P	Ground	
34	D3P	I/O	Data differential signal input pins.(Data lane 3)	
35	D3N	I/O	Data differential signal input pins.(Data lane 3)	

36	GND	P	Ground	
37	LEDK	P	Back-light Cathode	
38	LEDA	P	Back-light Anode	
39	GND	P	Ground	

4 LCM Interface Timing

4.1 Reset Timing

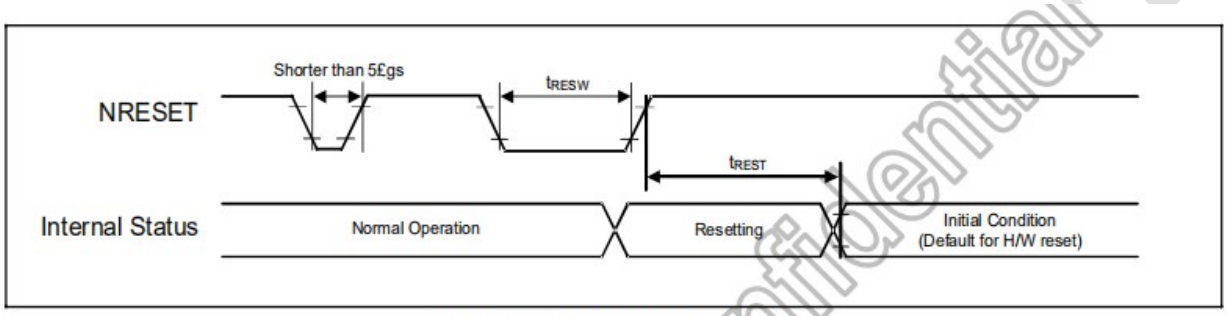


Figure 7.8: Reset input timing

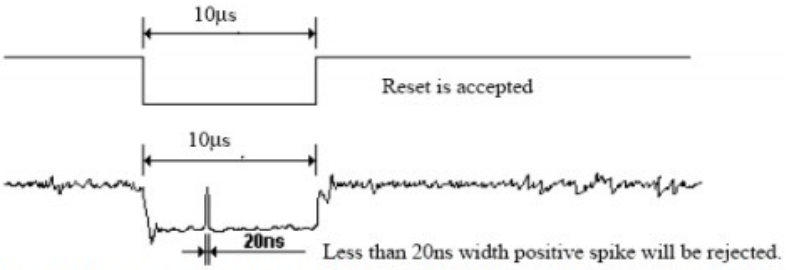
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

4.2 DSI Timing Characteristics

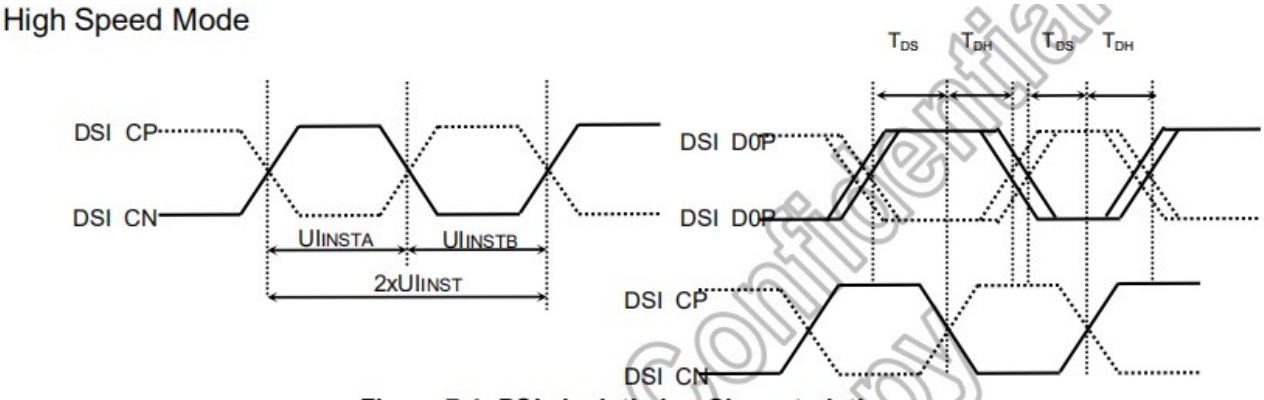


Figure 7.4: DSI clock timing Characteristics

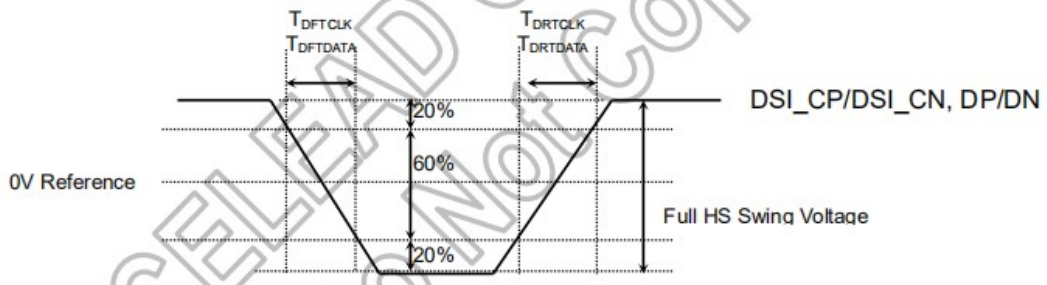


Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xU_{INST}$	TBD	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

Low Power Mode

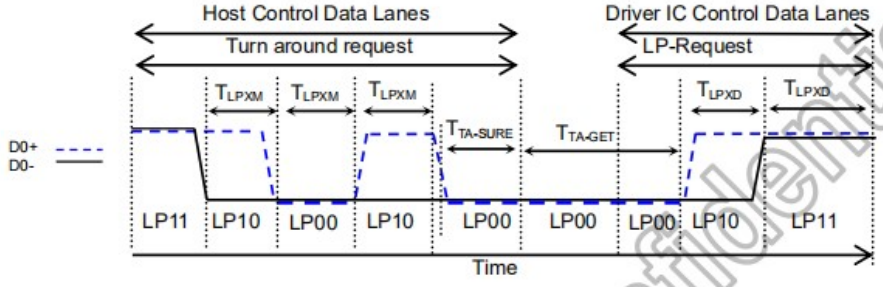


Figure 7.6: BTA from HOST to Display Module Timing

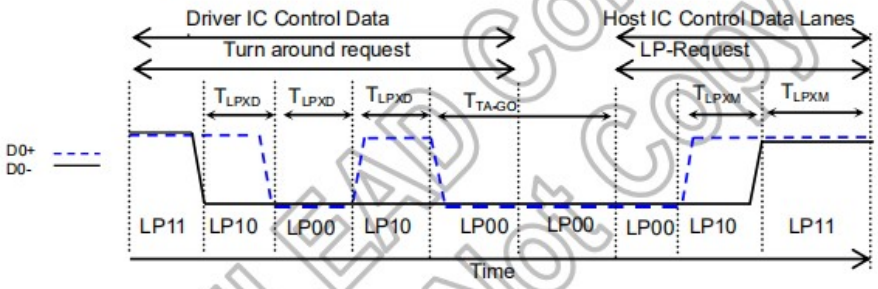


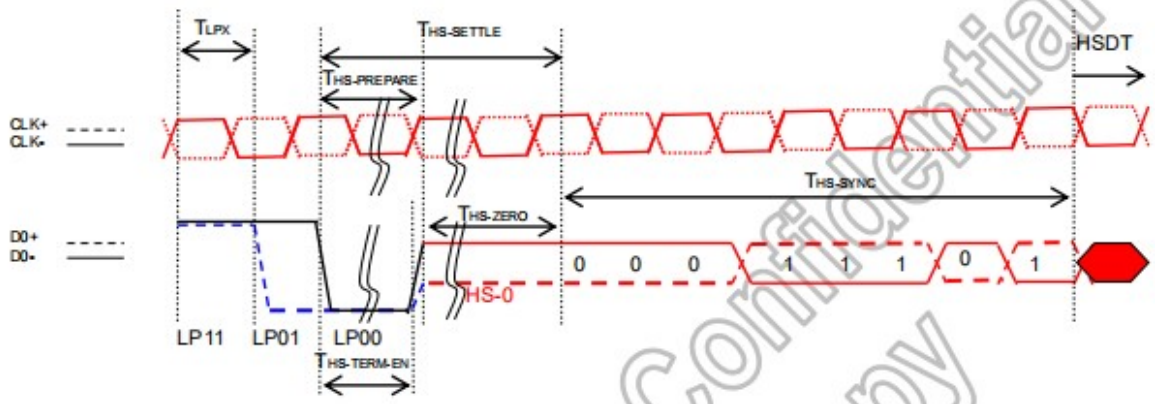
Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

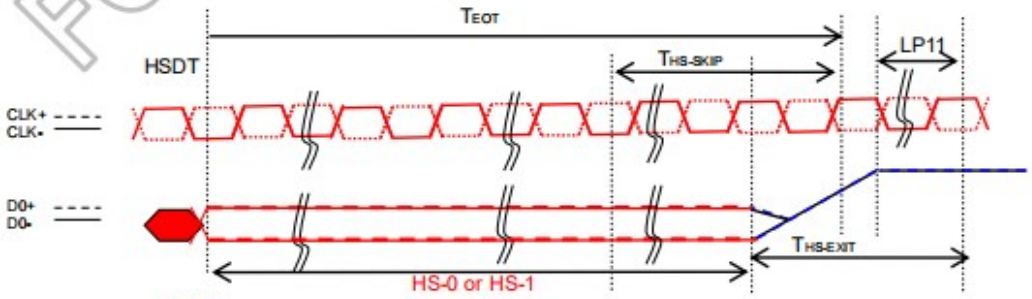
Table 7.4: DSI Low Power Mode Characteristics

DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

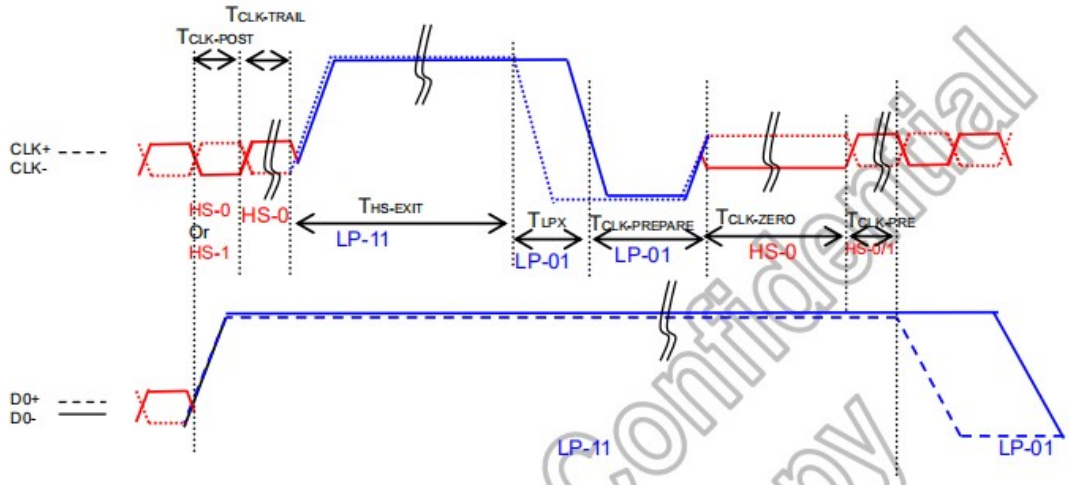
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing



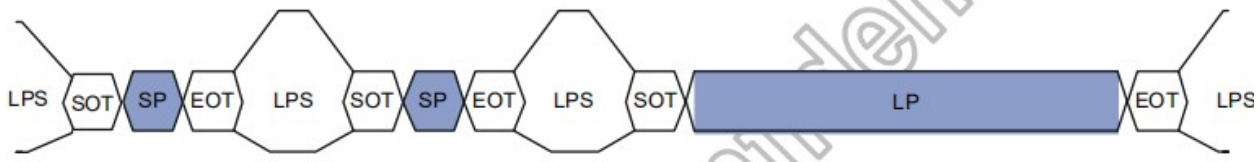
Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

4.3 Packet data

DSI Packet Level Communication

The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Below figure illustrates multiple HS Transmission packets.



LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

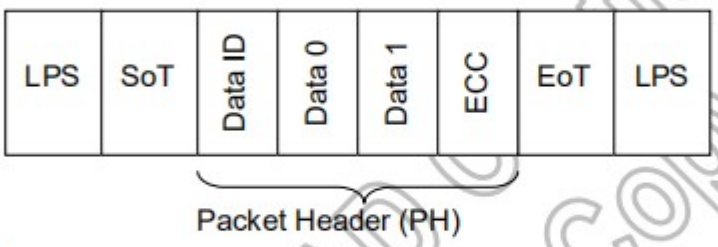
Figure 5.22: DSI multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

General Packet Structure

Short packets

Specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Below figure shows the structure of the Short packet.

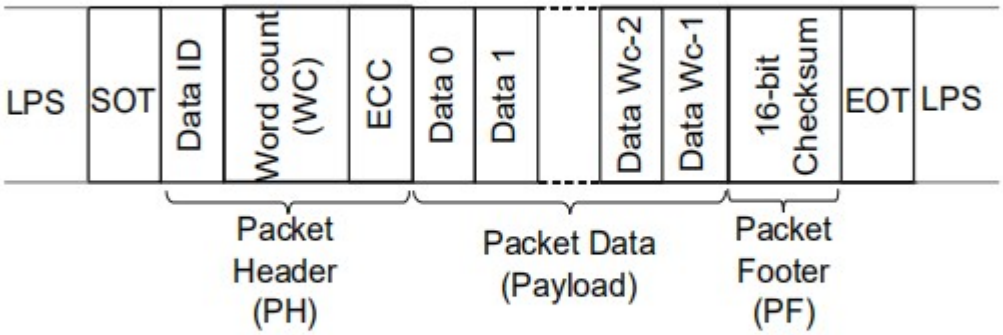


SOT: Start of Transmission
DI(Data ID): 8-bit Contain Virtual Channel Identifier and Data Type.
Data 0 and Data 1: Packet Data (8+8bit)
ECC(Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 5.23: Structure of the short packet

Long packets

Specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Below figure shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = (216-1) + 4 bytes PH + 2 bytes PF



DI (Data ID) : Contain Virtual Channel Identifier and Data Type.
WC (Word Count) : 8+8 bits The receiver use WC to define packet end.
ECC (Error Correction Code) : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer) : Mean 16-bit Checksum.

Figure 5.24: Structure of the long packet

5 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage (Analog)	VCC~GND	-0.3	4.6	V
Logic signal voltage(I/O)	IOVCC~GND	-0.3	4.6	V
Operating Temperature	TOP	-20	70	° C
Storage Temperature	TST	-30	80	° C
Humidity	RH	-	90%(Max 60° C)	RH

6 Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analog operating voltage	VCC	2.5	2.8	3.3	V
Logic operating voltage	IOVCC	1.65	1.8	3.3	V
Input Current	IDD	-	TBD	-	mA
Input Voltage ' H ' level	VIH	0.7IOVCC	-	IOVCC	V
Input Voltage ' L ' level	VIL	GND	-	0.3IOVCC	
Output Voltage ' H ' level	VOH	0.8IOVCC	-	IOVCC	
Output Voltage ' L ' level	VOL	GND	-	0.2IOVCC	

7 Backlight Characteristics

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Voltage for LED backlight	V_f	-	21	-	V
Current for LED backlight	I_f	-	40	-	mA
Power consumption	Wbl	-	840	-	mW
Uniformity	Avg	80	-	-	%
LED Life Time	-	30000	40000	-	Hrs

Note:

1.The LED life time is defined as the module brightness decrease to 50% original brightness at Ta=25°C, 60%RH ±5 %.

2. The life time of LED will be reduced if LED is driven by high current, high ambient temperature and humidity conditions.

3. Typical operating life time is an estimated data.

4. Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded .Functional operation should be restricted to the conditions described under normal operating conditions.

8 LCD Optical specifications

Item	Symbol	Condition	Specification			Unit	Remark
			Min	Typ	Max		
Response time (By Quick)	Tr+Tf	θ = 0°	-	20	30	ms	Note 5
Contrast ratio	CR	θ = 0°	-	800	-		Note 2,6
Luminance of white (Center point)	L_w	B/L on	-	310	-	cd/m²	BM-7
Viewing angle	Top	CR≧10	-	80	-	Deg.	Note 2,6,7
	Bottom	CR≧10	-	80	-		
	Left	CR≧10	-	80	-		
	Right	CR≧10	-	80	-		
Color chromaticity (CF only with ITO, light source is C light, CIE 1931)	Wx	θ = 0°	-0.03	0.3030	+0.03		Note 3
	Wy			0.3277			
	Rx			0.6514			
	Ry			0.3262			
	Gx			0.3134			
	Gy			0.6185			
	Bx			0.1502			
	By			0.0636			
NTSC			57%	60%	-		Note 3
Cross talk	Ct		-	-	2%		Note 9
Transmittance	Trans		-	3.43%	-		Note 4

Note 1: Ambient temperature = 25°C.

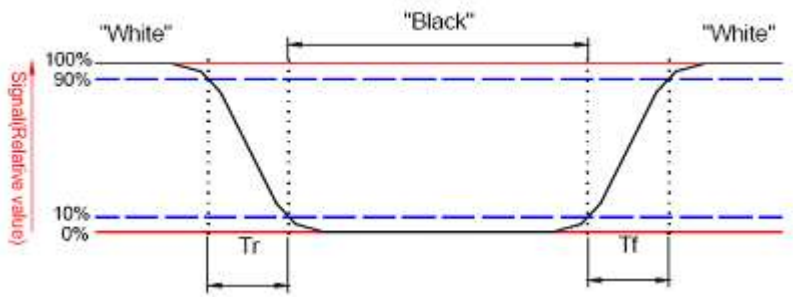
Note 2: To be measured with a viewing cone of 2°by Topcon luminance meter BM-5A.

Note 3: To be measured with Otsuta chromaticity meter LCF-2100M, CF only measure under C light simulation.

Note 4: CTC shipping status is cell without polarizer. Transmittance of Specification is cell with polarizer. The tolerance of Transmittance is ±10%.

Note 5: Definition of response time:

The output signals of TRD-100 are measured when the input signals are changed to “White” (falling time) and from “White” to “Black” (rising time), respectively. The interval is between the 10% and 90% of amplitudes. Refer to figure as below.

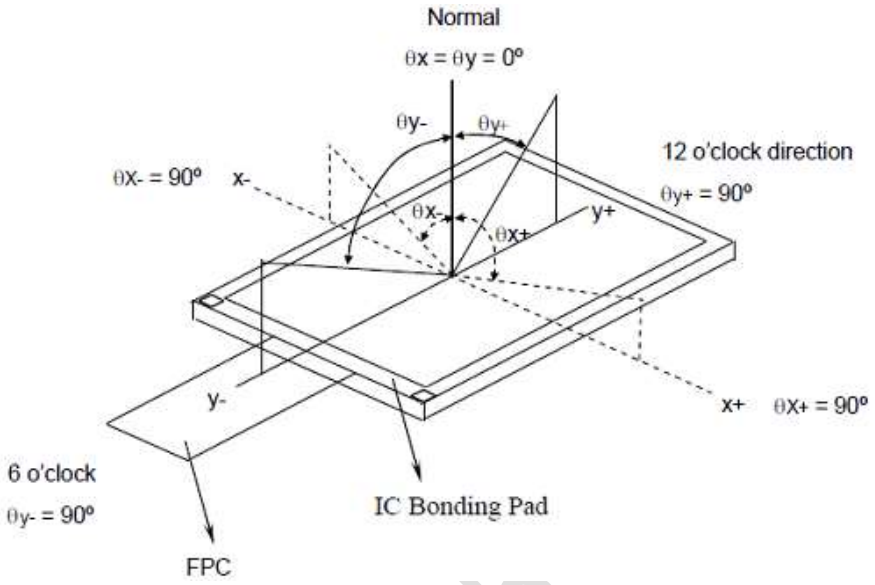


Note 6: Definition of contrast ratio:

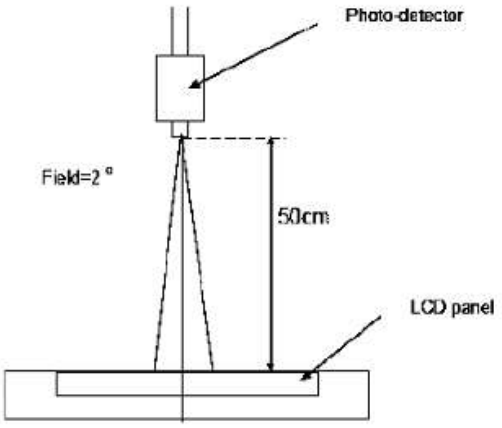
Contrast ratio is calculated by the following formula.

Contrast ratio (CR)= $\frac{\text{Brightness on the "white" state}}{\text{Brightness on the "black" state}}$

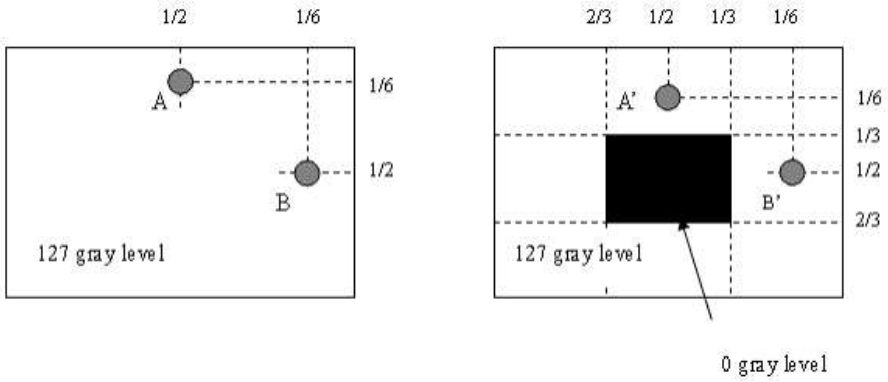
Note 7: Definition of viewing angle



Note 8: Optical characteristic measurement setup.



Note 9:



l LA-LA'l / LA x 100%= 2% max., LA and LA' are brightness at location A and A'.

l LB-LB'l / LB x 100%= 2% max., LB and LB' are brightness at location B and B'.

9 RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	INSPECTION AFTER TEST
1	High Temperature Storage	70±2°C/96 hours	Inspection after 2~4 hours storage at room temperature and humidity. The condensation is not accepted. The sample shall be free from defects: 1. Air bubble in the LCD 2. Seal leak 3. Non-display 4. Missing segments 5. Glass crack
2	Low Temperature Storage	-20±2°C/96 hours	
3	High Temperature Operating	60±2°C/96 hours	
4	Low Temperature Operating	-10±2°C/96 hours	
5	Temperature Cycle	-30±2°C ~ 25~ 70± 2°C × 10 cycles (30 min.) (5min.) (30min.)	
6	Damp Proof Test	60°C ±5°C × 90%RH/96 hours	
7	Vibration Test	Frequency 10Hz~55Hz Stroke: 1.5mm Sweep: 10Hz~150 Hz~10Hz 2 hours For each direction of X, Y, Z	
8	Shock Test	Half-sine, wave, 300m/s	
9	Packing Drop Test	Height: 80 cm 1 corner, concrete floor	
10	Electrostatic Discharge Test	C=150pF, R=330 Ω Air: ±8KV 150pF/330Ω 30 times Contact: ±4KV,20 times	

10 Suggestions for using LCD modules

10.1 Handling of LCM

1. The LCD screen is made of glass. Don't give excessive external shock, or drop from a high place.
2. If the LCD screen is damaged and the liquid crystal leaks out, do not lick and swallow. When the liquid is attach to your hand, skin, cloth etc, wash it off by using soap and water thoroughly and immediately.
3. Don't apply excessive force on the surface of the LCM.
4. If the surface is contaminated, clean it with soft cloth. If the LCM is severely contaminated, use Isopropyl alcohol/Ethyl alcohol to clean. Other solvents may damage the polarizer. The following solvents is especially prohibited: water , ketone Aromatic solvents etc.
5. Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

6. Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
7. Don't disassemble the LCM.
8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

9. Do not alter, modify or change the the shape of the tab on the metal frame.
10. Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
11. Do not damage or modify the pattern writing on the printed circuit board.
12. Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector
13. Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
14. Do not drop, bend or twist LCM.

10.2 Storage

1. Store in an ambient temperature of 5 to 45 C, and in a relative humidity of 40% to 60%. Don't expose to sunlight or fluorescent light.
2. Storage in a clean environment, free from dust, active gas, and solvent.
3. Store in antistatic container.