# EXP 6502

Technical reference

v1.0 12/04/2023 Eric Nunney

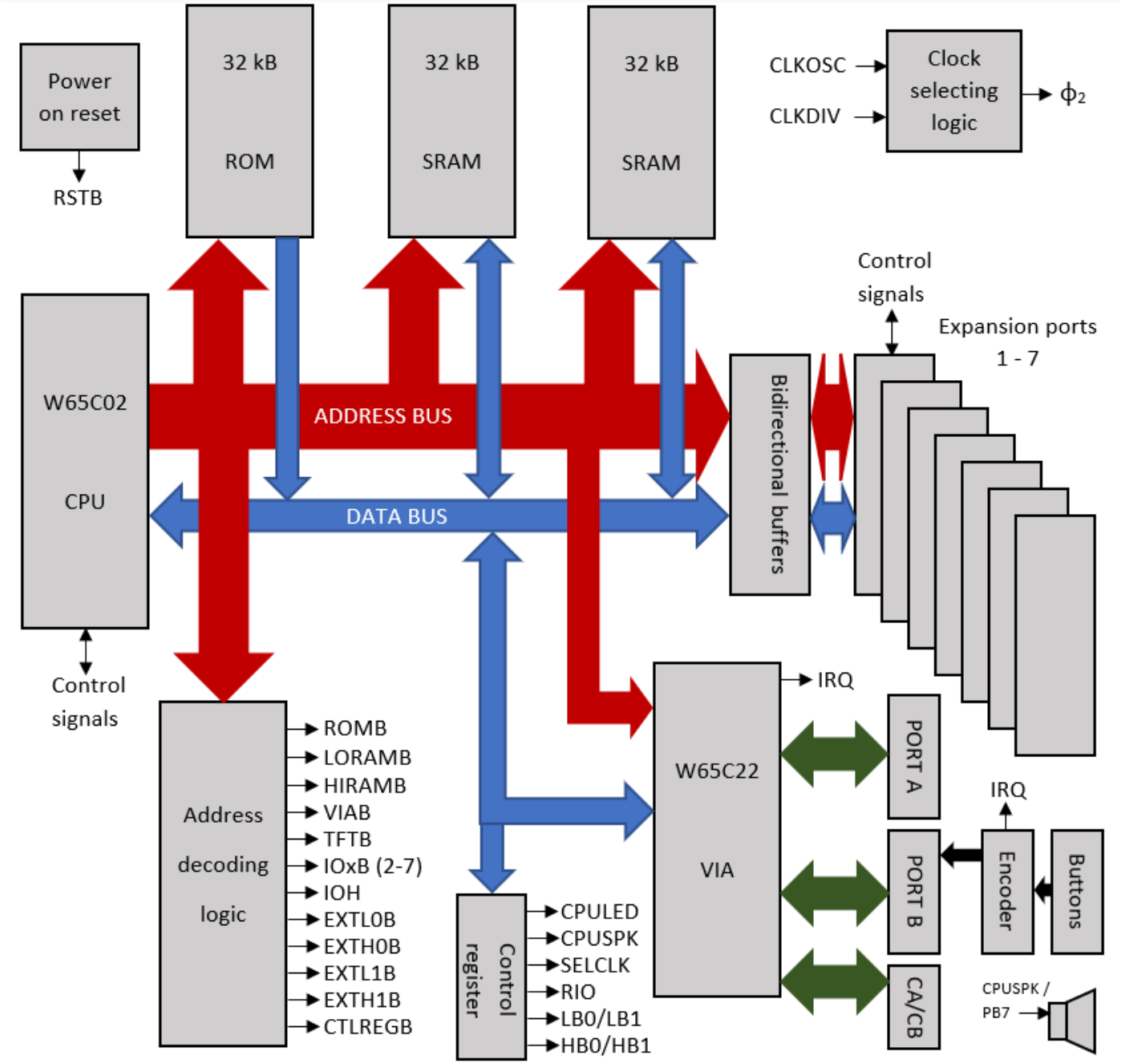
Table of contents

# I. Specifications

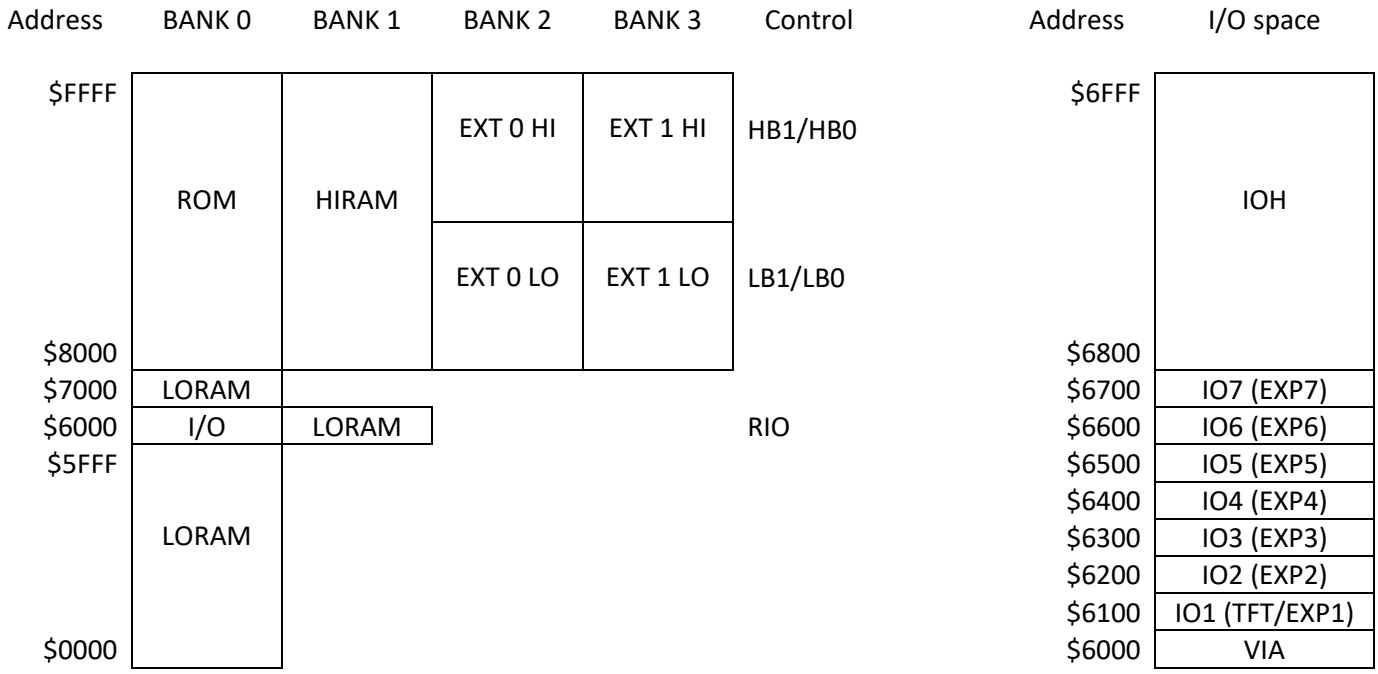
- W65C02 microprocessor at up to 8 MHz (MOS 6502 compatible)
- 64 kB SRAM
- 32 kB EEPROM (read only)
- W65C22 Versatile Interface Adapter
- 7 general purpose expansion ports
- Bank switching, access to up to 160 kB of memory
- Software controllable glitchless clock switching (8 MHz / configurable fraction of 8 MHz)
- Power-on reset circuit
- Built-in beeper speaker
- Built-in LED
- 5 built-in push buttons with interrupt capability
- Single 5V DC power input
- CMOS only logic ICs (higher speed / less power)

# II. Architecture

## 1. Block diagram



## 2. Memory map




The lower half of the address space contains 32 kB of RAM (the low RAM) and the I/O space. The I/O space sits between $6000 and $6FFF. It can be switched out to access the 4 kB of RAM located at the same memory addresses.

The I/O space is made of two parts. The bottom one is divided in 8 pages, each of these controlling one I/O peripheral. The first I/O page is reserved for the built in VIA. The 7 others are each attributed to a different expansion port. The top part of the I/O space, IOH, is available on every expansion port, in case they need more I/O addresses.

The upper half of the address space is divided in two blocks, each of them is multiplied in 4 banks. One bank in each block can be selected at a time, and the two blocks can have a different bank selected.

The first bank gives access to the ROM of the computer, it is selected by default at start up or after reset.

The second one gives access to 32 kB of RAM, the high RAM.

The third and fourth ones give access to memory placed on the expansion ports. The chip select signals of these banks are accessible on any expansion port.

## 3. Bank switching

The bank switching in the lower half of the address space is controlled by the RIO signal, bit 3 of the control register. It allows switching the window between $6000 and $6FFF to the I/O space, when RIO is low, or to the low RAM, when RIO is high.

The bank switching in the upper half of the address space is controlled by the LB0, LB1, HB0 and HB1 signals, bits 4 to 7 of the control register. The bits LB0 and LB1 control the bank switching in the bottom block ($8000 to $BFFF). HB0 and HB1 control the switching in the top block ($C000 to $FFFF).

The first bank, bank 0, is mapped to the ROM, in the two blocks. It is enabled in the bottom block when LB1 = 0 and LB0 = 0, and in the top block when HB1 = 0 and HB0 = 0.

The bank 1, is mapped in the two blocks to the high RAM. It is enabled in the bottom block when LB1 = 0 and LB0 = 1, and in the top block when HB1 = 0 and HB0 = 1.

The bank 2 enables the external high memory 0, EXT0HI in the top block when HB1 = 1 and HB0 = 0. It enables the external low memory 0, EXT0LO when LB1 = 1 and LB0 = 0.

The bank 3 enables the external high memory 1, EXT1HI in the top block when HB1 = 1 and HB0 = 1. It enables the external low memory 1, EXT1LO when LB1 = 1 and LB0 = 1.

## 4. Control register

The control register allows the software to switch the memory banks, to change the clock speed and to directly control an LED and the beeper speaker.

It is located at address $0000 of the address space, in the zero page of the 6502 microprocessor, to allow faster access.

The function of each of its bits is given below:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HB1 | HB0 | LB1 | LB0 | RIO | SELCLK | CPUSPK | CPULED |

- → Bit 0: CPULED
  - Control signal for the built in LED.
- → Bit 1: CPUSPK
  - Can be connected to the built in beeper speaker.
- → Bit 2: SELCLK
  - Control the current clock source for the main clock $\phi_2$.
    - 0: divided clock 1: Oscillator clock
- → Bit 3: RIO
  - Select the I/O space or the low RAM between $6000 and $6FFF.
    - 0: I/O space 1: low RAM
- → Bit 4: LB0
  - LSB of the number of the selected bank in the bottom block of the upper half of the address space.
- → Bit 5: LB1
  - MSB of the number of the selected bank in the bottom block of the upper half of the address space.
- → Bit 6: HB0
  - LSB of the number of the selected bank in the top block of the upper half of the address space.
- → Bit 7: HB1
  - MSB of the number of the selected bank in the top block of the upper half of the address space.

## 5. Clock switching

The main clock of the computer, $\phi_2$, can be switched between two different sources: the oscillator clock or a divided version of the oscillator clock.

The default oscillator frequency is 8 MHz. A counter and a JK flip-flop generate a divided version of this clock. The dividing ratio can be configured with 4 jumpers on the computer. The ratio is between /2 when the value configured by the jumpers is set to 15, and /32 when the value is 0.

The dividing ratio follows the formula: R = 2*(16-n), where n is the value configured with the jumpers.

The oscillator clock can also be replaced by an external clock, placed on any of the expansion port. The external clock must be selected with the corresponding jumper.

## 6. Expansion ports

The computer has 7 general purpose expansion ports.

They give access to buffered versions of the address and data buses of the computer, to various control signals of the microprocessor and to the selecting signals for the external memory banks. They also have access to some pins of the VIA.

The expansion ports have access to the main clock, $\phi_2$, as well as the oscillator clock and the divided clock. This feature allows an expansion card to keep using one of these clocks while the computer has switched to another one, for instance for slow peripherals that couldn't handle the oscillator frequency. It is worth noting that the CPU can't access these peripherals while the clocks are different, as it would have an unpredictable behavior.

Any expansion port can take control of the computer, by setting low the EXTCTLB signal, which disables the busses of the CPU and reverses the direction of the address and data buffers. The RDY signal should be put low at the same time to effectively halt the CPU.

The expansion port 1 has an additional two pins header socket placed next to it. It is intended to be connected to the read and write pins of a TFT LCD screen (controlled by an ILI9341 IC or compatible) for write only access when the port 1 is connected to such a screen.

The following table is a pinout of an expansion port. They are all identical excepted the I/O select line IOxB which is different for each port, allowing to access each expansion card as a different I/O peripheral.

| | | | |
|---|---|---|---|
| GND | 2 | 1 | GND |
| VDD | 4 | 3 | VDD |
| AE15 | 6 | 5 | IOxB |
| AE14 | 8 | 7 | CLKOSC |
| AE13 | 10 | 9 | IOHB |
| AE12 | 12 | 11 | CLKDIV |
| AE11 | 14 | 13 | RW |
| AE10 | 16 | 15 | PHI2 |
| AE9 | 18 | 17 | RSTB |
| AE8 | 20 | 19 | PHI1 |
| GND | 22 | 21 | GND |
| VDD | 24 | 23 | VDD |
| GND | 26 | 25 | GND |
| AE7 | 28 | 27 | DE7 |
| AE6 | 30 | 29 | DE6 |
| AE5 | 32 | 31 | DE5 |
| AE4 | 34 | 33 | DE4 |
| AE3 | 36 | 35 | DE3 |
| AE2 | 38 | 37 | DE2 |
| AE1 | 40 | 39 | DE1 |
| AE0 | 42 | 41 | DE0 |
| VDD | 44 | 43 | VDD |
| GND | 46 | 45 | GND |
| NMIB | 48 | 47 | IRQEXTB |
| RDY | 50 | 49 | EXTCTLB |
| EXTCLK | 52 | 51 | MLB |
| SYNC | 54 | 53 | VPB |
| EXTL0B | 56 | 55 | EXTH0B |
| EXTL1B | 58 | 57 | EXTH1B |
| CA1 | 60 | 59 | CA2 |
| CB1 | 62 | 61 | CB2 |
| GND | 64 | 63 | GND |

The function of each of the pins is given below:

| Signal | Active when | Function |
|---|---|---|
| AE0 to AE15 | X | buffered address bus |
| DE0 to DE7 | X | buffered data bus |
| IOxB | LOW | enabled when the corresponding memory page is accessed |
| IOHB | LOW | enabled when the top half of the I/O space is accessed |
| EXTL0B | LOW | enabled when the bottom bloc of bank 2 is accessed |
| EXTL1B | LOW | enabled when the bottom bloc of bank 3 is accessed |
| EXTH0B | LOW | enabled when the top bloc of bank 2 is accessed |
| EXTH1B | LOW | enabled when the top bloc of bank 3 is accessed |
| CLKOSC | X | Clock at the output of the crystal oscillator |
| CLKDIV | X | Divided clock |
| PHI2 | X | Main clock (CPU clock) |
| PHI1 | X | Inverted version of the main clock, generated by the CPU |
| EXTCLK | X | Input for an eventual external clock |
| RSTB | LOW | Reset signal |
| RW | X | Read (1) /write (0) signal |
| IRQEXTB | LOW | Interrupt request signal |
| NMIB | LOW | Non maskable interrupt request signal |
| EXTCTLB | LOW | Disables the data busses of the CPU and change the direction of the buffers |
| RDY | HIGH | When put LOW, halts the CPU. When it goes low indicate a WAI instruction |
| MLB | LOW | Active during the last three cycles of read-modify-write instructions of the CPU |
| VPB | LOW | Active when the CPU is retrieving interrupt vectors from memory |
| SYNC | HIGH | Active when the CPU is fetching an instruction opcode |
| CA1 | X | CA1 pin of the VIA |
| CA2 | X | CA2 pin of the VIA |
| CB1 | X | CB1 pin of the VIA |
| CB2 | X | CB2 pin of the VIA |
| VDD | X | +5V DC |
| GND | X | Ground |

# 7. Built-in I/O

The computer has a built in Versatile Interface Adapter (VIA), of which the two GPIO ports are accessible on 2 pin header sockets. The CA1, CA2, CB1 and CB2 pins of the VIA are accessible on another pin header socket, as well as on every expansion port.

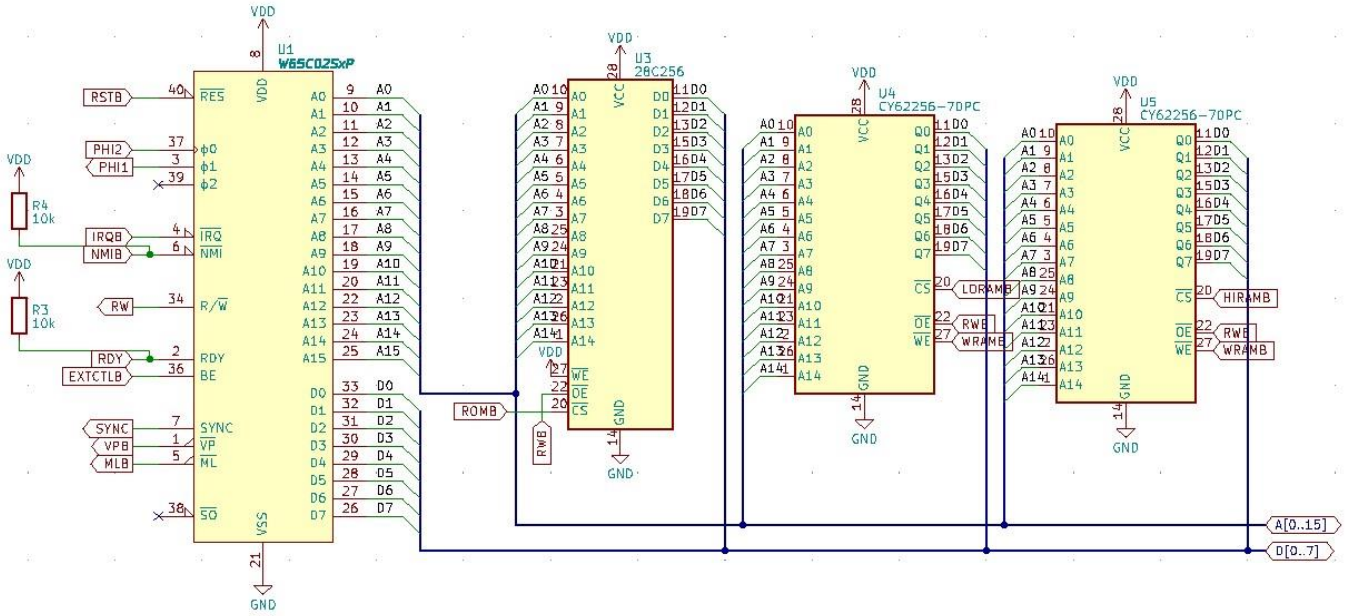
The bits 3, 4 and 5 of the PORT B of the VIA can be connected to an 8 to 3 priority encoder with jumpers. The inputs of the encoder are driven by 5 push buttons. When a button is pressed, the corresponding code is sent to the VIA. The encoder can generate an interrupt either directly or through the CA2 pin of the VIA, depending on the jumper configuration.

The VIA can also drive the built in beeper speaker when the jumper connected to the speaker is set accordingly.

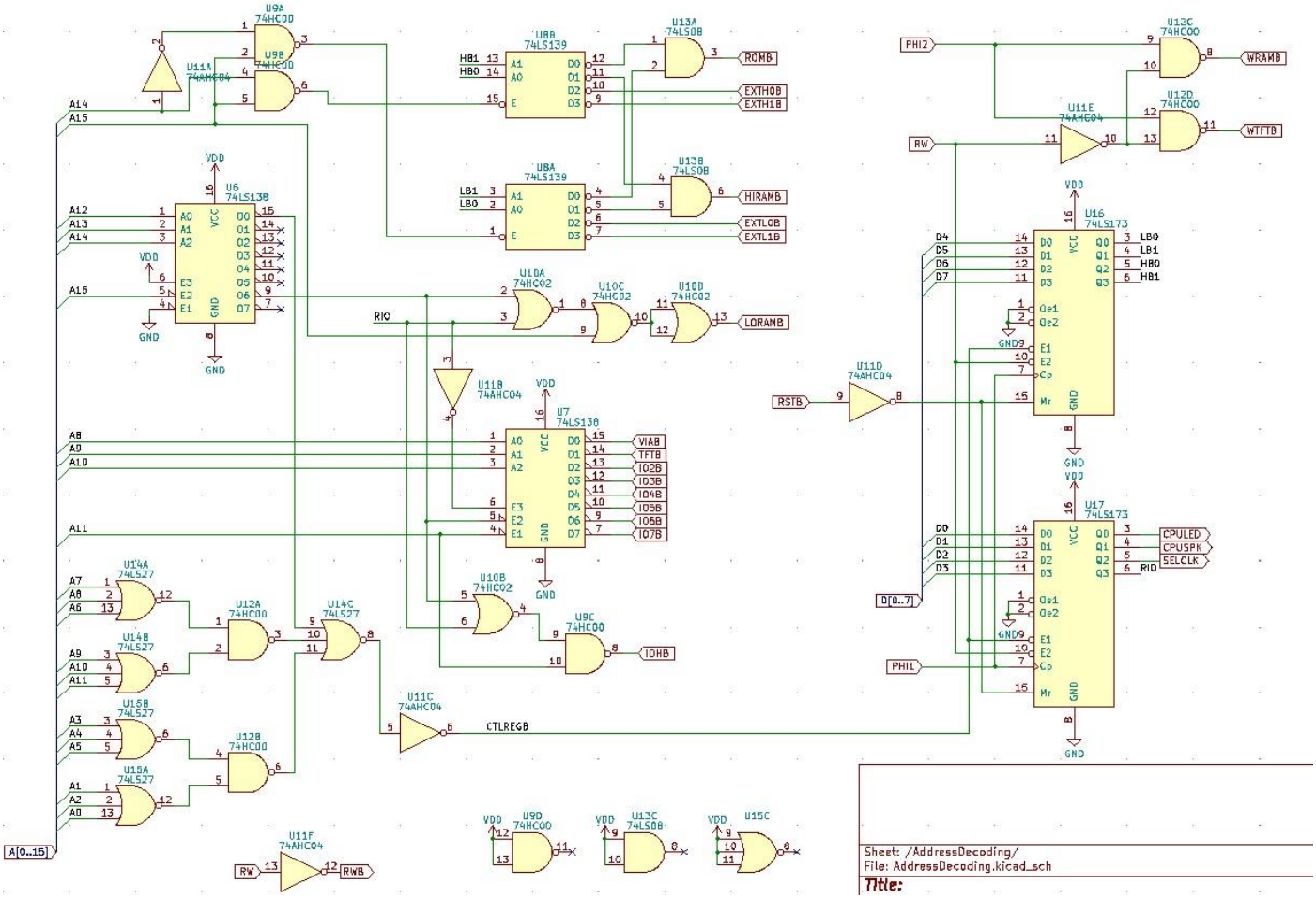
The control register is connected to the red LED and can be connected to the speaker.

# III. Schematic diagram

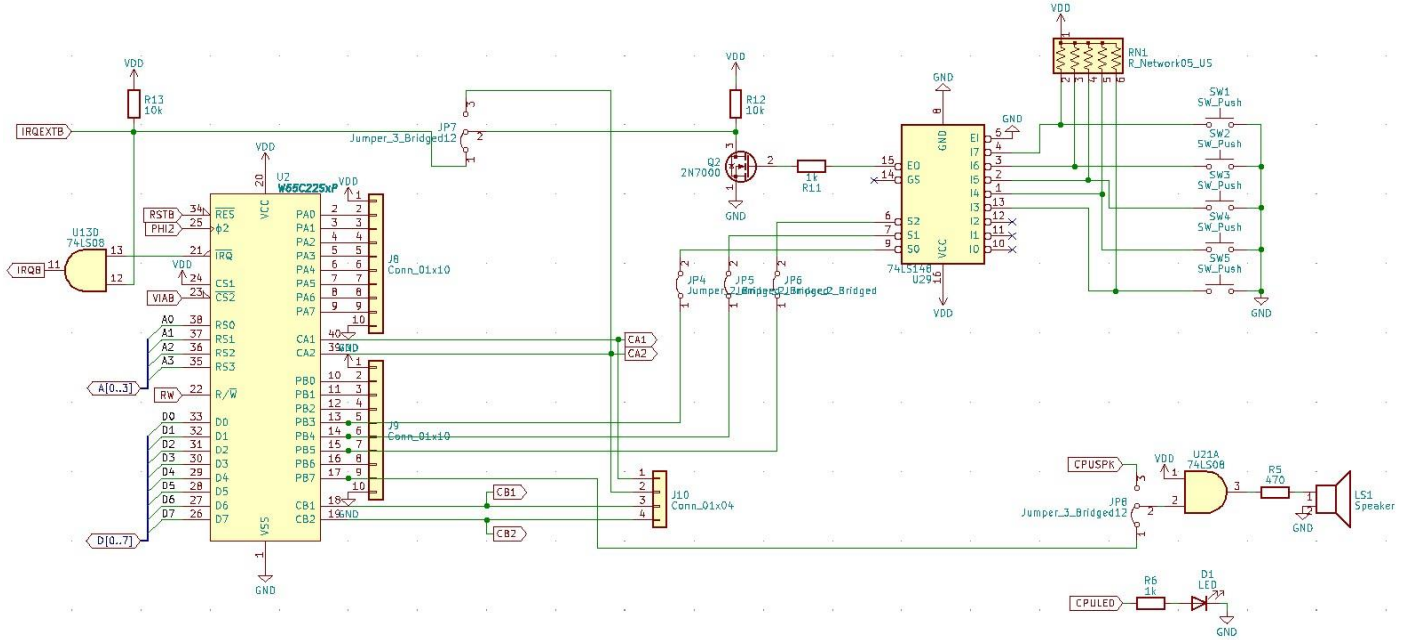
## 1. CPU and memory



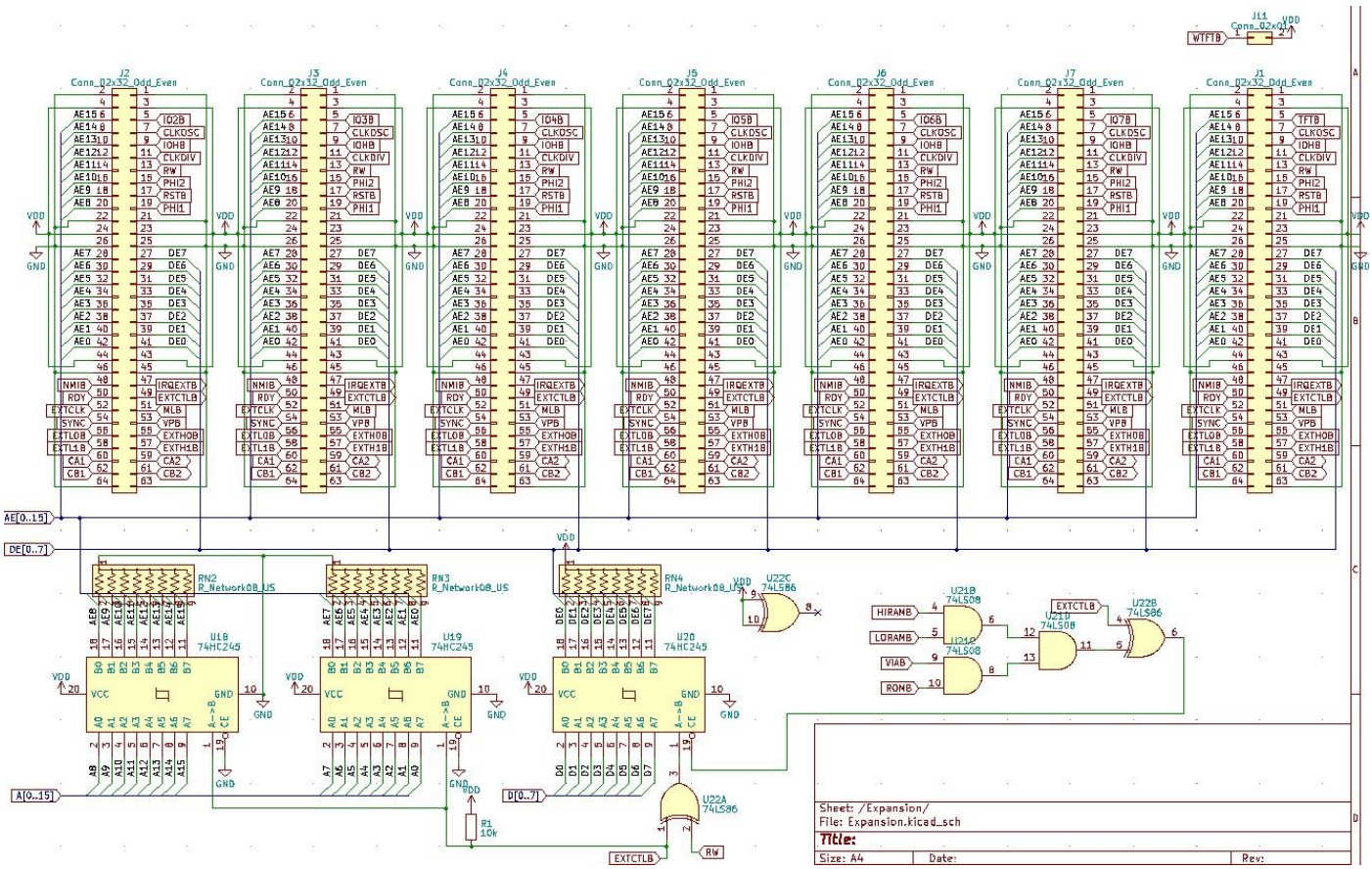
## 2. Address decoding



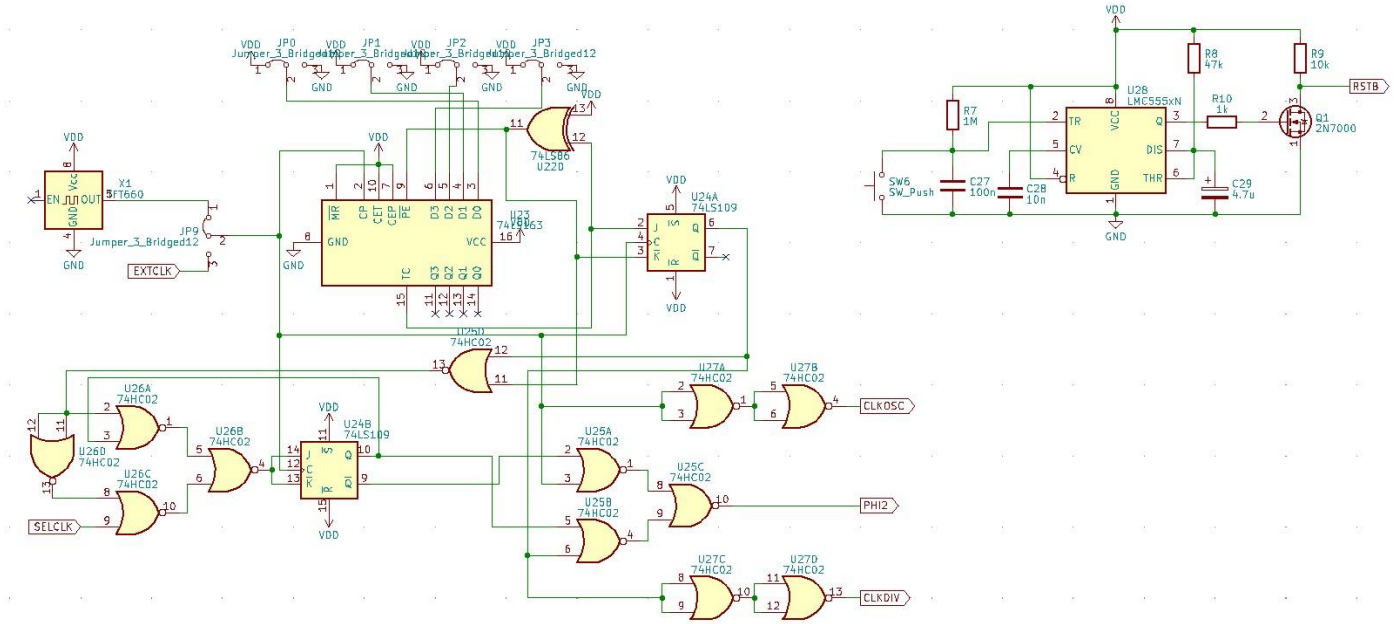

## 3. I/O



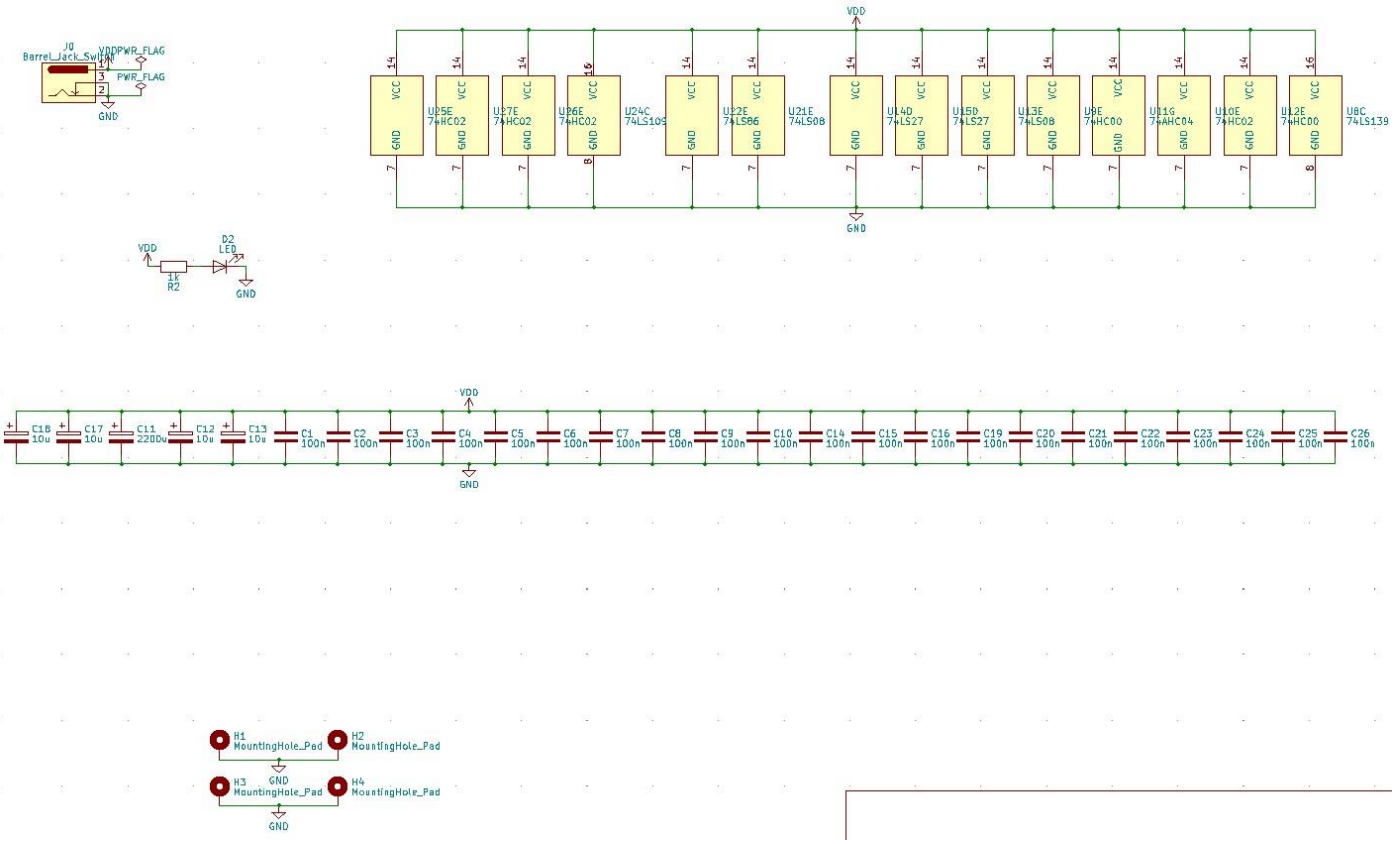
## 4. Expansion ports




## 5. Clock and reset

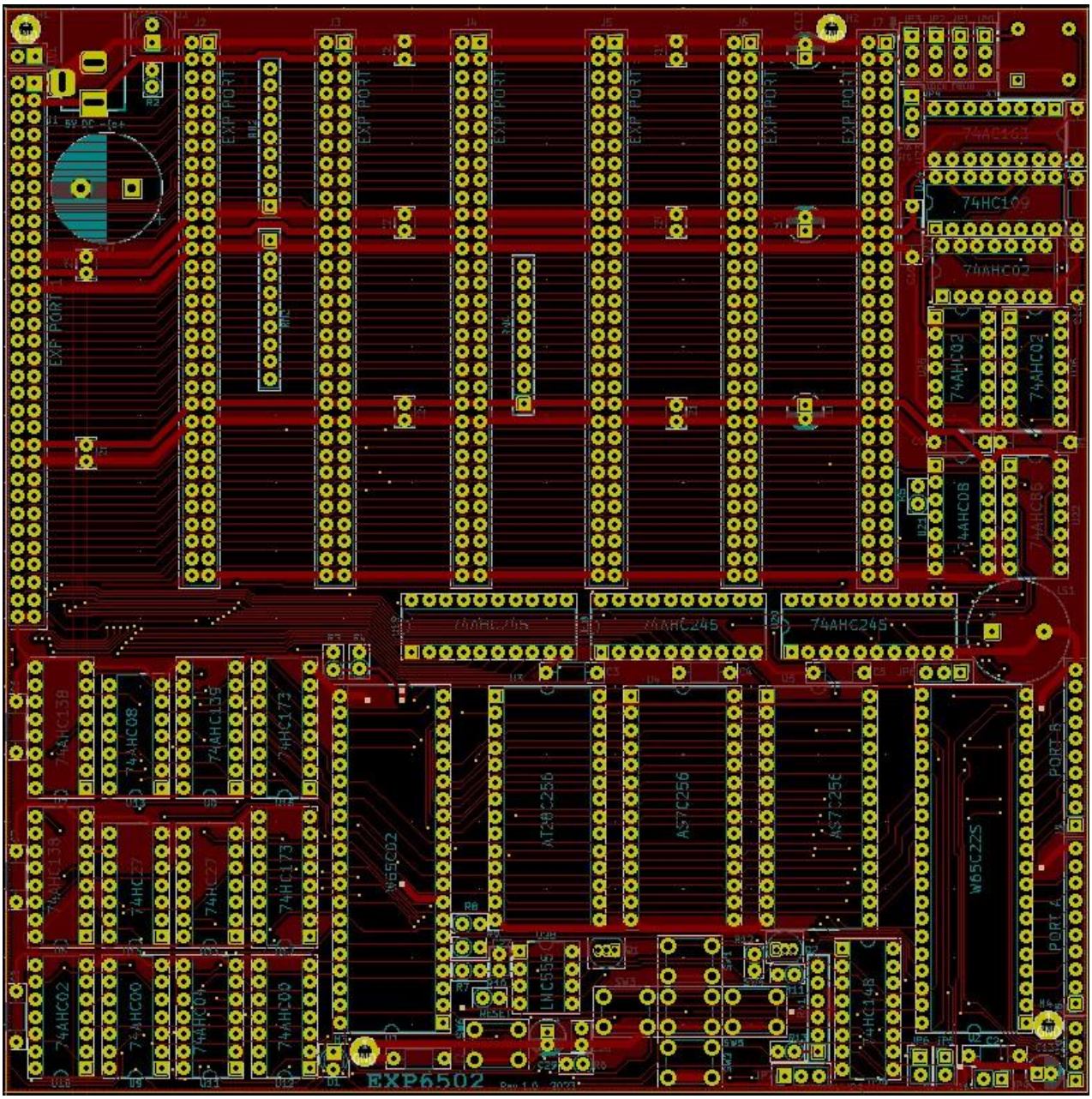


# 6. Power

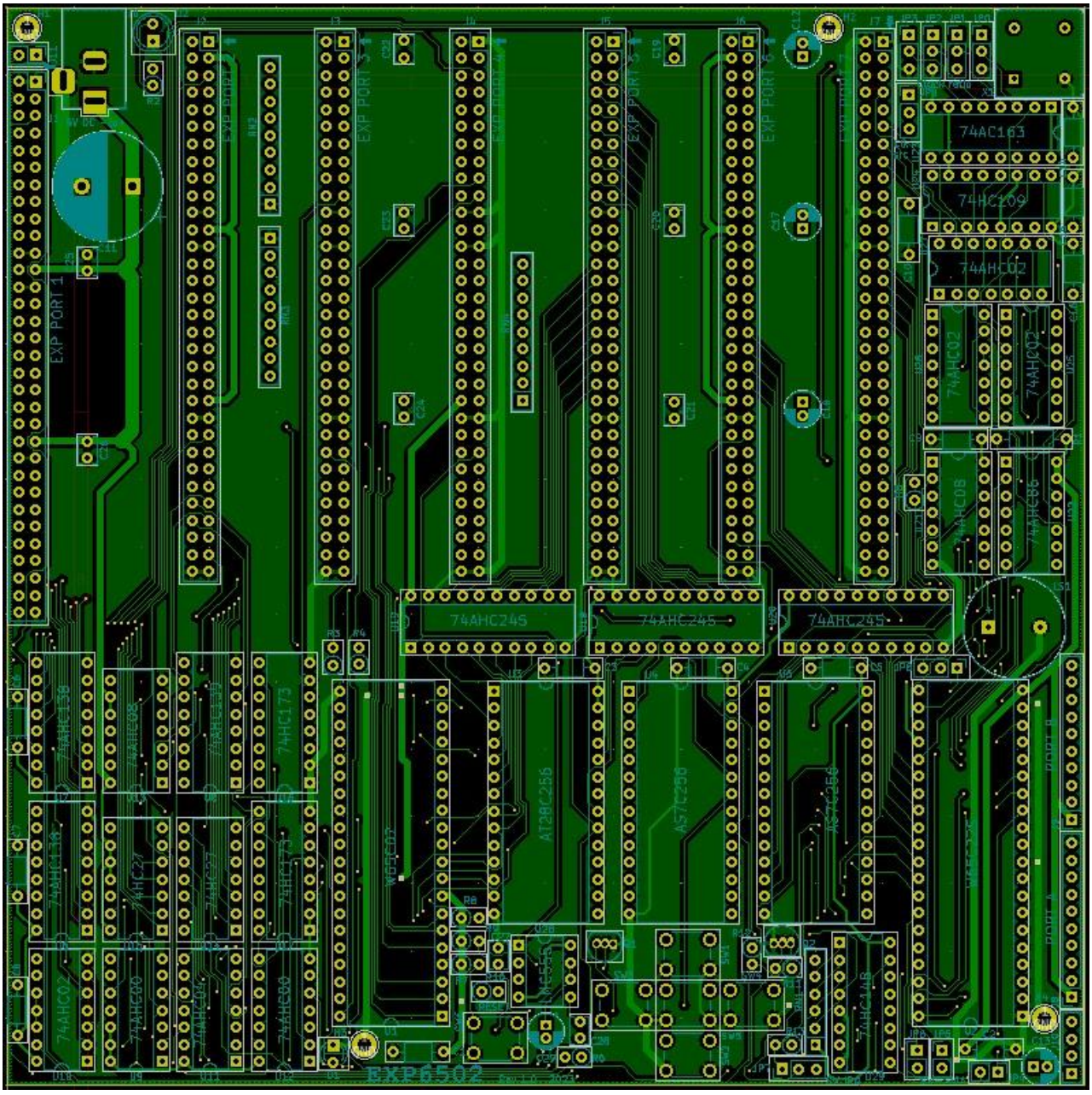

J0
Barrel_Jack_Switch
VDDPWR_FLAG
PWR_FLAG
GND
VDD
U25E 74HC02
U27E 74HC02
U26E 74HC02
U24C 74LS109
U22E 74LS86
U21E 74LS08
U14D 74LS27
U15D 74LS27
U13E 74LS08
U8E 74HC00
U11G 74AHC04
U10E 74HC02
U12E 74HC00
U8C 74LS139
VCC
GND
D2
LED
R2
1k
C18 10u
C17 10u
C11 220u
C12 10u
C13 10u
C1 100n
C2 100n
C3 100n
C4 100n
C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 100n
C14 100n
C15 100n
C16 100n
C19 100n
C20 100n
C21 100n
C22 100n
C23 100n
C24 100n
C25 100n
C26 100n
H1 MountingHole_Pad
H2 MountingHole_Pad
H3 MountingHole_Pad
H4 MountingHole_Pad

# IV. PCB layout

## 1. Top layer



2. Bottom layer



# 3. Jumper configuration

The following table explains the function of each jumper on the computer:

| Jumper | Connection | Function |
|---|---|---|
| JP0 | 1-2 | The bit 0 of the value loaded in the divider counter at each new CLKDIV cycle is HIGH |
| | 2-3 | The bit 0 of the value loaded in the divider counter at each new CLKDIV cycle is LOW |
| JP1 | 1-2 | The bit 1 of the value loaded in the divider counter at each new CLKDIV cycle is HIGH |
| | 2-3 | The bit 1 of the value loaded in the divider counter at each new CLKDIV cycle is LOW |
| JP2 | 1-2 | The bit 2 of the value loaded in the divider counter at each new CLKDIV cycle is HIGH |
| | 2-3 | The bit 2 of the value loaded in the divider counter at each new CLKDIV cycle is LOW |
| JP3 | 1-2 | The bit 3 of the value loaded in the divider counter at each new CLKDIV cycle is HIGH |
| | 2-3 | The bit 3 of the value loaded in the divider counter at each new CLKDIV cycle is LOW |
| JP4 | None | Open connection |
| | 1-2 | Connect output S0 of the encoder to the pin 3 of the PORT B of the VIA |
| JP5 | None | Open connection |
| | 1-2 | Connect output S1 of the encoder to the pin 4 of the PORT B of the VIA |
| JP6 | None | Open connection |
| | 1-2 | Connect output S2 of the encoder to the pin 6 of the PORT B of the VIA |
| JP7 | 1-2 | The encoder directly drives the IRQEXTB signal |
| | 2-3 | The encoder is connected to the CA2 pin of the VIA, to trigger an interrupt |
| JP8 | 1-2 | The speaker is connected to the pin 7 of the PORT B of the VIA (timer 1 output) |
| | 2-3 | The speaker is connected to the pin 1 of the control register, CPUSPK |
| JP9 | 1-2 | The CLKOSC clock comes from the built in crystal oscillator |
| | 2-3 | The CLKOSC clock is connected to the EXTCLK pin of the expansion connectors |