ELECTRICAL ENGINEERING DEPARTMENT
ELL201 DIGITAL ELECTRONIC CIRCUITS

MAJOR TEST

Date: May 7, 2016 **Time: 3:30PM to 5:30PM** **Total Marks: 40**

Q1. Design a Moore finite state machine that will recognize the sequence x = 0110 and output the sequence p = 0001 as this sequence occurs. This implies that output p = 0 when the first received bit of x = 0. Then output p = 0 if the next bit of x = 1; output p = 0 again if the following bit of x = 1. Finally, if the last (fourth) bit of x = 0, output p = 1. Hence, output p = 0 until the sequence x = 0110 is received, at which time output p = 1. Overlapping sequences have to be detected. Draw the State Diagram and the State Table. Design the finite state machine using only JK Flip Flops (and no other Flip Flops) and other logic gates. (6)

Q2. Design a new negative edge triggered flip flop (say) AB flip flop, starting from a NAND based clocked SR Latch with the condition that if A is equal to B the flip flop output retains the previous value and if A is not equal to B the output takes the value of A. Use any Gates of your choice including Multiplexers. (6)

Q3. Develop a Moore finite state machine to implement a serial adder (using the minimum possible number of states) for adding two bits 'a' and 'b' being serially input to the the adder. The states of this finite state machine could be defined based on the values of Carry and Sum, for example a state M00 could be defined as having Carry = 0 and Sum = 0. The output (z) of this finite state machine is the value of the Sum. Draw the State Diagram and the State Table. Design the required finite state machine using only D Flip Flops (and no other Flip Flops). (6)

Q4. Design a synchronous counter to count in the sequence (1->5->7->3->4->1->5..). Use +ve edge triggered flipflops (2 J-K Flip Flops and 1 T Flip Flop) to realize the counter using minimum number of logic gates. The left most and right most Flip Flops have to be JK Flip Flops and the middle Flip Flop has to be T Flip Flop. You may designate the output of the left most Flip Flop to be Q_2 and the right most as Q_0. (6)

Q5. Develop a finite state machine to implement a parity-bit generator that employs a code to generate the parity-bit. In this parity-bit generator, suppose that a 4-bit sequqential data is to be received; the first 3 bits constitute the message, and the fourth bit is always 0 (equivalent to a blank). To this *3*-bit message, an additional *1* bit is added, making the parity of the resulting (*4*)-bit sequential data odd. If the number of 1's in the 3-bit message is odd, the parity bit is to remain 0. If the number of 1's is even, a 1 bit is to be generated and inserted in the fourth position to make the parity of the 4-bit string odd. In either case, after the fourth bit, transition is to be to a reset state, in which the machine is ready to receive the next message sequence. Draw the State Diagram and the State Table. Design the required finite state machine using only D Flip Flops (and no other Flip Flops). (6)

Q6. When making a normal encoder circuit it converts base 4 input, represented by four lines each representing a number in base 4 number, to binary output represented by 2 lines. In a normal base 4 number to binary encoder, only one of the four inputs will be 1, the input being labeled I_3, I_2, I_1 and I_0. For example if I_3 is 1 and the rest 0 the encoded output, represented by lines Z_1 Z_0, will be 11. In a priority encoder more than one of the inputs could have a value 1, unlike in a normal base 4 number to binary encoder. We need to design a priority encoder that encodes such that when the input has more than one line equal to1, the output will be corresponding to the input with lowest subscript. For example if the inputs are I_3 =1 and I_1 =1 and the rest zero, the output should be 01. Draw a truth table for this encoder and realize it using 2 input NOR gates. (5)

Q7. Draw the timing diagrams, showing the output (M) and the states as a function of time, for the input (N) to the finite state machine whose state diagram is given below. Assume negative edge triggered flip flops are used in this machine. Realize this state machine using one T Flip Flop and one D Flip Flop. (5)