Department of Computer Science & Engg.
COL 216 Computer Architecture : Major Test

Date: 07.05.2016 Time: 13:00-15:00 Max marks: 30

[Note: Do Question 1 and any five out of the remaining eight.]

1) Consider a 5-stage pipelined processor designed to execute subset of ARM instructions (as per Lab exercise 4, but without data forwarding and branch prediction).

How many cycles will this pipeline take to execute the code of a function shown on right, counting from the first cycle of the first instruction to the last cycle of the last instruction? Also, compute the average number of cycles per instruction (CPI).

Assume that on seeing a branch instruction, any instruction in the pipeline following that branch is flushed out. Branch decision as well as address computation are done in EX stage.

```
        .text
Func:   ldr r1, =A
        add r2, r1, #800
        mov r3, #0
Loop:   cmp r1, r2
        beq Over
        ldr r4, [r1]
        cmp r4, #0
        addeq r3, r3, #1
        add r4, r4, #10
        str r4, [r1],
        add r1, r1 #4
        b Loop
Over:   mov pc, lr
        .data
A:      .space (800)
```

(5)

2) For the pipeline and program of Q.1, find the change in (i) the number of cycles and (ii) average CPI if data forwarding is introduced.

(5)

3) In the pipeline of Q.1, the data memory is replaced by a *4-way set associative* data cache and a main memory with the following specifications.

- Cache size = 4 KB, block size = 32B, hit time = 1 cycle, no *concurrent read* and no *forwarding*, write policy = *write through no write allocate*, no write buffer.
- For main memory, read or write time = 4 cycles for a word and 11 cycles for a block.

Find (i) the number of cycles and (ii) average CPI for the given program, assuming the cache to be empty in the beginning.

(5)

4) Three masters A, B and C are connected to a bus that uses daisy chaining bus arbitration scheme with *request*, *release* and *grant* signals. Draw a block diagram showing the scheme. Assume that A has the highest priority and C has the lowest. Draw the waveforms of all the signals if the requests arrive in the following order – B, C, A. Assume the bus to be free initially. When the requests from C and A arrive, the bus is being used by B.

(5)

5) Draw a flow chart to show how memory access is made in a system with virtual memory, cache (1 level) and TLB. Assume that the cache is physically addressed. The page table is in main memory. Note that the cache may contain information from any part of the main memory.

(5)

6) Consider addition of N signed 2's complement numbers one by one in a loop as shown on right. Overflows are ignored. Prove that if there is no overflow resulting from the last addition, r3 will have the correct sum even if there were overflows resulting from the previous additions.

```
        mov r3, #0
Loop:   ldr r4, [r1]
        add r3, r3, r4
        add r1, r1, #4
        cmp r1, r2
        bne Loop
```

(5)

7) A system has a common bus connecting processor, memory and 4 peripheral controllers. Each peripheral controller has 4 registers which are seen by the processor as memory mapped I/O ports (2 input and 2 output). Assume certain addresses for these ports in the memory address space and show the circuit for connecting these registers to the bus.

(5)

8) Exceptions may be classified into internal or external exceptions. These may be further classified into intentional or unintentional. Give an example of each of the four classes. Indicate which of these are synchronous and which are asynchronous. Give reasons.

(5)

9) A web server needs to be designed as per the architecture shown below to service 500 requests per second on average. Each request is received in the form of a 256 byte packet. Only 1% of the requests are for a file download (average size 1MB), 5% are for web pages with graphics (average size 200KB) and the remaining 94% are for textual web pages (average size 10KB). All the data is sent out over the network in the form of 1 KB packets. Each packet has 100 bytes of header information in addition to 256B of data for incoming packets or 1KB of data for outgoing packets. Each disk drive has a data transfer rate of 5 MB/s, a rotational speed of 10,000 rpm and an average seek time plus controller delay of 5 ms. The disk read operations are in terms of 10 KB at a time from consecutive sectors on a track. The web server process executes 10,000 instructions per request. Apart from this, the operating system requires 10,000 instructions per disk read and 2,000 instructions per packet input or output (including processing or creation of packet header). Because of cache misses, transfer of one cache block of size 64 bytes is required per 100 instructions between memory and cache. Note that cache is within the block labelled CPU in the figure. Give CPU MIPS, P-M bus bandwidth, I/O bus bandwidth, number of disk drives and network bandwidth to meet these requirements?

(5)