Santa Clara University

***Department of Electrical and Computer Engineering***

**Hardware-Software Co-Design – ELEN 503**

Spring Quarter 2023, Thursday 5:10 – 7:00pm

**Instructor:**

Hoeseok Yang (SCDI 4025P)
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**Office Hours**: Tuesday 2:30-4:00pm, Thursday 2:30-4:00pm
(or by appointments. Online meeting is available on request)

**References**:

- *System Design, Modeling, and Simulation using Ptolemy II*, available here.
- *Introduction to Embedded Systems, Second Edition: A Cyber-Physical Systems Approach*, 2nd Edition, ISBN-13: 978-0262533812, available here.
- IEEE Standard for Standard SystemC(R) Analog/Mixed-Signal Extensions Language Reference Manual, available here.
- Gurobi Optimizer Reference Manual, available here.
- Opt4J: a modular framework for meta-heuristic optimization, available here.

**Prerequisites**:

- Basic knowledge of logic design (ELEN 21) and computer architecture (ELEN 122)
- Basic knowledge of C/C++ and Java (for Ptolemy II, Opt4J, and Gurobi)

**Grading Policy:**

Midterm (written): 30%, homework: 30% and final exam (written): 40%

**Course Objectives**

- Understand the basic HW/SW co-design or Electronic System Level (ESL) design flow: specification, HW/SW partitioning, HW/SW co-simulation/co-verification, and HW/SW co-synthesis.
- Understand the basic concept of model-based system design and various models of computation.
- Understand the state-of-the-art HW/SW co-design methodologies and their applications (case studies).
- Have experiences using the following tools in HW/SW co-design
    - Ptolemy-II (for modeling/specification and simulation)
    - SystemC for Transaction Level Modeling (TLM)
    - Gurobi (Integer Linear Programming) or OPT4J (Evolutionary Algorithm) (for combinational optimizations)

**Exams**:

Two written exams: midterm (35%) and final (35%)

**Homework**:

There will be three homework assignments (10% each): modeling/specification (Ptolemy II or Simulink), TLM (SystemC), mapping/scheduling optimization (Gurobi or Opt4J) or PYNQ

**[tentative schedule]**

| | **Topics** |
|---|---|
| **Week 1 (Introduction)** | April 6th<br>- Introduction to HW/SW co-design<br>- Cyber-Physical Systems |
| **Week 2 (Model of Computation, State Machines)** | April 13th<br>- Model-of-Computations Overview<br>- State Machines |
| **Week 3 (Process Networks and Dataflow)** | April 20th<br>- Problems with Threads<br>- Kahn Process Network (KPN) and Dataflow<br>- System modeling in Ptolemy II (or Simulink)<br>- Homework #1 |
| **Week 4 (Process Networks and Dataflow, Cont'd)** | April 27th<br>- Kahn Process Network (KPN) and Dataflow<br>- Synchronous Dataflow |
| **Week 5 (Transaction Level Modeling)** | May 4th<br>- Transaction Level Modeling<br>- System C |
| **Week 6 (HW/SW Co-Synthesis with Xilinx Pynq)** | May 11th<br>- HW/SW Co-Design Practice with Xilinx Pynq<br>- Homework #2 |
| **Week 7 (Midterm)** | May 18th |
| **Week 8 (HW/SW Co-Synthesis with Xilinx Pynq)** | May 25th<br>- HW/SW Co-Design Practice with Xilinx Pynq |
| **Week 9 (Optimizations)** | June 1st<br>- Combinational optimization tools<br>- Integer Linear Programming, Evolutionary Algorithm<br>- Homework #3 |
| **Week 10 (HW/SW Co-Design Examples)** | June 8th<br>- HW/SW Co-Design examples<br>- Embedded machine learning |