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ELEN 511 - Advanced Computer Architecture
ASSIGNMENT #1 GEM 5
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## Homework #1

# Part 0 - setup:

```
SHCXX] X86/ext/drampower/src/Parametrisable.cc -> .os
     SHCXX] X86/ext/drampower/src/libdrampower/LibDRAMPower.cc -> .os
    SHCXX] X86/ext/drampower/src/CAHelpers.cc -> .os
    SHCXX] X86/ext/drampower/src/CmdHandlers.cc -> .os
    SHCXX] X86/ext/drampower/src/MemBankWiseParams.cc -> .os
    SHCXX] X86/ext/iostream3/zfstream.cc -> .os
    SHCXX] X86/ext/nomali/lib/gpu.cc -> .os
    SHCXX] X86/ext/nomali/lib/gpublock.cc -> .os
    SHCXX] X86/ext/nomali/lib/gpucontrol.cc -> .os
    SHCXX] X86/ext/nomali/lib/jobcontrol.cc -> .os
    SHCXX] X86/ext/nomali/lib/jobslot.cc -> .os
   AR] -> X86/ext/iostream3/libiostream3.a RANLIB] -> X86/ext/iostream3/libiostream3.a
    SHCXX] X86/ext/nomali/lib/mali_midgard.cc -> .os
        AR] -> X86/ext/drampower/libdrampower.a
   RANLIB] -> X86/ext/drampower/libdrampower.a
    SHCXX] X86/ext/nomali/lib/mali_t6xx.cc -> .os
    SHCXX] X86/ext/nomali/lib/mali t7xx.cc -> .os
    SHCXX] X86/ext/nomali/lib/addrspace.cc -> .os
    SHCXX] X86/ext/nomali/lib/mmu.cc -> .os
    SHCXX] X86/ext/nomali/lib/nomali_api.cc -> .os
        AR] -> X86/ext/nomali/libnomali.a
   RANLIB] -> X86/ext/nomali/libnomali.a
      CXX] X86/base/date.cc -> .o
     LINK]
            -> X86/gem5.opt
scons: done building targets.
*** Summary of Warnings ***
Warning: Header file <png.h> not found.
         This host has no libpng library.
         Disabling support for PNG framebuffers.
Warning: Couldn't find HDF5 C++ libraries. Disabling HDF5 support
```

I first started off by downloading virtualbox and had to build an image twice because the first one did not have enough disk drive to properly run Ubuntu and gem5. Furthermore, everything was fairly seamless other than the actual build command which required me to think outside the box and experiment with how to make scons work for my system. Ultimately, I was able to build gem5 as seen in the screenshot above.

#### Part 1 - creating a simple configuration:

```
Desktop$ cd gem5
lkim@lkim-VirtualBox:~/Desktop/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Nov 10 2022 21:46:19
gem5 started Nov 11 2022 01:41:38
gem5 executing on lkim-VirtualBox, pid 3751
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the addr
ess range assigned (512 Mbytes)
0: system.remote gdb: listening for remote gdb on port 7000
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
Hello world!
Exiting @ tick 454646000 because exiting with last active thread context
lkim@lkim-VirtualBox:~/Desktop/gem5$
```

This portion was fairly simple as the documentation was very procedural and was informative because it explained the purpose of each parameter that composed of our simple configuration.

# Part 2 - Write and run your own test application:

# **Configuration 3:**

```
system.clk_domain.clock = '1GHz'
system.cpu = TimingSimpleCPU()
system.mem ctrl.dram = DDR3 1600 8x8()
```

```
Returning '/home/lkim/Desktop/gem5/configs/tutorial/part1/sieveofe.o'build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
78498
Exiting @ tick 2904978744369 because exiting with last active thread context
lkim@lkim-VirtualBox:~/Desktop/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Nov 11 2022 14:52:49
gem5 started Nov 11 2022 15:53:00
gem5 executing on lkim-VirtualBox, pid 10514
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py
Global frequency set at 100000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the addr
ess range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7002
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall rseq(...)
build/X86/sim/mem_state.cc:443: info: Increasing stack size by one page.
build/X86/sim/syscall_emul.hh:1015: warn: readlink() called on '/proc/self/exe' may yield unexpected
results in various settings.
       Returning '/home/lkim/Desktop/gem5/configs/tutorial/part1/sieveofe.o'
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
Exiting @ tick 3397563657000 because exiting with last active thread context
lkim@lkim-VirtualBox:~/Desktop/gem5$
```

This portion of the assignment required me to understand how the algorithm which is called Shiva veritas the knees Works. After having done so I created a C program that takes a integer and I'll puts the number of prime numbers from zero up to that and put it in a jar, implementing

this portion of my own test application required me to understand the compilation of test applications, and end where it applies in comparison to the program in build.

# Part 3 - Analyze the statistics:

The statistics show a plethora of relevant CPU statistics. And he statistics range from a number of arithmetic logic. Unit axis is whether those are for integers, floats, vectors. I was looking for relevant cash information, but was not able to find any. The closest thing to some resemblance of a cash was a TLB. there were statistics referring to the translation lookaside buffer, those being accesses/ misses on read/write requests.

# Part 4 - Alternative Configurations:

## **Configuration 4.1:**

```
system.clk_domain.clock = '1GHz'
system.cpu = X86O3CPU()
system.mem ctrl.dram = DDR3 1600 8x8()
```

```
build/X86/python/m5/main.py(434): main
lkim@lkim-VirtualBox:~/Desktop/gem5$ build/X8
gem5 Simulator System. https://www.gem5.org
                                     op/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Nov 11 2022 14:52:49
gem5 started Nov 11 2022 16:42:56
gem5 executing on lkim-VirtualBox, pid 11209
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py
Global frequency set at 1000000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the addr
ess range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7002
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/X86/arch/x86/cpuid.cc:180: warn: x86 cpuid family 0x0000: unimplemented function 13
build/X86/arch/x86/cpuid.cc:180: warn: x86 cpuid family 0x0000: unimplemented function 20 build/X86/arch/x86/cpuid.cc:180: warn: x86 cpuid family 0x0000: unimplemented function 25 build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall rseq(...)
build/X86/sim/mem_state.cc:443: info: Increasing stack size by one page.
build/X86/sim/syscall_emul.hh:1015: warn: readlink() called on '/proc/self/exe' may yield unexpected
results in various settings.
        Returning '/home/lkim/Desktop/gem5/configs/tutorial/part1/sieveofe.o'
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
78498
Exiting @ tick 495887903000 because exiting with last active thread context
```

We can expect a lot of changes and we did see many changes as the actual cpu was interchanged with a different processor. We can see that for this configuration the simulation time was MUCH faster. With a time of 0.49 from the last 3.39 seconds. This makes sense as when we pull up the tlb accesses, we can read,

```
system.cpu.mmu.itb.wrMisses
# TLB misses on write requests (Count
```

#### Versus the original

```
system.cpu.mmu.itb.rdAccesses 0
# TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses 47529643
# TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses 0
# TLB misses on read requests (Count)
system.cpu.mmu.itb.wrMisses 56
# TLB misses on write requests (Count)
```

We observe that there is a huge difference is the number of accesses in the itb by almost a magnitude as there were 47.5 million accesses versus the new 6 million access reads. This could result in how the simulation time was also drastically reduced.

# **Configuration 4.2:**

```
system.clk_domain.clock = '3GHz'
system.cpu = TimingSimpleCPU()
system.mem ctrl.dram = DDR3 1600 8x8()
```

```
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
Exiting @ tick 3397563657000 because exiting with last active thread context
lkim@lkim-VirtualBox:~/Desktop/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Nov 11 2022 14:52:49
gem5 started Nov 11 2022 15:57:49
gem5 executing on lkim-VirtualBox, pid 10596
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py
Global frequency set at 100000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the addr
ess range assigned (512 Mbytes)
0: system.remote_gdb: listening for remote gdb on port 7002
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall rseq(...)
build/X86/sim/mem_state.cc:443: info: Increasing stack size by one page.
build/X86/sim/syscall_emul.hh:1015: warn: readlink() called on '/proc/self/exe' may yield unexpected
results in various settings.
      Returning '/home/lkim/Desktop/gem5/configs/tutorial/part1/sieveofe.o'
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
78498
Exiting @ tick 2904978744369 because exiting with last active thread context lkim@lkim-VirtualBox:~/Desktop/gem5$
```

For this configuration, we have a difference in the clock speed that we are using. We were using 1GHz, but now we are using 3GHz.

The change int clock is confirmed in our statistics line that says

```
system.clk_domain.clock
# Clock period in ticks (Tick)
```

And it is shown as the frequency increased by threefold and the period was decreased by threefold by comparison.

The number of tlb accesses/misses on read/write requests stayed the same which is to be expected as there is no change in the processing other than the speed. Intuitively, we can see that the simulation time is faster from 3.39 to 2.90.

# **Configuration 4.3:**

```
system.clk_domain.clock = '1GHz'
system.cpu = TimingSimpleCPU()
system.mem_ctrl.dram = DDR3_2133_8x8()
```

```
build/X86/python/m5/main.py(434): main
lkim@lkim-VirtualBox:~/Desktop/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Nov 11 2022 14:52:49
gem5 started Nov 11 2022 16:33:33
gem5 executing on lkim-VirtualBox, pid 10978
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py
Global frequency set at 100000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the addr
ess range assigned (512 \; 	exttt{Mbytes})
0: system.remote_gdb: listening for remote gdb on port 7002
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall rseq(...)
build/X86/sim/mem_state.cc:443: info: Increasing stack size by one page.
build/X86/sim/syscall_emul.hh:1015: warn: readlink() called on '/proc/self/exe' may yield unexpected
results in various settings.
       Returning '/home/lkim/Desktop/gem5/configs/tutorial/part1/sieveofe.o'
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
78498
Exiting @ tick 3271748533000 because exiting with last active thread context
```

For this configuration, we have a difference in the memory that we are using. We were using DDR3\_1600\_8x8, but now we are using DDR3\_2133\_8x8.

# **Configuration 4.4:**

```
system.clk_domain.clock = '1GHz'
system.cpu = TimingSimpleCPU()
system.mem_ctrl.dram = LPDDR2_S4_1066_1x32()
```

For this configuration, we have a difference in the memory that we are using. We were using DDR3\_1600\_8x8, but now we are using LPDDR2\_S4\_1066\_1x32(). I had to experiment a little bit with the sizing of the memory, but it does make sense that it turned out to be 1x32 as it is a low power memory which means that the bandwidth is likely to be much smaller.

```
configs/tutorial/part1/simple.py(23): <module>
  build/X86/python/m5/main.py(434): main
lkim@lkim-VirtualBox:~/Desktop/gem5$ build/X86/gem5.opt configs/tutorial/part1/simple.py
gem5 Simulator System. https://www.gem5.org
gem5 is copyrighted software; use the --copyright option for details.
gem5 version 22.0.0.2
gem5 compiled Nov 11 2022 14:52:49
gem5 started Nov 11 2022 16:55:02
gem5 executing on lkim-VirtualBox, pid 11378
command line: build/X86/gem5.opt configs/tutorial/part1/simple.py
Global frequency set at 100000000000 ticks per second
warn: No dot file generated. Please install pydot to generate the dot file and pdf.
0: system.remote_gdb: listening for remote gdb on port 7002
Beginning simulation!
build/X86/sim/simulate.cc:194: info: Entering event queue @ 0. Starting simulation...
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall set_robust_list(...)
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall rseq(...)
build/X86/sim/mem_state.cc:443: info: Increasing stack size by one page.
build/X86/sim/syscall_emul.hh:1015: warn: readlink() called on '/proc/self/exe' may yield unexpected
results in various settings.
      Returning '/home/lkim/Desktop/gem5/configs/tutorial/part1/sieveofe.o'
build/X86/sim/syscall_emul.cc:74: warn: ignoring syscall mprotect(...)
78498
Exiting @ tick 3387931467000 because exiting with last active thread context
lkim@lkim-VirtualBox:~/Desktop/gem5$
```

#### sieveofe.c

```
#include <stdio.h>
#include <math.h>
#define MAX 1000000 //1 mil
//#define MAX 100000000 //100 mil
char primes[MAX];
int main(int argc, char *argv[]){
 /* Create an array of values, where '1' indicates that a number is prime.
  * Start by assuming all numbers are prime by setting them to 1.
 */
 for (int i=0; i<MAX; i++) {
       primes[i] = 1;
 }
 /* Loop through a portion of the array (up to the square root of MAX). If
  * it's a prime, ensure all multiples of it are set to zero (false), as they
 * clearly cannot be prime.
 */
 int limit = sqrt(MAX) + 1;
 for (int i=2; i<limit; i++) {
       if (primes[i-1]) {
       for (int j=i*i; j<=MAX; j+=i) {
```

```
primes[j-1] = 0;
}
}

/* Output the results */
int count = 0;
for (int i=2; i<=MAX; i++) {
        if (primes[i-1]) {
        // printf("%d\n", i);
        count++;
        }
}
printf("%i\n",count);
return 0;
}</pre>
```

# Simple.py # this version is for configuration 4.4, but we can assume the parameters are changed for the appropriate configuration

```
import m5
from m5.objects import *
system = System()
system.clk_domain = SrcClockDomain()
system.clk domain.clock = '1GHz'
system.clk domain.voltage domain = VoltageDomain()
system.mem mode = 'timing'
system.mem_ranges = [AddrRange('512MB')]
system.cpu = TimingSimpleCPU()
system.membus = SystemXBar()
system.cpu.icache_port = system.membus.cpu_side_ports
system.cpu.dcache_port = system.membus.cpu_side_ports
system.cpu.createInterruptController()
system.cpu.interrupts[0].pio = system.membus.mem_side_ports
system.cpu.interrupts[0].int requestor = system.membus.cpu side ports
system.cpu.interrupts[0].int_responder = system.membus.mem_side_ports
system.system port = system.membus.cpu side ports
system.mem ctrl = MemCtrl()
system.mem_ctrl.dram = LPDDR2_S4_1066_1x32()
```

```
system.mem ctrl.dram.range = system.mem ranges[0]
system.mem_ctrl.port = system.membus.mem_side_ports
#
binary = 'configs/tutorial/part1/sieveofe.o'
# for gem5 V21 and beyond
system.workload = SEWorkload.init compatible(binary)
process = Process()
process.cmd = [binary]
system.cpu.workload = process
system.cpu.createThreads()
root = Root(full_system = False, system = system)
m5.instantiate()
print("Beginning simulation!")
exit_event = m5.simulate()
print('Exiting @ tick {} because {}'
       .format(m5.curTick(), exit_event.getCause()))
```

# Stats 3

```
----- Begin Simulation Statistics -----
simSeconds
                                            3.397564
# Number of seconds simulated (Second)
                                       3397563657000
simTicks
# Number of ticks simulated (Tick)
finalTick
                                        3397563657000
# Number of ticks from beginning of simulation (restored from checkpoints
and never reset) (Tick)
                                        1000000000000
simFreq
# The number of ticks per simulated second ((Tick/Second))
hostSeconds
                                              173.61
# Real time elapsed on the host (Second)
                                         19570292456
hostTickRate
# The number of ticks simulated per host second (ticks/s) ((Tick/Second))
hostMemory
                                              655500
# Number of bytes of host memory used (Byte)
                                            36199500
# Number of instructions simulated (Count)
```

```
simOps
                                             76555494
# Number of ops (including micro ops) simulated (Count)
hostInstRate
# Simulator instruction rate (inst/s) ((Count/Second))
hostOpRate
                                               440967
# Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk domain.clock
# Clock period in ticks (Tick)
system.clk domain.voltage domain.voltage
                                                    1
# Voltage in Volts (Volt)
                                           3397563657
system.cpu.numCycles
# Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted
                                                     0
# Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted
# Number of work items this cpu completed (Count)
system.cpu.exec context.thread 0.numInsts
                                              36199500
# Number of instructions committed (Count)
system.cpu.exec context.thread 0.numOps
                                             76555494
# Number of ops (including micro ops) committed (Count)
system.cpu.exec context.thread 0.numIntAluAccesses
                                                      76554574
# Number of integer alu accesses (Count)
system.cpu.exec context.thread 0.numFpAluAccesses
                                                           1471
# Number of float alu accesses (Count)
system.cpu.exec context.thread 0.numVecAluAccesses
# Number of vector alu accesses (Count)
system.cpu.exec context.thread 0.numCallsReturns
                                                           373
# Number of times a function call or return occured (Count)
system.cpu.exec context.thread 0.numCondCtrlInsts
# Number of instructions that are conditional controls (Count)
system.cpu.exec context.thread 0.numIntInsts
# Number of integer instructions (Count)
system.cpu.exec context.thread 0.numFpInsts
                                                    1471
# Number of float instructions (Count)
system.cpu.exec context.thread 0.numVecInsts
                                                         0
# Number of vector instructions (Count)
system.cpu.exec context.thread 0.numIntRegReads
# Number of times the integer registers were read (Count)
system.cpu.exec context.thread 0.numIntRegWrites
                                                      58976338
# Number of times the integer registers were written (Count)
system.cpu.exec context.thread 0.numFpRegReads
# Number of times the floating registers were read (Count)
system.cpu.exec context.thread 0.numFpRegWrites
# Number of times the floating registers were written (Count)
system.cpu.exec context.thread 0.numVecRegReads
# Number of times the vector registers were read (Count)
```

```
system.cpu.exec context.thread 0.numVecRegWrites
# Number of times the vector registers were written (Count)
system.cpu.exec context.thread 0.numVecPredRegReads
# Number of times the predicate registers were read (Count)
system.cpu.exec context.thread 0.numVecPredRegWrites
# Number of times the predicate registers were written (Count)
system.cpu.exec context.thread 0.numCCRegReads
# Number of times the CC registers were read (Count)
system.cpu.exec context.thread 0.numCCRegWrites
# Number of times the CC registers were written (Count)
system.cpu.exec context.thread 0.numMiscRegReads
                                                     37276209
# Number of times the Misc registers were read (Count)
system.cpu.exec context.thread 0.numMiscRegWrites
                                                             0
# Number of times the Misc registers were written (Count)
system.cpu.exec context.thread 0.numMemRefs
# Number of memory refs (Count)
system.cpu.exec context.thread 0.numLoadInsts
                                                  15574080
# Number of load instructions (Count)
system.cpu.exec context.thread 0.numStoreInsts
                                                    7325809
# Number of store instructions (Count)
system.cpu.exec context.thread 0.numIdleCycles
                                                   0.001000
# Number of idle cycles (Cycle)
system.cpu.exec context.thread 0.numBusyCycles 3397563656.999000
# Number of busy cycles (Cycle)
system.cpu.exec context.thread 0.notIdleFraction
                                                     1.000000
# Percentage of non-idle cycles (Ratio)
system.cpu.exec context.thread 0.idleFraction
                                                  0.000000
# Percentage of idle cycles (Ratio)
system.cpu.exec context.thread 0.numBranches
                                                  5126544
# Number of branches fetched (Count)
system.cpu.exec context.thread 0.statExecutedInstType::No OpClass
                    0.00% # Class of executed instruction. (Count)
system.cpu.exec_context.thread 0.statExecutedInstType::IntAlu
                                                                  53654589
          70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntMult
         0.00%
                  70.09% # Class of executed instruction. (Count)
177
system.cpu.exec context.thread 0.statExecutedInstType::IntDiv
                                                                        28
         70.09% # Class of executed instruction. (Count)
system.cpu.exec_context.thread 0.statExecutedInstType::FloatAdd
         0.00%
                  70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatCmp
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatCvt
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatMult
                70.09% # Class of executed instruction. (Count)
       0.00%
```

```
system.cpu.exec context.thread 0.statExecutedInstType::FloatMultAcc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatDiv
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMisc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatSqrt
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAdd
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAddAcc
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAlu
                 70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdCmp
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdCvt
                 70.09% # Class of executed instruction. (Count)
        0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdMisc
         0.00%
                  70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMult
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdMultAcc
              70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShift
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShiftAcc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdDiv
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdSqrt
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAdd
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAlu
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCmp
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCvt
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatDiv
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMisc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMult
       0.00% 70.09% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMultAcc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatSqrt
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAdd
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAlu
               70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceCmp
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceAdd
                70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceCmp
              70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAes
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAesMix
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShalHash
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha1Hash2
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash2
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma2
              70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma3
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdPredAlu
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::MemRead
15573939
            20.34%
                       90.43% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::MemWrite
            9.57% 100.00% # Class of executed instruction. (Count)
7325245
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemRead
        0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemWrite
        0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IprAccess
      0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::InstPrefetch
               100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::total 76555515
# Class of executed instruction. (Count)
```

```
system.cpu.interrupts.clk domain.clock
                                                16000
# Clock period in ticks (Tick)
system.cpu.mmu.dtb.rdAccesses
                                             15574084
# TLB accesses on read requests (Count)
system.cpu.mmu.dtb.wrAccesses
                                              7325810
# TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses
                                                   421
# TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses
                                                28844
# TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power state.pwrStateResidencyTicks::UNDEFINED
3397563657000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.mmu.itb.rdAccesses
                                                     0
# TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses
                                             47529643
# TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses
                                                     0
# TLB misses on read requests (Count)
                                                    56
system.cpu.mmu.itb.wrMisses
# TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power state.pwrStateResidencyTicks::UNDEFINED
3397563657000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.power state.pwrStateResidencyTicks::ON 3397563657000
# Cumulative time (in ticks) in various power states (Tick)
system.cpu.thread 0.numInsts
# Number of Instructions committed (Count)
system.cpu.thread 0.numOps
                                                     0
# Number of Ops committed (Count)
system.cpu.thread 0.numMemRefs
                                                     0
# Number of Memory References (Count)
system.cpu.workload.numSyscalls
                                                    17
# Number of system calls (Count)
system.mem ctrl.avgPriority cpu.inst::samples 47529643.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.avgPriority cpu.data::samples
                                                6934363.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.priorityMinLatency
                                         0.00000018750
# per QoS priority minimum request to response latency (Second)
system.mem ctrl.priorityMaxLatency
                                         2.262941650750
# per QoS priority maximum request to response latency (Second)
system.mem ctrl.numReadWriteTurnArounds
# Number of turnarounds from READ to WRITE (Count)
system.mem ctrl.numWriteReadTurnArounds
                                                44356
# Number of turnarounds from WRITE to READ (Count)
```

```
system.mem ctrl.numStayReadState
                                           115662297
# Number of times bus staying in READ state (Count)
system.mem ctrl.numStayWriteState
# Number of times bus staying in WRITE state (Count)
system.mem ctrl.readReqs
                                             63103726
# Number of read requests accepted (Count)
system.mem ctrl.writeReqs
                                              7325807
# Number of write requests accepted (Count)
system.mem ctrl.readBursts
                                             63103726
# Number of controller read bursts, including those serviced by the write
queue (Count)
system.mem ctrl.writeBursts
                                              7325807
# Number of controller write bursts, including those merged in the write
queue (Count)
                                              9349484
system.mem ctrl.servicedByWrQ
# Number of controller read bursts serviced by the write queue (Count)
system.mem ctrl.mergedWrBursts
                                              6616043
# Number of controller write bursts merged with an existing one (Count)
system.mem ctrl.neitherReadNorWriteReqs
                                                    0
# Number of requests that are neither read nor write (Count)
system.mem ctrl.avgRdQLen
# Average read queue length when enqueuing ((Count/Tick))
system.mem ctrl.avgWrQLen
# Average write queue length when enqueuing ((Count/Tick))
system.mem ctrl.numRdRetry
# Number of times read queue was full causing retry (Count)
system.mem ctrl.numWrRetry
# Number of times write queue was full causing retry (Count)
system.mem ctrl.readPktSize::0
                                              1001231
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::1
                                                   19
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::2
                                             14571441
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::3
                                             47531035
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::4
                                                    0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::5
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::6
                                                    0
# Read request sizes (log2) (Count)
system.mem ctrl.writePktSize::0
                                              3122099
# Write request sizes (log2) (Count)
                                                     3
system.mem ctrl.writePktSize::1
# Write request sizes (log2) (Count)
```

```
system.mem ctrl.writePktSize::2
                                              4201939
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::3
                                                 1766
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::4
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::5
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::6
                                                     0
# Write request sizes (log2) (Count)
                                             53754238
system.mem ctrl.rdQLenPdf::0
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::1
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::2
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::3
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::4
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::5
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::6
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::7
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::8
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::9
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::10
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::11
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::12
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::13
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::14
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::15
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::16
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::17
# What read queue length does an incoming req see (Count)
```

```
system.mem ctrl.rdQLenPdf::18
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::19
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::20
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::21
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::22
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::23
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::24
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::25
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::26
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::27
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::28
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::29
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::30
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::31
# What read queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::0
                                                    1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::1
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::2
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::3
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::4
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::5
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::6
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::7
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::8
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::9
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::10
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::11
                                                     1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::12
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::13
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::14
                                                     1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::15
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::16
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::17
                                                44356
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::18
                                                 44357
# What write queue length does an incoming req see (Count)
system.mem_ctrl.wrQLenPdf::19
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::20
                                                44357
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::21
                                                 44357
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::22
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::23
                                                 44357
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::24
                                                 44356
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::25
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::26
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::27
                                                44356
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::28
                                                 44356
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::29
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::30
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::31
                                                 44356
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::32
                                                44356
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::33
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::34
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::35
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::36
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::37
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::38
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::39
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::40
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::41
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::42
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::43
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::44
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::45
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::46
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::47
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::48
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::49
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::50
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::51
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::52
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::53
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::54
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::55
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::56
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::57
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::58
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::59
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::60
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::61
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::62
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::63
# What write queue length does an incoming reg see (Count)
system.mem ctrl.rdPerTurnAround::samples
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::mean
                                         1211.878664
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::gmean 338.313167
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::stdev 86600.937407
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::0-1.04858e+06
                                                      44355
                                                               100.00%
100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07
         100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::total
# Reads before turning the bus around for writes (Count)
system.mem ctrl.wrPerTurnAround::samples
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::mean
                                           16.001037
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::gmean
                                            16.000977
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::stdev
                                             0.045531
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::16
                                                44333
99.95% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::18
                                                   23
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::total
# Writes before turning the bus around for reads (Count)
```

```
system.mem ctrl.bytesReadWrQ
                                            598366976
# Total number of bytes read from write queue (Byte)
system.mem ctrl.bytesReadSys
                                            439535306
# Total read bytes from the system interface side (Byte)
system.mem ctrl.bytesWrittenSys
                                             19943987
# Total written bytes from the system interface side (Byte)
system.mem ctrl.avgRdBWSys
                                         129367791.26843597
# Average system read bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.avgWrBWSys
                                         5870084.86475578
# Average system write bandwidth in Byte/s ((Byte/Second))
                                         3397563531000
system.mem ctrl.totGap
# Total gap between requests (Tick)
                                             48240.61
system.mem ctrl.avgGap
# Average gap between requests ((Tick/Count))
system.mem ctrl.requestorReadBytes::cpu.inst
                                                380237144
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorReadBytes::cpu.data
                                                 21899389
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorWriteBytes::cpu.data
                                                    720805
# Per-requestor bytes write to memory (Byte)
system.mem ctrl.requestorReadRate::cpu.inst 111914648.962234288454
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorReadRate::cpu.data 6445615.508889934048
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorWriteRate::cpu.data 212153.493729227281
# Per-requestor bytes write to memory rate ((Byte/Second))
system.mem ctrl.requestorReadAccesses::cpu.inst
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorReadAccesses::cpu.data
                                                    15574083
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorWriteAccesses::cpu.data
                                                      7325807
# Per-requestor write serviced memory accesses (Count)
system.mem ctrl.requestorReadTotalLat::cpu.inst 1154721525250
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorReadTotalLat::cpu.data 270488760000
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorWriteTotalLat::cpu.data 78277683342750
# Per-requestor write total memory access latency (Tick)
system.mem ctrl.requestorReadAvgLat::cpu.inst
                                                  24294.77
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorReadAvgLat::cpu.data 17367.88
# Per-requestor read average memory access latency ((Tick/Count))
system.mem_ctrl.requestorWriteAvgLat::cpu.data 10685195.96
# Per-requestor write average memory access latency ((Tick/Count))
system.mem ctrl.dram.bytesRead::cpu.inst
                                            380237144
# Number of bytes read from this memory (Byte)
```

```
system.mem ctrl.dram.bytesRead::cpu.data
                                           59298162
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::total
                                            439535306
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::cpu.inst
                                                380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::total
                                             380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesWritten::cpu.data
                                                19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.bytesWritten::total
                                             19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.numReads::cpu.inst
                                             47529643
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::cpu.data
                                             15574083
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::total
                                             63103726
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::cpu.data
                                              7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::total
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.bwRead::cpu.inst
                                           111914649
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::cpu.data
                                             17453142
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::total
                                            129367791
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::cpu.inst 111914649
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::total
                                           111914649
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem_ctrl.dram.bwWrite::cpu.data
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::total
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.inst
                                           111914649
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.data
                                             23323227
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::total
                                           135237876
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.readBursts
                                            53754242
# Number of DRAM read bursts (Count)
system.mem ctrl.dram.writeBursts
                                               709742
# Number of DRAM write bursts (Count)
```

<pre>system.mem_ctrl.dram.perBankRdBursts::0</pre>	52796429
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::1</pre>	58693
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::2</pre>	58164
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::3</pre>	61969
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::4</pre>	66160
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::5</pre>	66349
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::6</pre>	65557
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::7</pre>	66179
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::8</pre>	65688
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::9</pre>	67381
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::10</pre>	66785
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::11</pre>	65843
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::12</pre>	66137
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::13</pre>	62864
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::14</pre>	58980
# Per bank write bursts (Count)	
<pre>system.mem ctrl.dram.perBankRdBursts::15</pre>	61064
# Per bank write bursts (Count)	
<pre>system.mem ctrl.dram.perBankWrBursts::0</pre>	44249
# Per bank write bursts (Count)	
<pre>system.mem ctrl.dram.perBankWrBursts::1</pre>	41967
# Per bank write bursts (Count)	
<pre>system.mem ctrl.dram.perBankWrBursts::2</pre>	41529
# Per bank write bursts (Count)	
<pre>system.mem ctrl.dram.perBankWrBursts::3</pre>	42110
# Per bank write bursts (Count)	
system.mem ctrl.dram.perBankWrBursts::4	44344
# Per bank write bursts (Count)	
system.mem ctrl.dram.perBankWrBursts::5	45114
# Per bank write bursts (Count)	
system.mem ctrl.dram.perBankWrBursts::6	45485
# Per bank write bursts (Count)	
·	

```
system.mem ctrl.dram.perBankWrBursts::7
                                                45865
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::8
                                                46100
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::9
                                                46302
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::10
                                                46512
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::11
                                                46705
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::12
                                                46857
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::13
                                                44923
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::14
                                                40793
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::15
                                                40887
# Per bank write bursts (Count)
system.mem ctrl.dram.totQLat
                                        417318247750
# Total ticks spent queuing (Tick)
system.mem ctrl.dram.totBusLat
                                        268771210000
# Total ticks spent in databus transfers (Tick)
system.mem ctrl.dram.totMemAccLat
                                       1425210285250
# Total ticks spent from burst creation until serviced by the DRAM (Tick)
system.mem ctrl.dram.avgQLat
                                              7763.45
# Average queueing delay per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgBusLat
# Average bus latency per DRAM burst ((Tick/Count))
system.mem_ctrl.dram.avgMemAccLat
                                             26513.45
# Average memory access latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.readRowHits
                                             42118516
# Number of row buffer hits during reads (Count)
system.mem ctrl.dram.writeRowHits
# Number of row buffer hits during writes (Count)
system.mem ctrl.dram.readRowHitRate
                                                78.35
# Row buffer hit rate for reads (Ratio)
system.mem ctrl.dram.writeRowHitRate
                                                91.43
# Row buffer hit rate for writes (Ratio)
system.mem ctrl.dram.bytesPerActivate::samples
                                                   11696565
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::mean
                                              298.009921
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::gmean 169.664060
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::stdev 304.957490
# Bytes accessed per row activation (Byte)
```

```
system.mem ctrl.dram.bytesPerActivate::0-127
                                                  5505879
                                                              47.07%
47.07% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::128-255
                                                    2141340
                                                                18.31%
65.38% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::256-383
                                                     125989
                                                                 1.08%
66.46% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::384-511
                                                     285359
                                                                 2.44%
68.90% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::512-639
                                                     922086
                                                                 7.88%
76.78% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::640-767
                                                    2040896
                                                                17.45%
94.23% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::768-895
                                                      38479
                                                                 0.33%
94.56% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::896-1023
                                                       47645
                                                                  0.41%
94.97% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::1024-1151
                                                       588892
                                                                   5.03%
100.00% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::total
                                                11696565
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesRead
                                           3440271488
# Total bytes read (Byte)
system.mem ctrl.dram.bytesWritten
                                             45423488
# Total bytes written (Byte)
system.mem ctrl.dram.avgRdBW
                                          1012.570134
# Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.avgWrBW
                                            13.369430
# Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.peakBW
                                             12800.00
# Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem ctrl.dram.busUtil
                                                 8.02
# Data bus utilization in percentage (Ratio)
system.mem ctrl.dram.busUtilRead
                                                 7.91
# Data bus utilization in percentage for reads (Ratio)
system.mem ctrl.dram.busUtilWrite
# Data bus utilization in percentage for writes (Ratio)
system.mem ctrl.dram.pageHitRate
                                                78.52
# Row buffer hit rate, read and write combined (Ratio)
system.mem ctrl.dram.power state.pwrStateResidencyTicks::UNDEFINED
3397563657000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.mem ctrl.dram.rank0.actEnergy
                                          82778475360
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preEnergy
                                          43997787900
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.readEnergy
                                        380130030000
# Energy for read commands per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank0.writeEnergy
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.refreshEnergy 268200622560.000031
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actBackEnergy 1480927690350
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preBackEnergy 57567442080
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.totalEnergy
                                        2315432509110
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.averagePower
                                           681.497903
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank0.totalIdleTime
                                                    0
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::IDLE 21716258750
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::REF 113452040000
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT 3262395358250
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT PDN
                                                            0
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.actEnergy
                                            735034440
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.preEnergy
                                            390676275
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.readEnergy
                                           3675257880
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.writeEnergy
                                           1874392380
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.refreshEnergy 268200622560.000031
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.actBackEnergy 295943547990
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.preBackEnergy 1055448825120
# Energy for precharge background per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank1.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.totalEnergy 1626268356645
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.averagePower
                                           478.657215
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank1.totalIdleTime
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::IDLE 2741190158500
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::REF 113452040000
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::PRE PDN
                                                             0
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT 542921458500
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT PDN
                                                             0
# Time in different power states (Tick)
system.mem ctrl.power state.pwrStateResidencyTicks::UNDEFINED
3397563657000
                                    # Cumulative time (in ticks) in
various power states (Tick)
                                             63103710
system.membus.transDist::ReadReq
# Transaction distribution (Count)
system.membus.transDist::ReadResp
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::WriteReq
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::WriteResp
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadReq
                                                    16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadResp
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteReq
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteResp
                                                      16
# Transaction distribution (Count)
system.membus.pktCount system.cpu.icache port::system.mem ctrl.port
95059286
                               # Packet count per connected requestor and
responder (Count)
```

```
system.membus.pktCount system.cpu.icache port::total
# Packet count per connected requestor and responder (Count)
system.membus.pktCount system.cpu.dcache port::system.mem ctrl.port
45799780
                               # Packet count per connected requestor and
responder (Count)
system.membus.pktCount system.cpu.dcache port::total
# Packet count per connected requestor and responder (Count)
system.membus.pktCount::total
                                            140859066
# Packet count per connected requestor and responder (Count)
system.membus.pktSize system.cpu.icache port::system.mem ctrl.port
380237144
                                # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.icache port::total
                                                        380237144
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::system.mem ctrl.port
79242149
                               # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::total
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total
                                            459479293
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops
# Total snoops (Count)
system.membus.snoopTraffic
                                                     0
# Total snoop traffic (Byte)
system.membus.snoopFanout::samples
                                             70429533
# Request fanout histogram (Count)
system.membus.snoopFanout::mean
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::stdev
                                                    0
# Request fanout histogram (Count)
system.membus.snoopFanout::underflows
                                                            0.00%
0.00% # Request famout histogram (Count)
system.membus.snoopFanout::0
                                             70429533
                                                         100.00%
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::1
                                                     0
                                                            0.00%
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::overflows
                                                            0.00%
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::min value
                                                    0
# Request fanout histogram (Count)
system.membus.snoopFanout::max value
# Request fanout histogram (Count)
system.membus.snoopFanout::total
                                             70429533
# Request fanout histogram (Count)
system.membus.power state.pwrStateResidencyTicks::UNDEFINED 3397563657000
# Cumulative time (in ticks) in various power states (Tick)
```

```
system.membus.reqLayer2.occupancy
                                   77755340000
# Layer occupancy (ticks) (Tick)
system.membus.reqLayer2.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.respLayer0.occupancy 109734297750
# Layer occupancy (ticks) (Tick)
system.membus.respLayer0.utilization
                                                 0.0
# Layer utilization (Ratio)
                                    42693685000
system.membus.respLayer1.occupancy
# Layer occupancy (ticks) (Tick)
system.membus.respLayer1.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.snoop filter.totRequests
# Total number of requests made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleRequests
# Number of requests hitting in the snoop filter with a single holder of
the requested data. (Count)
system.membus.snoop filter.hitMultiRequests
# Number of requests hitting in the snoop filter with multiple (>1)
holders of the requested data. (Count)
system.membus.snoop filter.totSnoops
# Total number of snoops made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleSnoops
# Number of snoops hitting in the snoop filter with a single holder of the
requested data. (Count)
system.membus.snoop filter.hitMultiSnoops
# Number of snoops hitting in the snoop filter with multiple (>1) holders
of the requested data. (Count)
system.workload.inst.arm
                                                   0
# number of arm instructions executed (Count)
system.workload.inst.quiesce
# number of quiesce instructions executed (Count)
----- End Simulation Statistics ------
Stats 4.1
----- Begin Simulation Statistics -----
simSeconds
                                            0.495888
# Number of seconds simulated (Second)
simTicks
                                       495887903000
# Number of ticks simulated (Tick)
                                        495887903000
# Number of ticks from beginning of simulation (restored from checkpoints
and never reset) (Tick)
                                        1000000000000
simFreq
# The number of ticks per simulated second ((Tick/Second))
hostSeconds
                                              410.22
# Real time elapsed on the host (Second)
```

```
hostTickRate
                                            1208826443
# The number of ticks simulated per host second (ticks/s) ((Tick/Second))
hostMemory
                                                658572
# Number of bytes of host memory used (Byte)
                                              36199500
simInsts
# Number of instructions simulated (Count)
                                              76555494
simOps
# Number of ops (including micro ops) simulated (Count)
hostInstRate
# Simulator instruction rate (inst/s) ((Count/Second))
hostOpRate
                                                186619
# Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk domain.clock
                                                  1000
# Clock period in ticks (Tick)
system.clk domain.voltage domain.voltage
# Voltage in Volts (Volt)
system.cpu.numCycles
                                             495887904
# Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted
                                                     \cap
# Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted
# Number of work items this cpu completed (Count)
system.cpu.instsAdded
                                              77908802
# Number of instructions added to the IQ (excludes non-spec) (Count)
system.cpu.nonSpecInstsAdded
                                                   100
# Number of non-speculative instructions added to the IQ (Count)
system.cpu.instsIssued
# Number of instructions issued (Count)
system.cpu.squashedInstsIssued
                                                    60
# Number of squashed instructions issued (Count)
system.cpu.squashedInstsExamined
                                               1353402
# Number of squashed instructions iterated over during squash; mainly for
profiling (Count)
system.cpu.squashedOperandsExamined
                                               3637174
# Number of squashed operands that are examined and possibly removed from
graph (Count)
system.cpu.squashedNonSpecRemoved
                                                    52
# Number of squashed non-spec instructions that were removed (Count)
system.cpu.numIssuedDist::samples
                                             302528199
# Number of insts issued each cycle (Count)
system.cpu.numIssuedDist::mean
                                             0.262593
# Number of insts issued each cycle (Count)
system.cpu.numIssuedDist::stdev
                                             0.775607
# Number of insts issued each cycle (Count)
                                                            0.00%
system.cpu.numIssuedDist::underflows
                                                     0
0.00% # Number of insts issued each cycle (Count)
```

system.cpu.numIssuedDist::0 261961260	86.59%
86.59% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::1 17194560	5.68%
92.27% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::2 13725745	4.54%
96.81% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::3 4968416	1.64%
98.45% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::4 3794029	1.25%
99.71% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::5 591194	0.20%
99.90% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::6 292661	0.10%
100.00% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::7 220	0.00%
100.00% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::8 114	0.00%
100.00% # Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::overflows 0	0.00%
100.00% # Number of insts issued each cycle (Count)	
<pre>system.cpu.numIssuedDist::min value 0</pre>	
# Number of insts issued each cycle (Count)	
system.cpu.numIssuedDist::max value 8	
<u> </u>	
# Number of insts issued each cycle (Count)	
# Number of insts issued each cycle (Count) system.cpu.numIssuedDist::total 302528199	
system.cpu.numIssuedDist::total 302528199	
<pre>system.cpu.numIssuedDist::total</pre>	0.00%
<pre>system.cpu.numIssuedDist::total</pre>	0.00%
<pre>system.cpu.numIssuedDist::total</pre>	
<pre>system.cpu.numIssuedDist::total 302528199 # Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntAlu 103</pre>	0.00%
<pre>system.cpu.numIssuedDist::total</pre>	51.50%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	
<pre>system.cpu.numIssuedDist::total</pre>	51.50%
<pre>system.cpu.numIssuedDist::total 302528199 # Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0</pre>	51.50%
# Number of insts issued each cycle (Count)  system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count)	51.50% 0.00%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	51.50%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	51.50% 0.00% 0.00% 0.00%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	51.50% 0.00%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	51.50% 0.00% 0.00% 0.00%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	51.50% 0.00% 0.00% 0.00%
<pre># Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass</pre>	51.50% 0.00% 0.00% 0.00% 0.00%
# Number of insts issued each cycle (Count)  system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::FloatCmp 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::FloatCvt 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::FloatCvt 0 51.50% # attempts to use FU when none available (Count)  system.cpu.statFuBusy::FloatMult 0	51.50% 0.00% 0.00% 0.00%
# Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCmp 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCvt 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0	51.50% 0.00% 0.00% 0.00% 0.00%
# Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCmp 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCvt 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0	51.50% 0.00% 0.00% 0.00% 0.00%
# Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCmp 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCvt 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMultAcc 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMultAcc 0 51.50% # attempts to use FU when none available (Count)	51.50% 0.00% 0.00% 0.00% 0.00% 0.00%
# Number of insts issued each cycle (Count) system.cpu.statFuBusy::No_OpClass 0 0.00% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntAlu 103 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::IntDiv 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatAdd 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCmp 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatCvt 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMult 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMultAcc 0 51.50% # attempts to use FU when none available (Count) system.cpu.statFuBusy::FloatMultAcc 0 51.50% # attempts to use FU when none available (Count)	51.50% 0.00% 0.00% 0.00% 0.00%

system.cpu.statFuBusy::FloatMisc	0	0.00%
51.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::FloatSqrt	0	0.00%
51.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdAdd	0	0.00%
51.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdAddAcc	0	0.00%
51.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdAlu	8	4.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdCmp	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdCvt	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdMisc	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdMult	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdMultAcc	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdShift	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdShiftAcc	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdDiv	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdSqrt</pre>	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdFloatAdd</pre>	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdFloatAlu</pre>	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdFloatCmp</pre>	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdFloatCvt</pre>	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdFloatDiv	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdFloatMisc</pre>	0	0.00%
55.50% # attempts to use FU when none available		
system.cpu.statFuBusy::SimdFloatMult	0	0.00%
55.50% # attempts to use FU when none available		
system.cpu.statFuBusy::SimdFloatMultAcc	0	0.00%
55.50% # attempts to use FU when none available		
system.cpu.statFuBusy::SimdFloatSqrt	0	0.00%
55.50% # attempts to use FU when none available	(Count)	

system.cpu.statFuBusy::SimdReduceAdd	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdReduceAlu	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdReduceCmp	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdFloatReduceAdd	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdFloatReduceCmp	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdAes	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::SimdAesMix</pre>	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdShalHash	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdSha1Hash2	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdSha256Hash	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdSha256Hash2	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdShaSigma2	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdShaSigma3	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::SimdPredAlu	0	0.00%
55.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::MemRead	36	18.00%
73.50% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::MemWrite</pre>	12	6.00%
79.50% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::FloatMemRead	27	13.50%
93.00% # attempts to use FU when none available	(Count)	
<pre>system.cpu.statFuBusy::FloatMemWrite</pre>	14	7.00%
100.00% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::IprAccess	0	0.00%
100.00% # attempts to use FU when none available	(Count)	
system.cpu.statFuBusy::InstPrefetch	0	0.00%
100.00% # attempts to use FU when none available		
system.cpu.statIssuedInstType_0::No_OpClass	486	0.00%
0.00% # Number of instructions issued per FU typ		
	244857	68.28%
68.28% # Number of instructions issued per FU ty		
system.cpu.statIssuedInstType_0::IntMult	203	0.00%
68.28% # Number of instructions issued per FU ty	pe, per th	read (Count)

```
system.cpu.statIssuedInstType 0::IntDiv
                                                28
                                                        0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatAdd
                                               211
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatCmp
                                                 0
                                                         0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatCvt
                                         0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatMult
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatMultAcc
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatDiv
                                                 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatMisc 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatSqrt 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdAdd
                                                8
                                                        0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdAddAcc 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdAlu
                                         142
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdCmp
                                                 0
                                                        0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdCvt
                                               54
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdMisc
                                                256
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdMult
                                                 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdMultAcc 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdShift 0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdShiftAcc
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdDiv
                                                 0
                                                        0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdSqrt
                                                0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatAdd
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatAlu
68.28% # Number of instructions issued per FU type, per thread (Count)
```

```
system.cpu.statIssuedInstType 0::SimdFloatCmp
                                                               0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatCvt
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatDiv
                                                               0.00%
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatMisc
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatMult
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatMultAcc
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatSqrt
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdReduceAdd
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdReduceAlu
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdReduceCmp
                                                         0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdFloatReduceAdd
         68.28% # Number of instructions issued per FU type, per thread
0.00%
system.cpu.statIssuedInstType 0::SimdFloatReduceCmp
0.00%
         68.28% # Number of instructions issued per FU type, per thread
system.cpu.statIssuedInstType 0::SimdAes
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdAesMix
                                                      0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdSha1Hash
                                                        0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdShalHash2
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdSha256Hash
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdSha256Hash2
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdShaSigma2
                                                         0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdShaSigma3
                                                         0
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::SimdPredAlu
68.28% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::MemRead
                                            17868533
90.78% # Number of instructions issued per FU type, per thread (Count)
```

```
system.cpu.statIssuedInstType 0::MemWrite 7325835
100.00% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatMemRead
                                                       531
100.00% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::FloatMemWrite
                                                        658
100.00% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::IprAccess
                                                      0
100.00% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::InstPrefetch
                                                         \cap
100.00% # Number of instructions issued per FU type, per thread (Count)
system.cpu.statIssuedInstType 0::total
                                             79441802
# Number of instructions issued per FU type, per thread (Count)
system.cpu.issueRate
                                             0.160201
# Inst issue rate ((Count/Cycle))
system.cpu.fuBusy
                                                  200
# FU busy when requested (Count)
system.cpu.fuBusyRate
                                             0.00003
# FU busy rate (busy events/executed inst) ((Count/Count))
system.cpu.intInstQueueReads
                                            461407937
# Number of integer instruction queue reads (Count)
system.cpu.intInstQueueWrites
# Number of integer instruction queue writes (Count)
system.cpu.intInstQueueWakeupAccesses
                                            77145937
# Number of integer instruction queue wakeup accesses (Count)
system.cpu.fpInstQueueReads
                                                 4126
# Number of floating instruction queue reads (Count)
system.cpu.fpInstQueueWrites
# Number of floating instruction queue writes (Count)
system.cpu.fpInstQueueWakeupAccesses
                                                 1635
# Number of floating instruction queue wakeup accesses (Count)
system.cpu.vecInstQueueReads
# Number of vector instruction queue reads (Count)
system.cpu.vecInstQueueWrites
# Number of vector instruction queue writes (Count)
system.cpu.vecInstQueueWakeupAccesses
# Number of vector instruction queue wakeup accesses (Count)
system.cpu.intAluAccesses
                                             79439434
# Number of integer alu accesses (Count)
                                                 2082
system.cpu.fpAluAccesses
# Number of floating point alu accesses (Count)
system.cpu.vecAluAccesses
                                                    0
# Number of vector alu accesses (Count)
system.cpu.numInsts
                                             79441607
# Number of executed instructions (Count)
system.cpu.numLoadInsts
                                             17868994
# Number of load instructions executed (Count)
```

```
system.cpu.numSquashedInsts
                                                   195
# Number of squashed instructions skipped in execute (Count)
system.cpu.numSwp
# Number of swp insts executed (Count)
system.cpu.numNop
# Number of nop insts executed (Count)
system.cpu.numRefs
                                              25195469
# Number of memory reference insts executed (Count)
system.cpu.numBranches
                                               5127301
# Number of branches executed (Count)
system.cpu.numStoreInsts
                                               7326475
# Number of stores executed (Count)
system.cpu.numRate
                                              0.160201
# Inst execution rate ((Count/Cycle))
system.cpu.timesIdled
                                              14975769
# Number of times that the entire CPU went into an idle state and
unscheduled itself (Count)
system.cpu.idleCycles
                                             193359705
# Total number of cycles that the CPU has spent unscheduled due to idling
(Cycle)
system.cpu.committedInsts
                                              36199500
# Number of Instructions Simulated (Count)
system.cpu.committedOps
                                              76555494
# Number of Ops (including micro ops) Simulated (Count)
system.cpu.cpi
                                             13.698750
# CPI: Cycles Per Instruction ((Cycle/Count))
system.cpu.totalCpi
                                             13.698750
# CPI: Total CPI of All Threads ((Cycle/Count))
system.cpu.ipc
                                              0.072999
# IPC: Instructions Per Cycle ((Count/Cycle))
system.cpu.totalIpc
                                              0.072999
# IPC: Total IPC of All Threads ((Count/Cycle))
system.cpu.intRegfileReads
                                              89555031
# Number of integer regfile reads (Count)
system.cpu.intRegfileWrites
                                              59566193
# Number of integer regfile writes (Count)
system.cpu.fpRegfileReads
                                                  1776
# Number of floating regfile reads (Count)
system.cpu.fpRegfileWrites
                                                   940
# Number of floating regfile writes (Count)
system.cpu.ccRegfileReads
                                              26635654
# number of cc regfile reads (Count)
system.cpu.ccRegfileWrites
                                              24907543
# number of cc regfile writes (Count)
system.cpu.miscRegfileReads
                                              39739173
# number of misc regfile reads (Count)
```

```
system.cpu.MemDepUnit 0.insertedLoads
                                             15828722
# Number of loads inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 0.insertedStores
                                              7414545
# Number of stores inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 0.conflictingLoads
# Number of conflicting loads. (Count)
system.cpu.MemDepUnit 0.conflictingStores
                                                 162186
# Number of conflicting stores. (Count)
system.cpu.MemDepUnit 1.insertedLoads
# Number of loads inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 1.insertedStores
# Number of stores inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 1.conflictingLoads
# Number of conflicting loads. (Count)
system.cpu.MemDepUnit 1.conflictingStores
# Number of conflicting stores. (Count)
system.cpu.MemDepUnit 2.insertedLoads
# Number of loads inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 2.insertedStores
# Number of stores inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 2.conflictingLoads
# Number of conflicting loads. (Count)
system.cpu.MemDepUnit 2.conflictingStores
# Number of conflicting stores. (Count)
system.cpu.MemDepUnit 3.insertedLoads
# Number of loads inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 3.insertedStores
# Number of stores inserted to the mem dependence unit. (Count)
system.cpu.MemDepUnit 3.conflictingLoads
# Number of conflicting loads. (Count)
system.cpu.MemDepUnit 3.conflictingStores
                                                      0
# Number of conflicting stores. (Count)
system.cpu.branchPred.lookups
                                              5210998
# Number of BP lookups (Count)
system.cpu.branchPred.condPredicted
                                              5209752
# Number of conditional branches predicted (Count)
system.cpu.branchPred.condIncorrect
                                                83692
# Number of conditional branches incorrect (Count)
system.cpu.branchPred.BTBLookups
                                              5202788
# Number of BTB lookups (Count)
system.cpu.branchPred.BTBHits
                                              5201923
# Number of BTB hits (Count)
system.cpu.branchPred.BTBHitRatio
                                             0.999834
# BTB Hit Ratio (Ratio)
system.cpu.branchPred.RASUsed
                                                  304
# Number of times the RAS was used to get a target. (Count)
```

```
system.cpu.branchPred.RASIncorrect
                                                     0
# Number of incorrect RAS predictions. (Count)
system.cpu.branchPred.indirectLookups
                                                   201
# Number of indirect predictor lookups. (Count)
system.cpu.branchPred.indirectHits
                                                    20
# Number of indirect target hits. (Count)
system.cpu.branchPred.indirectMisses
                                                   181
# Number of indirect misses. (Count)
                                                      96
system.cpu.branchPred.indirectMispredicted
# Number of mispredicted indirect branches. (Count)
system.cpu.commit.commitSquashedInsts
# The number of squashed insts skipped by commit (Count)
system.cpu.commit.commitNonSpecStalls
# The number of times commit has been forced to stall to communicate
backwards (Count)
system.cpu.commit.branchMispredicts
                                                 83424
# The number of times a branch was mispredicted (Count)
system.cpu.commit.numCommittedDist::samples
                                                302355604
# Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::mean
                                              0.253197
# Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::stdev
                                               0.930143
# Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::underflows
                                                           \cap
                                                                  0.00%
0.00% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::0
                                                           88.59%
88.59% # Number of insts committed each cycle (Count)
                                                            5.48%
system.cpu.commit.numCommittedDist::1
                                              16579102
94.07% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::2
                                                            2.87%
                                               8666013
96.94% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::3
                                                            1.64%
98.58% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::4
                                                667693
                                                            0.22%
98.80% # Number of insts committed each cycle (Count)
                                                   360
system.cpu.commit.numCommittedDist::5
                                                            0.00%
98.80% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::6
                                                            0.14%
98.94% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::7
                                               3042593
                                                            1.01%
99.95% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::8
                                                160996
                                                            0.05%
100.00% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::overflows
                                                                 0.00%
100.00% # Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::min value
                                                          0
# Number of insts committed each cycle (Count)
```

```
system.cpu.commit.numCommittedDist::max value
# Number of insts committed each cycle (Count)
system.cpu.commit.numCommittedDist::total
                                              302355604
# Number of insts committed each cycle (Count)
system.cpu.commit.instsCommitted
                                              36199500
# Number of instructions committed (Count)
system.cpu.commit.opsCommitted
                                              76555494
# Number of ops (including micro ops) committed (Count)
system.cpu.commit.memRefs
                                              22899885
# Number of memory references committed (Count)
system.cpu.commit.loads
                                              15574079
# Number of loads committed (Count)
system.cpu.commit.amos
                                                     0
# Number of atomic instructions committed (Count)
system.cpu.commit.membars
                                                    32
# Number of memory barriers committed (Count)
system.cpu.commit.branches
                                               5126544
# Number of branches committed (Count)
system.cpu.commit.vectorInstructions
                                                     \cap
# Number of committed Vector instructions. (Count)
system.cpu.commit.floating
# Number of committed floating point instructions. (Count)
system.cpu.commit.integer
                                              76554570
# Number of committed integer instructions. (Count)
system.cpu.commit.functionCalls
                                                   189
# Number of function calls committed. (Count)
system.cpu.commit.committedInstType 0::No OpClass
                                                            236
                                                                     0.00%
0.00% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::IntAlu
                                                   53654572
                                                                70.09%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::IntMult
                                                         177
                                                                  0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::IntDiv
                                                         28
                                                                 0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::FloatAdd
                                                          184
                                                                   0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::FloatCmp
                                                                   0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::FloatCvt
                                                                   0.00%
70.09% # Class of committed instruction (Count)
                                                                    0.00%
system.cpu.commit.committedInstType 0::FloatMult
                                                             0
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::FloatMultAcc
                                                                0
         70.09% # Class of committed instruction (Count)
                                                                   0.00%
system.cpu.commit.committedInstType 0::FloatDiv
                                                            ()
70.09% # Class of committed instruction (Count)
```

```
system.cpu.commit.committedInstType 0::FloatMisc
                                                                    0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::FloatSqrt
                                                             0
                                                                    0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdAdd
                                                           8
                                                                  0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdAddAcc
                                                              0
                                                                     0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdAlu
                                                          98
                                                                  0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdCmp
                                                                  0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdCvt
                                                          54
                                                                  0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdMisc
                                                          252
                                                                   0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdMult
                                                            0
                                                                   0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdMultAcc
                                                               0
                                                                      0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdShift
                                                             0
                                                                    0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdShiftAcc
         70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdDiv
                                                           0
                                                                  0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdSqrt
                                                            0
                                                                   0.00%
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatAdd
                                                                0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatAlu
                                                                0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatCmp
                                                                0
         70.09% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::SimdFloatCvt
                                                                0
          70.09% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::SimdFloatDiv
                                                                0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatMisc
                                                                 0
0.00%
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatMult
                                                                 0
          70.09% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::SimdFloatMultAcc
                                                                    0
         70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatSqrt
                                                                 0
         70.09% # Class of committed instruction (Count)
0.00%
```

```
system.cpu.commit.committedInstType 0::SimdReduceAdd
                                                                 0
          70.09% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::SimdReduceAlu
                                                                 0
         70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdReduceCmp
                                                                 0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdFloatReduceAdd
                                                                      0
          70.09% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::SimdFloatReduceCmp
                                                                      0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdAes
                                                                  0.00%
70.09% # Class of committed instruction (Count)
                                                              0
                                                                     0.00%
system.cpu.commit.committedInstType 0::SimdAesMix
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdShalHash
                                                                0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdShalHash2
                                                                 0
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdSha256Hash
                                                                  0
0.00%
          70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdSha256Hash2
                                                                   0
          70.09% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::SimdShaSigma2
                                                                 0
         70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::SimdShaSigma3
                                                                 0
          70.09% # Class of committed instruction (Count)
                                                                      0.00%
system.cpu.commit.committedInstType 0::SimdPredAlu
70.09% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::MemRead
                                                   15573938
                                                                 20.34%
90.43% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::MemWrite
                                                     7325243
                                                                   9.57%
100.00% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::FloatMemRead
                                                              141
         100.00% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::FloatMemWrite
                                                               563
         100.00% # Class of committed instruction (Count)
0.00%
system.cpu.commit.committedInstType 0::IprAccess
                                                             0
                                                                    0.00%
100.00% # Class of committed instruction (Count)
                                                                0
system.cpu.commit.committedInstType 0::InstPrefetch
0.00%
         100.00% # Class of committed instruction (Count)
system.cpu.commit.committedInstType 0::total
                                                 76555494
# Class of committed instruction (Count)
system.cpu.commit.commitEliqibleSamples
# number cycles where commit BW limit reached (Cycle)
system.cpu.decode.idleCycles
                                            250395229
# Number of cycles decode is idle (Cycle)
```

```
system.cpu.decode.blockedCycles
                                             39425743
# Number of cycles decode is blocked (Cycle)
system.cpu.decode.runCycles
                                             10623535
# Number of cycles decode is running (Cycle)
system.cpu.decode.unblockCycles
                                              2000145
# Number of cycles decode is unblocking (Cycle)
system.cpu.decode.squashCycles
                                                83547
# Number of cycles decode is squashing (Cycle)
system.cpu.decode.branchResolved
                                              5202158
# Number of times decode resolved a branch (Count)
system.cpu.decode.branchMispred
                                                  288
# Number of times decode detected a branch misprediction (Count)
system.cpu.decode.decodedInsts
                                             77909374
# Number of instructions handled by decode (Count)
system.cpu.decode.squashedInsts
# Number of squashed instructions handled by decode (Count)
system.cpu.fetch.icacheStallCycles
                                            249817678
# Number of cycles fetch is stalled on an Icache miss (Cycle)
system.cpu.fetch.insts
                                             36790390
# Number of instructions fetch has processed (Count)
system.cpu.fetch.branches
# Number of branches that fetch encountered (Count)
system.cpu.fetch.predictedBranches
                                              5202247
# Number of branches that fetch has predicted taken (Count)
system.cpu.fetch.cycles
                                             52626470
# Number of cycles fetch has run and was not squashing or blocked (Cycle)
system.cpu.fetch.squashCycles
                                               167670
# Number of cycles fetch has spent squashing (Cycle)
system.cpu.fetch.miscStallCycles
                                                   48
# Number of cycles fetch has spent waiting on interrupts, or bad
addresses, or out of MSHRs (Cycle)
system.cpu.fetch.pendingTrapStallCycles
# Number of stall cycles due to pending traps (Cycle)
system.cpu.fetch.icacheWaitRetryStallCycles
# Number of stall cycles due to full MSHR (Cycle)
system.cpu.fetch.cacheLines
                                              6497296
# Number of cache lines fetched (Count)
system.cpu.fetch.icacheSquashes
                                                83630
# Number of outstanding Icache misses that were squashed (Count)
system.cpu.fetch.nisnDist::samples
                                            302528199
# Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::mean
                                             0.257537
# Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::stdev
                                             1.293057
# Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::underflows
                                                    0
                                                           0.00%
0.00% # Number of instructions fetched each cycle (Total) (Count)
```

```
system.cpu.fetch.nisnDist::0
                                            289904405
                                                           95.83%
95.83% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::1
                                                  265
                                                            0.00%
95.83% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::2
                                              1000352
                                                            0.33%
96.16% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::3
                                                  308
                                                            0.00%
96.16% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::4
                                              2129756
96.86% # Number of instructions fetched each cycle (Total) (Count)
                                                   304
system.cpu.fetch.nisnDist::5
                                                            0.00%
96.86% # Number of instructions fetched each cycle (Total) (Count)
                                              4276129
system.cpu.fetch.nisnDist::6
98.28% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::7
                                                   329
                                                            0.00%
98.28% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::8
                                              5216351
                                                           1.72%
100.00% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::overflows
                                                            0.00%
                                                    0
100.00% # Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::min value
# Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::max value
# Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.nisnDist::total
                                            302528199
# Number of instructions fetched each cycle (Total) (Count)
system.cpu.fetch.branchRate
                                             0.010508
# Number of branch fetches per cycle (Ratio)
system.cpu.fetch.rate
                                             0.074191
# Number of inst fetches per cycle ((Count/Cycle))
system.cpu.iew.idleCycles
                                                    0
# Number of cycles IEW is idle (Cycle)
system.cpu.iew.squashCycles
                                                83547
# Number of cycles IEW is squashing (Cycle)
system.cpu.iew.blockCycles
                                                89475
# Number of cycles IEW is blocking (Cycle)
system.cpu.iew.unblockCycles
                                             15000856
# Number of cycles IEW is unblocking (Cycle)
system.cpu.iew.dispatchedInsts
                                             77908902
# Number of instructions dispatched to IQ (Count)
system.cpu.iew.dispSquashedInsts
# Number of squashed instructions skipped by dispatch (Count)
system.cpu.iew.dispLoadInsts
                                             15828722
# Number of dispatched load instructions (Count)
system.cpu.iew.dispStoreInsts
                                              7414545
# Number of dispatched store instructions (Count)
```

```
system.cpu.iew.dispNonSpecInsts
                                                   34
# Number of dispatched non-speculative instructions (Count)
system.cpu.iew.iqFullEvents
# Number of times the IQ has become full, causing a stall (Count)
system.cpu.iew.lsqFullEvents
                                             15000838
# Number of times the LSQ has become full, causing a stall (Count)
system.cpu.iew.memOrderViolationEvents
# Number of memory order violations (Count)
system.cpu.iew.predictedTakenIncorrect
                                                77796
# Number of branches that were predicted taken incorrectly (Count)
system.cpu.iew.predictedNotTakenIncorrect
# Number of branches that were predicted not taken incorrectly (Count)
system.cpu.iew.branchMispredicts
                                                83473
# Number of branch mispredicts detected at execute (Count)
system.cpu.iew.instsToCommit
                                             77147723
# Cumulative count of insts sent to commit (Count)
system.cpu.iew.writebackCount
                                             77147572
# Cumulative count of insts written-back (Count)
system.cpu.iew.producerInst
                                             54442198
# Number of instructions producing a value (Count)
system.cpu.iew.consumerInst
# Number of instructions consuming a value (Count)
system.cpu.iew.wbRate
                                             0.155575
# Insts written-back per cycle ((Count/Cycle))
system.cpu.iew.wbFanout
                                             0.892612
# Average fanout of values written-back ((Count/Count))
system.cpu.interrupts.clk domain.clock
# Clock period in ticks (Tick)
system.cpu.lsq0.forwLoads
                                              9324850
# Number of loads that had data forwarded from stores (Count)
system.cpu.lsq0.squashedLoads
                                               254643
# Number of loads squashed (Count)
system.cpu.lsq0.ignoredResponses
                                                    0
# Number of memory responses ignored because the instruction is squashed
(Count)
system.cpu.lsq0.memOrderViolation
                                                  103
# Number of memory ordering violations (Count)
system.cpu.lsq0.squashedStores
                                                88739
# Number of stores squashed (Count)
system.cpu.lsq0.rescheduledLoads
                                                     0
# Number of loads that were rescheduled (Count)
system.cpu.lsq0.blockedByCache
                                              2209889
# Number of times an access to memory failed due to the cache being
blocked (Count)
system.cpu.lsq0.loadToUse::samples
                                             15574079
# Distribution of cycle latency between the first time a load is issued
and its completion (Unspecified)
```

```
system.cpu.lsq0.loadToUse::mean
                                            25.365366
# Distribution of cycle latency between the first time a load is issued
and its completion (Unspecified)
system.cpu.lsq0.loadToUse::stdev
                                            37.482952
# Distribution of cycle latency between the first time a load is issued
and its completion (Unspecified)
system.cpu.lsq0.loadToUse::0-9
                                              9324215
                                                           59.87%
59.87% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::20-29
                                              2122035
73.50% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::50-59
                                               871472
                                                            5.60%
79.09% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::60-69
                                                 60999
79.48% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::70-79
                                                  225
                                                            0.00%
79.48% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::80-89
                                              3010038
                                                          19.33%
98.81% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::90-99
                                                82165
                                                            0.53%
99.34% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::100-109
                                                  390
                                                            0.00%
99.34% \# Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::110-119
                                                    8
                                                            0.00%
99.34% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::120-129
                                                  345
                                                            0.00%
99.34% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::130-139
                                                47522
                                                            0.31%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::140-149
                                                   36
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::150-159
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
```

```
system.cpu.lsq0.loadToUse::170-179
                                                    1
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::180-189
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::190-199
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::220-229
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
                                                   34
                                                            0.00%
system.cpu.lsq0.loadToUse::230-239
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::240-249
                                                  106
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::250-259
                                                  528
                                                            0.00%
99.65% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::260-269
                                                  458
                                                            0.00%
99.66% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::270-279
                                                  656
                                                            0.00%
99.66% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::280-289
                                                  805
                                                            0.01%
99.67% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::290-299
                                                  657
                                                            0.00%
99.67% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::overflows
                                                51370
                                                            0.33%
100.00% # Distribution of cycle latency between the first time a load is
issued and its completion (Unspecified)
system.cpu.lsq0.loadToUse::min value
# Distribution of cycle latency between the first time a load is issued
and its completion (Unspecified)
system.cpu.lsq0.loadToUse::max value
                                                  451
# Distribution of cycle latency between the first time a load is issued
and its completion (Unspecified)
system.cpu.lsq0.loadToUse::total
                                             15574079
# Distribution of cycle latency between the first time a load is issued
and its completion (Unspecified)
system.cpu.mmu.dtb.rdAccesses
                                             15658795
# TLB accesses on read requests (Count)
```

```
7326476
system.cpu.mmu.dtb.wrAccesses
# TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses
                                                   470
# TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses
                                                28850
# TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power state.pwrStateResidencyTicks::UNDEFINED
495887903000
                                   # Cumulative time (in ticks) in various
power states (Tick)
system.cpu.mmu.itb.rdAccesses
# TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses
                                              6497328
# TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses
                                                     0
# TLB misses on read requests (Count)
system.cpu.mmu.itb.wrMisses
                                                    93
# TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power state.pwrStateResidencyTicks::UNDEFINED
495887903000
                                   # Cumulative time (in ticks) in various
power states (Tick)
system.cpu.power state.pwrStateResidencyTicks::ON 495887903000
# Cumulative time (in ticks) in various power states (Tick)
system.cpu.rename.squashCycles
                                                83547
# Number of cycles rename is squashing (Cycle)
system.cpu.rename.idleCycles
                                            251062187
# Number of cycles rename is idle (Cycle)
system.cpu.rename.blockCycles
                                             15090358
# Number of cycles rename is blocking (Cycle)
system.cpu.rename.serializeStallCycles
                                                  246
# count of cycles rename stalled for serializing inst (Cycle)
system.cpu.rename.runCycles
                                             11956695
# Number of cycles rename is running (Cycle)
system.cpu.rename.unblockCycles
                                             24335166
# Number of cycles rename is unblocking (Cycle)
                                             77909147
system.cpu.rename.renamedInsts
# Number of instructions processed by rename (Count)
system.cpu.rename.ROBFullEvents
# Number of times rename has blocked due to ROB full (Count)
system.cpu.rename.IQFullEvents
                                                   236
# Number of times rename has blocked due to IQ full (Count)
                                             23668230
system.cpu.rename.SQFullEvents
# Number of times rename has blocked due to SQ full (Count)
system.cpu.rename.renamedOperands
                                            128819633
# Number of destination operands rename has renamed (Count)
system.cpu.rename.lookups
                                            240155080
# Number of register rename lookups that rename has made (Count)
```

```
system.cpu.rename.intLookups
                                             88369006
# Number of integer rename lookups (Count)
system.cpu.rename.fpLookups
                                                 1933
# Number of floating rename lookups (Count)
system.cpu.rename.committedMaps
                                            126364676
# Number of HB maps that are committed (Count)
system.cpu.rename.undoneMaps
                                              2454948
# Number of HB maps that are undone due to squashing (Count)
system.cpu.rename.serializing
# count of serializing insts renamed (Count)
system.cpu.rename.tempSerializing
# count of temporary serializing insts renamed (Count)
system.cpu.rename.skidInsts
                                             12000898
# count of insts added to the skid buffer (Count)
system.cpu.rob.reads
                                            380103226
# The number of ROB reads (Count)
system.cpu.rob.writes
                                            155990359
# The number of ROB writes (Count)
system.cpu.thread 0.numInsts
                                             36199500
# Number of Instructions committed (Count)
system.cpu.thread 0.numOps
                                             76555494
# Number of Ops committed (Count)
system.cpu.thread 0.numMemRefs
                                                    0
# Number of Memory References (Count)
system.cpu.workload.numSyscalls
                                                   17
# Number of system calls (Count)
system.mem ctrl.avgPriority cpu.inst::samples 6497296.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.avgPriority cpu.data::samples 4961408.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.priorityMinLatency
                                        0.00000018750
# per QoS priority minimum request to response latency (Second)
system.mem ctrl.priorityMaxLatency 0.311197507750
# per QoS priority maximum request to response latency (Second)
system.mem ctrl.numReadWriteTurnArounds
# Number of turnarounds from READ to WRITE (Count)
system.mem ctrl.numWriteReadTurnArounds
                                                46736
# Number of turnarounds from WRITE to READ (Count)
system.mem ctrl.numStayReadState
                                             26451082
# Number of times bus staying in READ state (Count)
system.mem ctrl.numStayWriteState
# Number of times bus staying in WRITE state (Count)
system.mem ctrl.readReqs
                                             12831113
# Number of read requests accepted (Count)
system.mem ctrl.writeReqs
                                              7325807
# Number of write requests accepted (Count)
```

```
system.mem ctrl.readBursts
                                             12831113
# Number of controller read bursts, including those serviced by the write
queue (Count)
system.mem ctrl.writeBursts
                                              7325807
# Number of controller write bursts, including those merged in the write
queue (Count)
system.mem ctrl.servicedByWrQ
                                              2122189
# Number of controller read bursts serviced by the write queue (Count)
system.mem ctrl.mergedWrBursts
                                              6576027
# Number of controller write bursts merged with an existing one (Count)
system.mem ctrl.neitherReadNorWriteReqs
# Number of requests that are neither read nor write (Count)
system.mem ctrl.avgRdQLen
# Average read queue length when enqueuing ((Count/Tick))
system.mem ctrl.avgWrQLen
# Average write queue length when enqueuing ((Count/Tick))
system.mem ctrl.numRdRetry
# Number of times read queue was full causing retry (Count)
system.mem ctrl.numWrRetry
# Number of times write queue was full causing retry (Count)
system.mem ctrl.readPktSize::0
                                              1001314
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::1
                                                   24
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::2
                                              5330404
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::3
                                                 2075
# Read request sizes (log2) (Count)
system.mem_ctrl.readPktSize::4
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::5
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::6
                                              6497296
# Read request sizes (log2) (Count)
system.mem ctrl.writePktSize::0
                                              3122099
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::1
                                                     3
# Write request sizes (log2) (Count)
                                              4201939
system.mem ctrl.writePktSize::2
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::3
                                                 1766
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::4
                                                     0
# Write request sizes (log2) (Count)
                                                     0
system.mem ctrl.writePktSize::5
# Write request sizes (log2) (Count)
```

```
system.mem ctrl.writePktSize::6
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.rdQLenPdf::0
                                              3203060
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::1
                                               6518010
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::2
                                               986402
# What read queue length does an incoming reg see (Count)
system.mem_ctrl.rdQLenPdf::3
                                                   734
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::4
                                                   278
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::5
                                                   155
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::6
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::7
                                                    67
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::8
                                                    33
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::9
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::10
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::11
                                                    20
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::12
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::13
                                                     Δ
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::14
                                                     3
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::15
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::16
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::17
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::18
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::19
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::20
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::21
                                                     0
# What read queue length does an incoming req see (Count)
```

```
system.mem ctrl.rdQLenPdf::22
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::23
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::24
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::25
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::26
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::27
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::28
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::29
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::30
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::31
# What read queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::0
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::2
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::3
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::4
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::5
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::6
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::7
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::8
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::9
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::10
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::11
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::12
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::13
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::14
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::15
                                                   909
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::16
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::17
                                                20035
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::18
                                                 60717
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::19
                                                 47383
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::20
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::21
                                                47357
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::22
                                                 47372
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::23
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::24
                                                47293
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::25
                                                 47301
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::26
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::27
                                                 47387
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::28
                                                 52355
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::29
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::30
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::31
                                                 46771
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::32
                                                 46749
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::33
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::34
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::35
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::36
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::37
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::38
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::39
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::40
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::41
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::42
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::43
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::44
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::45
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::46
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::47
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::48
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::49
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::50
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::51
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::52
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::53
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::54
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::55
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::56
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::57
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::58
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::59
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::60
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::61
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::62
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::63
# What write queue length does an incoming req see (Count)
system.mem ctrl.rdPerTurnAround::samples
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::mean
                                          229.130863
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::stdev 20030.720262
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::0-262143
                                                 46735
                                                          100.00%
100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::4.1943e+06-4.45645e+06
0.00%
         100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::total
# Reads before turning the bus around for writes (Count)
system.mem ctrl.wrPerTurnAround::samples
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::mean
                                           16.042237
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::gmean
                                           16.039588
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::stdev
                                             0.304617
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::16
                                                45827
98.06% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::17
                                                    1
98.06% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::18
                                                  752
99.67% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::19
                                                  155
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::20
                                                    1
                                                           0.00%
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::total
# Writes before turning the bus around for reads (Count)
system.mem ctrl.bytesReadWrQ
# Total number of bytes read from write queue (Byte)
system.mem ctrl.bytesReadSys
                                            438166513
# Total read bytes from the system interface side (Byte)
```

```
system.mem ctrl.bytesWrittenSys
                                             19943987
# Total written bytes from the system interface side (Byte)
system.mem ctrl.avgRdBWSys
                                        883599923.18667221
# Average system read bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.avgWrBWSys
                                         40218740.72616770
# Average system write bandwidth in Byte/s ((Byte/Second))
                                         495887893000
system.mem ctrl.totGap
# Total gap between requests (Tick)
system.mem ctrl.avgGap
                                             24601.37
# Average gap between requests ((Tick/Count))
system.mem ctrl.requestorReadBytes::cpu.inst
                                               415826944
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorReadBytes::cpu.data
                                                13849638
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorWriteBytes::cpu.data
                                                    878614
# Per-requestor bytes write to memory (Byte)
system.mem ctrl.requestorReadRate::cpu.inst 838550288.249318242073
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorReadRate::cpu.data 27928969.261426001787
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorWriteRate::cpu.data 1771799.623835550621
# Per-requestor bytes write to memory rate ((Byte/Second))
system.mem ctrl.requestorReadAccesses::cpu.inst
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorReadAccesses::cpu.data
                                                     6333817
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorWriteAccesses::cpu.data
# Per-requestor write serviced memory accesses (Count)
system.mem ctrl.requestorReadTotalLat::cpu.inst 258411205000
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorReadTotalLat::cpu.data 202843452750
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorWriteTotalLat::cpu.data 11017646788500
# Per-requestor write total memory access latency (Tick)
                                                 39772.12
system.mem ctrl.requestorReadAvgLat::cpu.inst
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorReadAvgLat::cpu.data 32025.47
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorWriteAvgLat::cpu.data 1503949.91
# Per-requestor write average memory access latency ((Tick/Count))
system.mem ctrl.dram.bytesRead::cpu.inst
                                           415826880
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::cpu.data
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::total
                                            438166449
# Number of bytes read from this memory (Byte)
```

```
system.mem ctrl.dram.bytesInstRead::cpu.inst
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::total
                                             415826880
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesWritten::cpu.data
                                                19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.bytesWritten::total
                                           19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.numReads::cpu.inst
                                              6497295
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::cpu.data
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::total
                                             12831112
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::cpu.data
                                              7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::total
                                              7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.bwRead::cpu.inst
                                            838550159
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::cpu.data
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::total
                                          883599794
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::cpu.inst
                                          838550159
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::total
                                           838550159
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::cpu.data
                                            40218741
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::total
                                           40218741
# Write bandwidth from this memory ((Byte/Second))
system.mem_ctrl.dram.bwTotal::cpu.inst
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.data
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::total
                                          923818535
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.readBursts
                                             10708924
# Number of DRAM read bursts (Count)
system.mem ctrl.dram.writeBursts
                                               749750
# Number of DRAM write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::0
                                            9761533
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::1
                                                57754
# Per bank write bursts (Count)
```

<pre>system.mem_ctrl.dram.perBankRdBursts::2</pre>	58016
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::3</pre>	61829
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::4</pre>	65663
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::5</pre>	65660
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::6</pre>	65545
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::7</pre>	65696
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::8</pre>	65575
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::9</pre>	65929
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::10</pre>	65884
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::11</pre>	65592
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::12</pre>	65674
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::13</pre>	62819
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::14</pre>	57931
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::15</pre>	57824
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankWrBursts::0</pre>	83509
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankWrBursts::1</pre>	41674
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankWrBursts::2</pre>	41603
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankWrBursts::3</pre>	42298
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankWrBursts::4</pre>	44550
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankWrBursts::5</pre>	45300
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankWrBursts::6	45623
# Per bank write bursts (Count)	45005
system.mem_ctrl.dram.perBankWrBursts::7	45935
# Per bank write bursts (Count)	4.64.4.5
system.mem_ctrl.dram.perBankWrBursts::8	46117
# Per bank write bursts (Count)	

```
system.mem ctrl.dram.perBankWrBursts::9
                                                46320
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::10
                                                46537
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::11
                                                46733
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::12
                                                46879
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::13
                                                44948
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::14
                                                40816
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::15
                                                40908
# Per bank write bursts (Count)
system.mem ctrl.dram.totQLat
                                        260462332750
# Total ticks spent queuing (Tick)
system.mem ctrl.dram.totBusLat
                                         53544620000
# Total ticks spent in databus transfers (Tick)
system.mem ctrl.dram.totMemAccLat
                                        461254657750
# Total ticks spent from burst creation until serviced by the DRAM (Tick)
system.mem ctrl.dram.avgQLat
                                             24321.99
# Average queueing delay per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgBusLat
# Average bus latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgMemAccLat
# Average memory access latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.readRowHits
                                              4119584
# Number of row buffer hits during reads (Count)
system.mem ctrl.dram.writeRowHits
                                               688318
# Number of row buffer hits during writes (Count)
system.mem ctrl.dram.readRowHitRate
                                                38.47
# Row buffer hit rate for reads (Ratio)
system.mem ctrl.dram.writeRowHitRate
                                                91.81
# Row buffer hit rate for writes (Ratio)
system.mem ctrl.dram.bytesPerActivate::samples
                                                    6650760
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::mean
                                              110.265683
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::gmean
                                               93.794039
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::stdev 114.591988
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::0-127
                                                  3391789
                                                              51.00%
51.00% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::128-255 3143785
                                                                47.27%
98.27% # Bytes accessed per row activation (Byte)
```

```
system.mem ctrl.dram.bytesPerActivate::256-383
                                                       8903
                                                                 0.13%
98.40% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::384-511
                                                       4696
                                                                  0.07%
98.47% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::512-639
                                                       3004
                                                                  0.05%
98.52% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::640-767
                                                       3487
                                                                  0.05%
98.57% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::768-895
                                                       5010
                                                                  0.08%
98.65% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::896-1023
                                                                   0.21%
                                                       14191
98.86% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::1024-1151
                                                                   1.14%
                                                        75895
100.00% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::total
                                                 6650760
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesRead
                                            685371136
# Total bytes read (Byte)
system.mem ctrl.dram.bytesWritten
                                             47984000
# Total bytes written (Byte)
system.mem ctrl.dram.avgRdBW
                                          1382.109005
# Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.avgWrBW
                                            96.763804
# Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.peakBW
                                             12800.00
# Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem ctrl.dram.busUtil
# Data bus utilization in percentage (Ratio)
system.mem ctrl.dram.busUtilRead
                                                10.80
# Data bus utilization in percentage for reads (Ratio)
system.mem ctrl.dram.busUtilWrite
# Data bus utilization in percentage for writes (Ratio)
system.mem ctrl.dram.pageHitRate
                                                41.96
# Row buffer hit rate, read and write combined (Ratio)
system.mem ctrl.dram.power state.pwrStateResidencyTicks::UNDEFINED
495887903000
                                   # Cumulative time (in ticks) in various
power states (Tick)
system.mem ctrl.dram.rank0.actEnergy
                                          46995401460
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preEnergy
                                          24978625485
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.readEnergy
                                          72840109440
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.writeEnergy
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.refreshEnergy 39144577680.000008
# Energy for refresh commands per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank0.actBackEnergy 178168711590
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preBackEnergy 40384145280
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.totalEnergy
                                         404549939175
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.averagePower
                                           815.809252
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank0.totalIdleTime
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::IDLE 37382178500
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::REF 16558620000
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT 441947104500
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.actEnergy
                                            491110620
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.preEnergy
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.readEnergy
                                           3621607920
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.writeEnergy
                                           1875326760
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rankl.refreshEnergy 39144577680.000008
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.actBackEnergy 66463813740
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rankl.preBackEnergy 134451427680
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank1.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.totalEnergy
                                        246308873115
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.averagePower
                                           496.702726
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank1.totalIdleTime
                                                    0
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::IDLE 348505776500
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::REF 16558620000
# Time in different power states (Tick)
                                                         0
system.mem ctrl.dram.rank1.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT 130823506500
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT PDN
                                                            0
# Time in different power states (Tick)
system.mem ctrl.power state.pwrStateResidencyTicks::UNDEFINED 495887903000
# Cumulative time (in ticks) in various power states (Tick)
system.membus.transDist::ReadReq
                                             12831097
# Transaction distribution (Count)
system.membus.transDist::ReadResp
                                             12831096
# Transaction distribution (Count)
system.membus.transDist::WriteReq
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::WriteResp
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadReg
                                                    16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadResp
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteReq
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteResp
                                                      16
# Transaction distribution (Count)
system.membus.pktCount system.cpu.icache port::system.mem ctrl.port
12994591
                               # Packet count per connected requestor and
responder (Count)
system.membus.pktCount system.cpu.icache port::total
                                                         12994591
# Packet count per connected requestor and responder (Count)
system.membus.pktCount system.cpu.dcache port::system.mem ctrl.port
                               # Packet count per connected requestor and
27319248
responder (Count)
```

```
system.membus.pktCount system.cpu.dcache port::total
# Packet count per connected requestor and responder (Count)
system.membus.pktCount::total
                                              40313839
# Packet count per connected requestor and responder (Count)
system.membus.pktSize system.cpu.icache port::system.mem ctrl.port
415826880
                                # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.icache port::total
                                                        415826880
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::system.mem ctrl.port
42283556
                               # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::total
                                                         42283556
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total
                                            458110436
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops
# Total snoops (Count)
system.membus.snoopTraffic
                                                     0
# Total snoop traffic (Byte)
system.membus.snoopFanout::samples
                                             20156920
# Request fanout histogram (Count)
system.membus.snoopFanout::mean
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::stdev
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::underflows
                                                            0.00%
0.00% # Request famout histogram (Count)
system.membus.snoopFanout::0
                                              20156920
                                                          100.00%
100.00% # Request fanout histogram (Count)
system.membus.snoopFanout::1
                                                     \cap
                                                            0.00%
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::overflows
                                                            0.00%
                                                     0
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::min value
                                                     \Omega
# Request fanout histogram (Count)
system.membus.snoopFanout::max value
# Request fanout histogram (Count)
system.membus.snoopFanout::total
                                              20156920
# Request fanout histogram (Count)
system.membus.power state.pwrStateResidencyTicks::UNDEFINED 495887903000
# Cumulative time (in ticks) in various power states (Tick)
system.membus.reqLayer2.occupancy
                                         27482727000
# Layer occupancy (ticks) (Tick)
system.membus.reqLayer2.utilization
                                                   0.1
# Layer utilization (Ratio)
```

```
system.membus.respLayer0.occupancy
                                    34870803250
# Layer occupancy (ticks) (Tick)
system.membus.respLayer0.utilization
                                                 0.1
# Layer utilization (Ratio)
system.membus.respLayer1.occupancy 21328052248
# Layer occupancy (ticks) (Tick)
system.membus.respLayer1.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.snoop filter.totRequests
# Total number of requests made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleRequests
# Number of requests hitting in the snoop filter with a single holder of
the requested data. (Count)
system.membus.snoop filter.hitMultiRequests
# Number of requests hitting in the snoop filter with multiple (>1)
holders of the requested data. (Count)
system.membus.snoop filter.totSnoops
# Total number of snoops made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleSnoops
# Number of snoops hitting in the snoop filter with a single holder of the
requested data. (Count)
system.membus.snoop filter.hitMultiSnoops
# Number of snoops hitting in the snoop filter with multiple (>1) holders
of the requested data. (Count)
system.workload.inst.arm
                                                   0
# number of arm instructions executed (Count)
system.workload.inst.quiesce
# number of quiesce instructions executed (Count)
----- End Simulation Statistics -----
----- Begin Simulation Statistics -----
                                            2.904979
simSeconds
# Number of seconds simulated (Second)
                                       2904978744369
simTicks
# Number of ticks simulated (Tick)
finalTick
                                        2904978744369
# Number of ticks from beginning of simulation (restored from checkpoints
and never reset) (Tick)
simFreq
                                        1000000000000
# The number of ticks per simulated second ((Tick/Second))
hostSeconds
                                              151.65
# Real time elapsed on the host (Second)
hostTickRate
                                         19155619113
# The number of ticks simulated per host second (ticks/s) ((Tick/Second))
```

```
655496
hostMemory
# Number of bytes of host memory used (Byte)
simInsts
                                             36199500
# Number of instructions simulated (Count)
                                             76555494
simOps
# Number of ops (including micro ops) simulated (Count)
hostInstRate
# Simulator instruction rate (inst/s) ((Count/Second))
hostOpRate
                                               504812
# Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk domain.clock
# Clock period in ticks (Tick)
system.clk domain.voltage domain.voltage
                                                    1
# Voltage in Volts (Volt)
system.cpu.numCycles
                                           8723659893
# Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted
# Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted
# Number of work items this cpu completed (Count)
system.cpu.exec context.thread 0.numInsts
# Number of instructions committed (Count)
system.cpu.exec context.thread 0.numOps
# Number of ops (including micro ops) committed (Count)
system.cpu.exec context.thread 0.numIntAluAccesses
                                                     76554574
# Number of integer alu accesses (Count)
system.cpu.exec context.thread 0.numFpAluAccesses
                                                           1471
# Number of float alu accesses (Count)
system.cpu.exec_context.thread 0.numVecAluAccesses
                                                               0
# Number of vector alu accesses (Count)
system.cpu.exec context.thread 0.numCallsReturns
# Number of times a function call or return occured (Count)
system.cpu.exec context.thread 0.numCondCtrlInsts
# Number of instructions that are conditional controls (Count)
                                                 76554574
system.cpu.exec context.thread 0.numIntInsts
# Number of integer instructions (Count)
system.cpu.exec context.thread 0.numFpInsts
                                                    1471
# Number of float instructions (Count)
system.cpu.exec context.thread 0.numVecInsts
                                                         0
# Number of vector instructions (Count)
system.cpu.exec context.thread 0.numIntRegReads
                                                    87007781
# Number of times the integer registers were read (Count)
system.cpu.exec context.thread 0.numIntRegWrites
# Number of times the integer registers were written (Count)
system.cpu.exec context.thread 0.numFpRegReads
# Number of times the floating registers were read (Count)
```

```
system.cpu.exec context.thread 0.numFpRegWrites
# Number of times the floating registers were written (Count)
system.cpu.exec context.thread 0.numVecRegReads
# Number of times the vector registers were read (Count)
system.cpu.exec context.thread 0.numVecRegWrites
# Number of times the vector registers were written (Count)
system.cpu.exec context.thread 0.numVecPredRegReads
# Number of times the predicate registers were read (Count)
system.cpu.exec context.thread 0.numVecPredRegWrites
# Number of times the predicate registers were written (Count)
system.cpu.exec context.thread 0.numCCRegReads
# Number of times the CC registers were read (Count)
system.cpu.exec context.thread 0.numCCRegWrites
                                                    24904504
# Number of times the CC registers were written (Count)
system.cpu.exec context.thread 0.numMiscRegReads
# Number of times the Misc registers were read (Count)
system.cpu.exec context.thread 0.numMiscRegWrites
# Number of times the Misc registers were written (Count)
system.cpu.exec context.thread 0.numMemRefs
                                                22899889
# Number of memory refs (Count)
system.cpu.exec context.thread 0.numLoadInsts
                                                  15574080
# Number of load instructions (Count)
system.cpu.exec context.thread 0.numStoreInsts
                                                    7325809
# Number of store instructions (Count)
system.cpu.exec context.thread 0.numIdleCycles
                                                   0.003003
# Number of idle cycles (Cycle)
system.cpu.exec context.thread 0.numBusyCycles 8723659892.996996
# Number of busy cycles (Cycle)
system.cpu.exec context.thread_0.notIdleFraction
                                                     1.000000
# Percentage of non-idle cycles (Ratio)
system.cpu.exec context.thread 0.idleFraction
                                                  0.000000
# Percentage of idle cycles (Ratio)
system.cpu.exec context.thread 0.numBranches
                                                  5126544
# Number of branches fetched (Count)
system.cpu.exec context.thread 0.statExecutedInstType::No OpClass
236
         0.00%
                    0.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntAlu
                                                                  53654589
          70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntMult
         0.00%
                   70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntDiv
                                                                        28
          70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatAdd
                 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatCmp
       0.00% 70.09% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::FloatCvt
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatMult
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMultAcc
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatDiv
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatMisc
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatSqrt
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAdd
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAddAcc
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAlu
                 70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdCmp
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdCvt
                 70.09% # Class of executed instruction. (Count)
        0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdMisc
         0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMult
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMultAcc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShift
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShiftAcc
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdDiv
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSqrt
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAdd
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAlu
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCmp
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCvt
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatDiv
               70.09% # Class of executed instruction. (Count)
       0.00%
```

```
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMisc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMult
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMultAcc
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatSqrt
               70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAdd
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAlu
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceCmp
              70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceAdd
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceCmp
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAes
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAesMix
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShalHash
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha1Hash2
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash
              70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash2
      0.00%
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma2
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma3
      0.00%
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdPredAlu
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::MemRead
           20.34% 90.43% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::MemWrite
7325245
            9.57% 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemRead
                100.00% # Class of executed instruction. (Count)
        0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemWrite
        0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IprAccess
  0.00% 100.00% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::InstPrefetch
                100.00% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::total
                                                               76555515
# Class of executed instruction. (Count)
system.cpu.interrupts.clk domain.clock
                                                 5328
# Clock period in ticks (Tick)
system.cpu.mmu.dtb.rdAccesses
                                             15574084
# TLB accesses on read requests (Count)
system.cpu.mmu.dtb.wrAccesses
                                              7325810
# TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses
                                                  421
# TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses
                                                28844
# TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power state.pwrStateResidencyTicks::UNDEFINED
2904978744369
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.mmu.itb.rdAccesses
# TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses
                                             47529643
# TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses
# TLB misses on read requests (Count)
system.cpu.mmu.itb.wrMisses
                                                   56
# TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power state.pwrStateResidencyTicks::UNDEFINED
2904978744369
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.power state.pwrStateResidencyTicks::ON 2904978744369
# Cumulative time (in ticks) in various power states (Tick)
system.cpu.thread 0.numInsts
                                                    0
# Number of Instructions committed (Count)
system.cpu.thread 0.numOps
                                                    0
# Number of Ops committed (Count)
system.cpu.thread 0.numMemRefs
                                                    0
# Number of Memory References (Count)
system.cpu.workload.numSyscalls
                                                   17
# Number of system calls (Count)
system.mem ctrl.avgPriority cpu.inst::samples 47529643.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.avgPriority cpu.data::samples
                                               6943403.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.priorityMinLatency
                                        0.000000018750
# per QoS priority minimum request to response latency (Second)
system.mem ctrl.priorityMaxLatency 1.983623239254
# per QoS priority maximum request to response latency (Second)
```

```
system.mem ctrl.numReadWriteTurnArounds
# Number of turnarounds from READ to WRITE (Count)
system.mem ctrl.numWriteReadTurnArounds
# Number of turnarounds from WRITE to READ (Count)
system.mem ctrl.numStayReadState
                                            115552918
# Number of times bus staying in READ state (Count)
system.mem ctrl.numStayWriteState
# Number of times bus staying in WRITE state (Count)
system.mem ctrl.readReqs
# Number of read requests accepted (Count)
                                              7325807
system.mem ctrl.writeReqs
# Number of write requests accepted (Count)
system.mem ctrl.readBursts
                                             63103726
# Number of controller read bursts, including those serviced by the write
queue (Count)
system.mem ctrl.writeBursts
                                              7325807
# Number of controller write bursts, including those merged in the write
queue (Count)
system.mem ctrl.servicedByWrQ
                                              9340636
# Number of controller read bursts serviced by the write queue (Count)
system.mem ctrl.mergedWrBursts
                                              6615851
# Number of controller write bursts merged with an existing one (Count)
system.mem ctrl.neitherReadNorWriteReqs
# Number of requests that are neither read nor write (Count)
system.mem ctrl.avgRdQLen
# Average read queue length when enqueuing ((Count/Tick))
system.mem ctrl.avgWrQLen
# Average write queue length when enqueuing ((Count/Tick))
system.mem ctrl.numRdRetry
# Number of times read queue was full causing retry (Count)
system.mem ctrl.numWrRetry
# Number of times write queue was full causing retry (Count)
system.mem ctrl.readPktSize::0
                                              1001231
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::1
                                                    19
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::2
                                             14571441
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::3
                                             47531035
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::4
                                                     \Omega
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::5
                                                     0
# Read request sizes (log2) (Count)
                                                     0
system.mem ctrl.readPktSize::6
# Read request sizes (log2) (Count)
```

```
system.mem ctrl.writePktSize::0
                                              3122099
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::1
                                                    3
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::2
                                              4201939
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::3
                                                 1766
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::4
                                                     0
# Write request sizes (log2) (Count)
                                                     0
system.mem ctrl.writePktSize::5
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::6
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.rdQLenPdf::0
                                             53763086
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::1
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::2
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::3
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::4
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::5
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::6
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::7
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::8
# What read queue length does an incoming reg see (Count)
system.mem_ctrl.rdQLenPdf::9
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::10
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::11
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::12
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::13
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::14
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::15
# What read queue length does an incoming req see (Count)
```

```
system.mem ctrl.rdQLenPdf::16
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::17
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::18
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::19
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::20
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::21
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::22
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::23
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::24
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::25
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::26
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::27
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::28
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::29
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::30
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::31
# What read queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::0
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::2
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::3
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::4
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::5
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::6
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::7
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::8
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::9
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::10
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::11
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::12
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::13
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::14
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::15
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::16
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::17
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::18
                                                44371
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::19
                                                 44371
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::20
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::21
                                                44371
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::22
                                                44371
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::23
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::24
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::25
                                                44371
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::26
                                                 44371
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::27
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::28
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::29
                                                 44371
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::30
                                                44371
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::31
                                                44371
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::32
                                                44371
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::33
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::34
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::35
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::36
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::37
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::38
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::39
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::40
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::41
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::42
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::43
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::44
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::45
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::46
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::47
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::48
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::49
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::50
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::51
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::52
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::53
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::54
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::55
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::56
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::57
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::58
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::59
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::60
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::61
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::62
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::63
# What write queue length does an incoming req see (Count)
system.mem ctrl.rdPerTurnAround::samples
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::mean 1211.670122
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::gmean
                                          338.242484
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::stdev 86586.289948
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::0-1.04858e+06
                                                     44370
                                                              100.00%
100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07
         100.00% # Reads before turning the bus around for writes (Count)
0.00%
system.mem ctrl.rdPerTurnAround::total
                                               44371
# Reads before turning the bus around for writes (Count)
system.mem ctrl.wrPerTurnAround::samples
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::mean
                                          16.000045
# Writes before turning the bus around for reads (Count)
                                          16.000042
system.mem ctrl.wrPerTurnAround::gmean
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::stdev 0.009495
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::16
                                               44370
                                                       100.00%
100.00% # Writes before turning the bus around for reads (Count)
```

```
system.mem ctrl.wrPerTurnAround::18
                                                           0.00%
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::total
                                                44371
# Writes before turning the bus around for reads (Count)
system.mem ctrl.bytesReadWrQ
                                            597800704
# Total number of bytes read from write queue (Byte)
                                           439535306
system.mem ctrl.bytesReadSys
# Total read bytes from the system interface side (Byte)
system.mem ctrl.bytesWrittenSys
                                           19943987
# Total written bytes from the system interface side (Byte)
                                         151304138.40445256
system.mem ctrl.avgRdBWSys
# Average system read bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.avgWrBWSys
                                        6865450.23389908
# Average system write bandwidth in Byte/s ((Byte/Second))
                                        2904978632481
system.mem ctrl.totGap
# Total gap between requests (Tick)
system.mem ctrl.avgGap
                                             41246.60
# Average gap between requests ((Tick/Count))
system.mem ctrl.requestorReadBytes::cpu.inst
                                                380237144
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorReadBytes::cpu.data
                                               21934765
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorWriteBytes::cpu.data
                                                    721850
# Per-requestor bytes write to memory (Byte)
system.mem ctrl.requestorReadRate::cpu.inst 130891540.854489982128
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorReadRate::cpu.data 7550748.879838885739
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorWriteRate::cpu.data 248487.188210664666
# Per-requestor bytes write to memory rate ((Byte/Second))
system.mem ctrl.requestorReadAccesses::cpu.inst
# Per-requestor read serviced memory accesses (Count)
system.mem_ctrl.requestorReadAccesses::cpu.data
                                                   15574083
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorWriteAccesses::cpu.data
                                                      7325807
# Per-requestor write serviced memory accesses (Count)
system.mem ctrl.requestorReadTotalLat::cpu.inst 1143607376552
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorReadTotalLat::cpu.data 267861554323
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorWriteTotalLat::cpu.data 70795069287956
# Per-requestor write total memory access latency (Tick)
system.mem ctrl.requestorReadAvgLat::cpu.inst
                                                 24060.93
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorReadAvgLat::cpu.data 17199.19
# Per-requestor read average memory access latency ((Tick/Count))
```

```
system.mem ctrl.requestorWriteAvgLat::cpu.data 9663791.21
# Per-requestor write average memory access latency ((Tick/Count))
system.mem ctrl.dram.bytesRead::cpu.inst
                                            380237144
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::cpu.data
                                             59298162
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::total
                                            439535306
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::cpu.inst
                                                380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::total
                                             380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesWritten::cpu.data
                                                19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.bytesWritten::total
                                             19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.numReads::cpu.inst
                                          47529643
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::cpu.data
                                             15574083
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::total
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::cpu.data
                                              7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::total
                                              7325807
# Number of write requests responded to by this memory (Count)
                                           130891541
system.mem ctrl.dram.bwRead::cpu.inst
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::cpu.data
                                            20412598
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::total
                                           151304138
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::cpu.inst
                                           130891541
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::total
                                           130891541
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::cpu.data
                                              6865450
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::total
                                              6865450
# Write bandwidth from this memory ((Byte/Second))
                                           130891541
system.mem ctrl.dram.bwTotal::cpu.inst
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.data
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::total
                                            158169589
# Total bandwidth to/from this memory ((Byte/Second))
```

<pre>system.mem_ctrl.dram.readBursts</pre>	53763090
# Number of DRAM read bursts (Count)	
system.mem_ctrl.dram.writeBursts	709938
# Number of DRAM write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::0</pre>	52805285
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::1</pre>	58690
# Per bank write bursts (Count)	
<pre>system.mem_ctrl.dram.perBankRdBursts::2</pre>	58157
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::3</pre>	61971
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::4</pre>	66160
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::5</pre>	66349
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::6</pre>	65557
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::7</pre>	66179
<pre># Per bank write bursts (Count)</pre>	
<pre>system.mem_ctrl.dram.perBankRdBursts::8</pre>	65688
<pre># Per bank write bursts (Count)</pre>	
system.mem_ctrl.dram.perBankRdBursts::9	67381
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankRdBursts::10	66785
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankRdBursts::11	65843
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankRdBursts::12	66137
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankRdBursts::13	62865
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankRdBursts::14	58979
# Per bank write bursts (Count)	64.0.64
system.mem_ctrl.dram.perBankRdBursts::15	61064
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankWrBursts::0	44533
# Per bank write bursts (Count)	44.00
system.mem_ctrl.dram.perBankWrBursts::1	41907
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankWrBursts::2	41515
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankWrBursts::3	42093
# Per bank write bursts (Count)	
system.mem_ctrl.dram.perBankWrBursts::4	44340
# Per bank write bursts (Count)	

```
system.mem ctrl.dram.perBankWrBursts::5 45115
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::6
                                               45484
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::7
                                               45866
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::8
                                               46100
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::9
                                               46302
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::10
                                               46512
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::11
                                               46708
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::12
                                               46858
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::13
                                               44924
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::14
                                              40794
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::15
                                                40887
# Per bank write bursts (Count)
system.mem ctrl.dram.totQLat
                                       403410993375
# Total ticks spent queuing (Tick)
system.mem ctrl.dram.totBusLat
                                        268815450000
# Total ticks spent in databus transfers (Tick)
system.mem ctrl.dram.totMemAccLat
                                       1411468930875
# Total ticks spent from burst creation until serviced by the DRAM (Tick)
system.mem ctrl.dram.avgQLat
                                              7503.49
# Average queueing delay per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgBusLat
# Average bus latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgMemAccLat
                                            26253.49
# Average memory access latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.readRowHits
# Number of row buffer hits during reads (Count)
system.mem ctrl.dram.writeRowHits
                                              648271
# Number of row buffer hits during writes (Count)
system.mem ctrl.dram.readRowHitRate
                                               78.47
# Row buffer hit rate for reads (Ratio)
system.mem ctrl.dram.writeRowHitRate
                                               91.31
# Row buffer hit rate for writes (Ratio)
system.mem ctrl.dram.bytesPerActivate::samples
                                                  11636492
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::mean 299.597937
# Bytes accessed per row activation (Byte)
```

```
system.mem ctrl.dram.bytesPerActivate::gmean
                                               170.594697
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::stdev
                                               305.879668
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::0-127
                                                  5442191
                                                              46.77%
46.77% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::128-255
                                                    2170999
                                                                18.66%
65.43% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::256-383
                                                      68240
                                                                 0.59%
66.01% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::384-511
                                                                 2.09%
                                                     243053
68.10% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::512-639
                                                                 8.54%
                                                     993233
76.64% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::640-767
                                                    2082764
                                                                17.90%
94.53% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::768-895
                                                       3089
                                                                 0.03%
94.56% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::896-1023
                                                        3745
                                                                  0.03%
94.59% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::1024-1151
                                                       629178
                                                                   5.41%
100.00% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::total
                                                 11636492
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesRead
                                           3440837760
# Total bytes read (Byte)
system.mem ctrl.dram.bytesWritten
                                             45436032
# Total bytes written (Byte)
system.mem ctrl.dram.avgRdBW
                                          1184.462285
# Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.avgWrBW
                                            15.640745
# Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.peakBW
                                             12800.00
# Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem ctrl.dram.busUtil
                                                 9.38
# Data bus utilization in percentage (Ratio)
system.mem ctrl.dram.busUtilRead
                                                 9.25
# Data bus utilization in percentage for reads (Ratio)
system.mem ctrl.dram.busUtilWrite
                                                 0.12
# Data bus utilization in percentage for writes (Ratio)
system.mem ctrl.dram.pageHitRate
# Row buffer hit rate, read and write combined (Ratio)
system.mem ctrl.dram.power state.pwrStateResidencyTicks::UNDEFINED
2904978744369
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.mem ctrl.dram.rank0.actEnergy 82411657860
# Energy for activate commands per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank0.preEnergy
                                        43802815980
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.readEnergy
                                        380193204720
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.writeEnergy
                                           1831452660
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.refreshEnergy 229316037600.000031
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actBackEnergy 1259461453290
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preBackEnergy 54912719520
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.selfRefreshEnergy
                                                        0
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.totalEnergy
                                         2051929341630
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.averagePower
                                           706.349176
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank0.totalIdleTime
                                                    0
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::IDLE 16427461440
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::REF
                                              97003400000
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::SREF
                                                         0
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT 2791547882929
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT PDN
                                                            0
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.actEnergy
                                            672959280
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.preEnergy
                                            357671160
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.readEnergy
                                           3675257880
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.writeEnergy
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.refreshEnergy 229316037600.000031
# Energy for refresh commands per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank1.actBackEnergy 261012021960
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.preBackEnergy 895712240640
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.totalEnergy
                                         1392620612220
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.averagePower
                                           479.390982
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank1.totalIdleTime
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::IDLE 2326194428411
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::REF 97003400000
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT 481780915958
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT PDN
# Time in different power states (Tick)
system.mem ctrl.power state.pwrStateResidencyTicks::UNDEFINED
2904978744369
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.membus.transDist::ReadReg
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::ReadResp
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::WriteReq
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::WriteResp
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadReq
                                                    16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadResp
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteReq
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteResp
                                                      16
# Transaction distribution (Count)
```

```
system.membus.pktCount system.cpu.icache port::system.mem ctrl.port
95059286
                               # Packet count per connected requestor and
responder (Count)
system.membus.pktCount system.cpu.icache port::total
# Packet count per connected requestor and responder (Count)
system.membus.pktCount system.cpu.dcache port::system.mem ctrl.port
45799780
                               # Packet count per connected requestor and
responder (Count)
system.membus.pktCount system.cpu.dcache port::total
                                                          45799780
# Packet count per connected requestor and responder (Count)
system.membus.pktCount::total
                                            140859066
# Packet count per connected requestor and responder (Count)
system.membus.pktSize system.cpu.icache port::system.mem ctrl.port
                                # Cumulative packet size per connected
380237144
requestor and responder (Byte)
system.membus.pktSize system.cpu.icache port::total
                                                        380237144
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::system.mem ctrl.port
79242149
                               # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::total
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total
                                            459479293
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops
# Total snoops (Count)
system.membus.snoopTraffic
                                                     0
# Total snoop traffic (Byte)
system.membus.snoopFanout::samples
                                             70429533
# Request fanout histogram (Count)
system.membus.snoopFanout::mean
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::stdev
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::underflows
                                                            0.00%
0.00% # Request famout histogram (Count)
system.membus.snoopFanout::0
                                             70429533
                                                          100.00%
100.00% # Request famout histogram (Count)
                                                            0.00%
system.membus.snoopFanout::1
100.00% # Request fanout histogram (Count)
                                                            0.00%
system.membus.snoopFanout::overflows
                                                     \cap
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::min value
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::max value
                                                     0
# Request fanout histogram (Count)
```

```
system.membus.snoopFanout::total
                                            70429533
# Request fanout histogram (Count)
system.membus.power state.pwrStateResidencyTicks::UNDEFINED 2904978744369
# Cumulative time (in ticks) in various power states (Tick)
system.membus.reqLayer2.occupancy
                                         25892528220
# Layer occupancy (ticks) (Tick)
system.membus.reqLayer2.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.respLayer0.occupancy
                                       40605288314
# Layer occupancy (ticks) (Tick)
system.membus.respLayer0.utilization
                                                 0.0
# Layer utilization (Ratio)
                                        18475240264
system.membus.respLayer1.occupancy
# Layer occupancy (ticks) (Tick)
system.membus.respLayer1.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.snoop filter.totRequests
# Total number of requests made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleRequests
# Number of requests hitting in the snoop filter with a single holder of
the requested data. (Count)
system.membus.snoop filter.hitMultiRequests
# Number of requests hitting in the snoop filter with multiple (>1)
holders of the requested data. (Count)
system.membus.snoop filter.totSnoops
# Total number of snoops made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleSnoops
# Number of snoops hitting in the snoop filter with a single holder of the
requested data. (Count)
system.membus.snoop filter.hitMultiSnoops
# Number of snoops hitting in the snoop filter with multiple (>1) holders
of the requested data. (Count)
system.workload.inst.arm
# number of arm instructions executed (Count)
system.workload.inst.quiesce
# number of quiesce instructions executed (Count)
----- End Simulation Statistics -----
Stats 4.3
----- Begin Simulation Statistics -----
simSeconds
                                            3.271749
# Number of seconds simulated (Second)
simTicks
                                        3271748533000
# Number of ticks simulated (Tick)
```

```
finalTick
                                         3271748533000
# Number of ticks from beginning of simulation (restored from checkpoints
and never reset) (Tick)
                                         10000000000000
simFreq
# The number of ticks per simulated second ((Tick/Second))
hostSeconds
# Real time elapsed on the host (Second)
hostTickRate
                                          21450822174
# The number of ticks simulated per host second (ticks/s) ((Tick/Second))
hostMemorv
# Number of bytes of host memory used (Byte)
                                             36199500
simInsts
# Number of instructions simulated (Count)
simOps
                                             76555494
# Number of ops (including micro ops) simulated (Count)
hostInstRate
# Simulator instruction rate (inst/s) ((Count/Second))
hostOpRate
# Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk domain.clock
                                                 1000
# Clock period in ticks (Tick)
system.clk domain.voltage domain.voltage
# Voltage in Volts (Volt)
                                           3271748533
system.cpu.numCycles
# Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted
                                                    0
# Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted
# Number of work items this cpu completed (Count)
system.cpu.exec context.thread 0.numInsts
# Number of instructions committed (Count)
system.cpu.exec context.thread 0.numOps
# Number of ops (including micro ops) committed (Count)
system.cpu.exec context.thread 0.numIntAluAccesses 76554574
# Number of integer alu accesses (Count)
system.cpu.exec context.thread 0.numFpAluAccesses
                                                          1471
# Number of float alu accesses (Count)
system.cpu.exec context.thread 0.numVecAluAccesses
# Number of vector alu accesses (Count)
system.cpu.exec context.thread 0.numCallsReturns
# Number of times a function call or return occured (Count)
system.cpu.exec context.thread 0.numCondCtrlInsts
# Number of instructions that are conditional controls (Count)
system.cpu.exec context.thread 0.numIntInsts
# Number of integer instructions (Count)
system.cpu.exec context.thread 0.numFpInsts
                                                    1471
# Number of float instructions (Count)
```

```
system.cpu.exec context.thread 0.numVecInsts
                                                        0
# Number of vector instructions (Count)
system.cpu.exec context.thread 0.numIntRegReads
                                                    87007781
# Number of times the integer registers were read (Count)
system.cpu.exec context.thread 0.numIntRegWrites
                                                     58976338
# Number of times the integer registers were written (Count)
system.cpu.exec context.thread 0.numFpRegReads
# Number of times the floating registers were read (Count)
system.cpu.exec context.thread 0.numFpRegWrites
# Number of times the floating registers were written (Count)
system.cpu.exec context.thread 0.numVecRegReads
# Number of times the vector registers were read (Count)
system.cpu.exec context.thread 0.numVecRegWrites
# Number of times the vector registers were written (Count)
system.cpu.exec context.thread 0.numVecPredRegReads
# Number of times the predicate registers were read (Count)
system.cpu.exec context.thread 0.numVecPredRegWrites
# Number of times the predicate registers were written (Count)
system.cpu.exec context.thread 0.numCCRegReads
                                                   26632889
# Number of times the CC registers were read (Count)
system.cpu.exec context.thread 0.numCCRegWrites
# Number of times the CC registers were written (Count)
system.cpu.exec context.thread 0.numMiscRegReads
                                                     37276209
# Number of times the Misc registers were read (Count)
system.cpu.exec context.thread 0.numMiscRegWrites
                                                             \cap
# Number of times the Misc registers were written (Count)
system.cpu.exec context.thread 0.numMemRefs
# Number of memory refs (Count)
system.cpu.exec context.thread 0.numLoadInsts
                                                  15574080
# Number of load instructions (Count)
system.cpu.exec context.thread 0.numStoreInsts
                                                    7325809
# Number of store instructions (Count)
system.cpu.exec context.thread 0.numIdleCycles
                                                   0.001000
# Number of idle cycles (Cycle)
system.cpu.exec context.thread 0.numBusyCycles 3271748532.999000
# Number of busy cycles (Cycle)
system.cpu.exec context.thread 0.notIdleFraction
                                                     1.000000
# Percentage of non-idle cycles (Ratio)
system.cpu.exec context.thread 0.idleFraction
                                                  0.000000
# Percentage of idle cycles (Ratio)
system.cpu.exec context.thread 0.numBranches
                                                  5126544
# Number of branches fetched (Count)
system.cpu.exec_context.thread 0.statExecutedInstType::No OpClass
                  0.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntAlu
                                                                  53654589
         70.09% # Class of executed instruction. (Count)
70.09%
```

```
system.cpu.exec context.thread 0.statExecutedInstType::IntMult
                  70.09% # Class of executed instruction. (Count)
177
         0.00%
system.cpu.exec context.thread 0.statExecutedInstType::IntDiv
       70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatAdd
         0.00%
                 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatCmp
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatCvt
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMult
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMultAcc
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatDiv
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMisc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatSqrt
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAdd
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAddAcc
              70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAlu
                 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdCmp
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdCvt
                70.09% # Class of executed instruction. (Count)
        0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdMisc
                  70.09% # Class of executed instruction. (Count)
         0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdMult
       0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMultAcc
       0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShift
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShiftAcc
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdDiv
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSqrt
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAdd
       0.00% 70.09% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAlu
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCmp
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCvt
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatDiv
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMisc
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMult
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMultAcc
              70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatSqrt
       0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAdd
       0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAlu
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceCmp
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceAdd
       0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceCmp
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAes
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAesMix
       0.00%
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShalHash
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha1Hash2
       0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash
       0.00%
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash2
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma2
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma3
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdPredAlu
       0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::MemRead
15573939 20.34% 90.43% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::MemWrite
             9.57%
                     100.00% # Class of executed instruction. (Count)
7325245
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemRead
         0.00% 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemWrite
         0.00%
                 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IprAccess
       0.00%
              100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::InstPrefetch
                100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::total 76555515
# Class of executed instruction. (Count)
system.cpu.interrupts.clk domain.clock
                                                16000
# Clock period in ticks (Tick)
system.cpu.mmu.dtb.rdAccesses
                                             15574084
# TLB accesses on read requests (Count)
system.cpu.mmu.dtb.wrAccesses
                                              7325810
# TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses
                                                  421
# TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses
                                                28844
# TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power state.pwrStateResidencyTicks::UNDEFINED
3271748533000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.mmu.itb.rdAccesses
                                                    0
# TLB accesses on read requests (Count)
                                             47529643
system.cpu.mmu.itb.wrAccesses
# TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses
                                                    0
# TLB misses on read requests (Count)
                                                   56
system.cpu.mmu.itb.wrMisses
# TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power state.pwrStateResidencyTicks::UNDEFINED
3271748533000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.power state.pwrStateResidencyTicks::ON 3271748533000
# Cumulative time (in ticks) in various power states (Tick)
system.cpu.thread 0.numInsts
# Number of Instructions committed (Count)
system.cpu.thread 0.numOps
                                                    \Omega
# Number of Ops committed (Count)
system.cpu.thread 0.numMemRefs
                                                    0
# Number of Memory References (Count)
system.cpu.workload.numSyscalls
                                                   17
# Number of system calls (Count)
```

```
system.mem ctrl.avgPriority cpu.inst::samples 47529643.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.avgPriority cpu.data::samples 6926926.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.priorityMinLatency
                                        0.000000016842
# per QoS priority minimum request to response latency (Second)
system.mem ctrl.priorityMaxLatency 2.172427269932
# per QoS priority maximum request to response latency (Second)
system.mem ctrl.numReadWriteTurnArounds
# Number of turnarounds from READ to WRITE (Count)
system.mem ctrl.numWriteReadTurnArounds
# Number of turnarounds from WRITE to READ (Count)
system.mem ctrl.numStayReadState
                                           115615734
# Number of times bus staying in READ state (Count)
system.mem ctrl.numStayWriteState
# Number of times bus staying in WRITE state (Count)
system.mem ctrl.readReqs
                                             63103726
# Number of read requests accepted (Count)
system.mem ctrl.writeReqs
                                             7325807
# Number of write requests accepted (Count)
system.mem ctrl.readBursts
                                             63103726
# Number of controller read bursts, including those serviced by the write
queue (Count)
                                              7325807
system.mem ctrl.writeBursts
# Number of controller write bursts, including those merged in the write
queue (Count)
system.mem ctrl.servicedByWrQ
                                              9356785
# Number of controller read bursts serviced by the write queue (Count)
system.mem ctrl.mergedWrBursts
                                              6616179
# Number of controller write bursts merged with an existing one (Count)
system.mem ctrl.neitherReadNorWriteRegs
# Number of requests that are neither read nor write (Count)
system.mem ctrl.avgRdQLen
# Average read queue length when enqueuing ((Count/Tick))
system.mem ctrl.avgWrQLen
# Average write queue length when enqueuing ((Count/Tick))
system.mem ctrl.numRdRetry
# Number of times read queue was full causing retry (Count)
system.mem ctrl.numWrRetry
# Number of times write queue was full causing retry (Count)
                                             1001231
system.mem ctrl.readPktSize::0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::1
                                                   19
# Read request sizes (log2) (Count)
                                            14571441
system.mem ctrl.readPktSize::2
# Read request sizes (log2) (Count)
```

```
system.mem ctrl.readPktSize::3
                                             47531035
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::4
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::5
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::6
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.writePktSize::0
                                              3122099
# Write request sizes (log2) (Count)
                                                     3
system.mem ctrl.writePktSize::1
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::2
                                              4201939
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::3
                                                 1766
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::4
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::5
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::6
# Write request sizes (log2) (Count)
system.mem ctrl.rdQLenPdf::0
                                             53746937
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::1
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::2
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::3
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::4
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::5
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::6
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::7
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::8
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::9
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::10
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::11
# What read queue length does an incoming req see (Count)
```

```
system.mem ctrl.rdQLenPdf::12
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::13
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::14
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::15
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::16
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::17
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::18
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::19
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::20
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::21
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::22
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::23
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::24
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::25
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::26
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::27
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::28
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::29
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::30
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::31
# What read queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::0
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::2
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::3
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::4
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::5
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::6
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::7
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::8
                                                    1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::9
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::10
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::11
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::12
                                                    1
# What write queue length does an incoming req see (Count)
system.mem_ctrl.wrQLenPdf::13
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::14
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::15
                                                   428
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::16
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::17
                                                44298
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::18
                                                44298
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::19
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::20
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::21
                                                44298
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::22
                                                44297
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::23
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::24
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::25
                                                 44297
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::26
                                                44297
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::27
                                                44297
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::28
                                                44297
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::29
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::30
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::31
                                                44297
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::32
                                                44297
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::33
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::34
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::35
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::36
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::37
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::38
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::39
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::40
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::41
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::42
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::43
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::44
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::45
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::46
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::47
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::48
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::49
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::50
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::51
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::52
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::53
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::54
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::55
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::56
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::57
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::58
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::59
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::60
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::61
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::62
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::63
# What write queue length does an incoming reg see (Count)
system.mem ctrl.rdPerTurnAround::samples
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::mean 1213.325440
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::gmean
                                           338.733664
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::stdev 86658.496903
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::0-1.04858e+06
                                                      44296
                                                               100.00%
100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07
         100.00% # Reads before turning the bus around for writes (Count)
0.00%
system.mem ctrl.rdPerTurnAround::total
# Reads before turning the bus around for writes (Count)
system.mem ctrl.wrPerTurnAround::samples
# Writes before turning the bus around for reads (Count)
```

```
system.mem ctrl.wrPerTurnAround::mean 16.019279
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::gmean 16.018176
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::stdev
                                             0.195415
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::16
                                                43870
                                                          99.04%
99.04% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::18
                                                 427
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::total
# Writes before turning the bus around for reads (Count)
system.mem ctrl.bytesReadWrQ
                                            598834240
# Total number of bytes read from write queue (Byte)
system.mem ctrl.bytesReadSys
# Total read bytes from the system interface side (Byte)
system.mem ctrl.bytesWrittenSys
                                            19943987
# Total written bytes from the system interface side (Byte)
system.mem ctrl.avgRdBWSys
                                         134342631.03251770
# Average system read bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.avgWrBWSys
                                        6095819.03952519
# Average system write bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.totGap
                                        3271748412000
# Total gap between requests (Tick)
system.mem ctrl.avgGap
                                             46454.21
# Average gap between requests ((Tick/Count))
system.mem ctrl.requestorReadBytes::cpu.inst
                                                380237144
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorReadBytes::cpu.data
                                               21870171
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorWriteBytes::cpu.data
                                                    719938
# Per-requestor bytes write to memory (Byte)
system.mem ctrl.requestorReadRate::cpu.inst 116218327.956685915589
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorReadRate::cpu.data 6684551.327649361454
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorWriteRate::cpu.data 220046.862629708106
# Per-requestor bytes write to memory rate ((Byte/Second))
system.mem ctrl.requestorReadAccesses::cpu.inst
                                                    47529643
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorReadAccesses::cpu.data
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorWriteAccesses::cpu.data
# Per-requestor write serviced memory accesses (Count)
system.mem ctrl.requestorReadTotalLat::cpu.inst 1046412273808
# Per-requestor read total memory access latency (Tick)
```

```
system.mem ctrl.requestorReadTotalLat::cpu.data 254768310736
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorWriteTotalLat::cpu.data 85141809253008
# Per-requestor write total memory access latency (Tick)
system.mem ctrl.requestorReadAvgLat::cpu.inst
                                                 22015.99
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorReadAvgLat::cpu.data 16358.48
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorWriteAvgLat::cpu.data 11622174.77
# Per-requestor write average memory access latency ((Tick/Count))
system.mem ctrl.dram.bytesRead::cpu.inst
                                           380237144
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::cpu.data
                                         59298162
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::total
                                           439535306
# Number of bytes read from this memory (Byte)
system.mem_ctrl.dram.bytesInstRead::cpu.inst
                                               380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::total
                                            380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesWritten::cpu.data
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.bytesWritten::total
                                            19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.numReads::cpu.inst 47529643
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::cpu.data 15574083
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::total
                                            63103726
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::cpu.data
                                            7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::total
                                             7325807
# Number of write requests responded to by this memory (Count)
                                          116218328
system.mem ctrl.dram.bwRead::cpu.inst
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::cpu.data
                                       18124303
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::total
                                           134342631
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::cpu.inst 116218328
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::total 116218328
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::cpu.data
                                             6095819
# Write bandwidth from this memory ((Byte/Second))
```

```
system.mem ctrl.dram.bwWrite::total
                                              6095819
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.inst
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.data
                                             24220122
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::total
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.readBursts
                                            53746941
# Number of DRAM read bursts (Count)
                                               709606
system.mem ctrl.dram.writeBursts
# Number of DRAM write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::0
                                          52789130
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::1
                                                58693
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::2
                                               58167
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::3
                                                61969
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::4
                                                66160
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::5
                                                66349
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::6
                                                65557
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::7
                                                66179
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::8
                                                65688
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::9
                                                67381
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::10
                                                66785
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::11
                                                65848
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::12
                                                66124
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::13
                                                62866
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::14
                                                58981
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::15
                                                61064
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::0
                                               44015
# Per bank write bursts (Count)
```

```
system.mem ctrl.dram.perBankWrBursts::1 41937
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::2
                                              41594
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::3
                                              42161
# Per bank write bursts (Count)
                                               44341
system.mem ctrl.dram.perBankWrBursts::4
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::5
                                               45114
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::6
                                              45486
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::7
                                               45865
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::8
                                               46102
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::9
                                               46303
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::10
                                              46513
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::11
                                               46708
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::12
                                              46857
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::13
                                              44926
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::14
                                               40796
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::15
                                               40888
# Per bank write bursts (Count)
system.mem ctrl.dram.totQLat
                                       395974604222
# Total ticks spent queuing (Tick)
system.mem ctrl.dram.totBusLat
                                       201658522632
# Total ticks spent in databus transfers (Tick)
system.mem ctrl.dram.totMemAccLat
                                       1301180584544
# Total ticks spent from burst creation until serviced by the DRAM (Tick)
system.mem ctrl.dram.avgQLat
                                            7367.39
# Average queueing delay per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgBusLat
                                             3752.00
# Average bus latency per DRAM burst ((Tick/Count))
                                           24209.39
system.mem ctrl.dram.avgMemAccLat
# Average memory access latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.readRowHits
# Number of row buffer hits during reads (Count)
system.mem ctrl.dram.writeRowHits 648956
# Number of row buffer hits during writes (Count)
```

```
system.mem ctrl.dram.readRowHitRate
                                                78.35
# Row buffer hit rate for reads (Ratio)
system.mem ctrl.dram.writeRowHitRate
                                                91.45
# Row buffer hit rate for writes (Ratio)
system.mem ctrl.dram.bytesPerActivate::samples
                                                   11694403
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::mean
                                              298.024518
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::gmean
                                               169.571890
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::stdev
                                               306.218865
# Bytes accessed per row activation (Byte)
                                                              46.73%
system.mem ctrl.dram.bytesPerActivate::0-127
                                                  5464845
46.73% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::128-255
                                                    2236969
                                                                 19.13%
65.86% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::256-383
                                                      86170
                                                                 0.74%
66.60% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::384-511
                                                     251437
                                                                 2.15%
68.75% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::512-639
                                                     938593
                                                                 8.03%
76.77% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::640-767
                                                    2061445
                                                                17.63%
94.40% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::768-895
                                                       3086
                                                                 0.03%
94.43% # Bytes accessed per row activation (Byte)
                                                                  0.03%
system.mem ctrl.dram.bytesPerActivate::896-1023
                                                        3723
94.46% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::1024-1151
                                                       648135
                                                                   5.54%
100.00% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::total
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesRead
                                           3439804224
# Total bytes read (Byte)
system.mem ctrl.dram.bytesWritten
                                             45414784
# Total bytes written (Byte)
system.mem ctrl.dram.avgRdBW
                                          1051.365711
# Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.avgWrBW
                                            13.880891
# Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.peakBW
                                             17057.00
# Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem ctrl.dram.busUtil
                                                 6.25
# Data bus utilization in percentage (Ratio)
system.mem ctrl.dram.busUtilRead
                                                 6.16
# Data bus utilization in percentage for reads (Ratio)
```

```
system.mem ctrl.dram.busUtilWrite
                                                 0.08
# Data bus utilization in percentage for writes (Ratio)
system.mem ctrl.dram.pageHitRate
# Row buffer hit rate, read and write combined (Ratio)
system.mem ctrl.dram.power state.pwrStateResidencyTicks::UNDEFINED
3271748533000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.mem ctrl.dram.rank0.actEnergy
                                         122155663279.023529
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preEnergy
                                        60294777315.755035
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.readEnergy
                                        352318832675.713135
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.writeEnergy 1783309196.255445
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.refreshEnergy 270838752737.947968
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actBackEnergy 1651197300621.838623
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preBackEnergy 64149527831.815384
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.totalEnergy
                                        2522738163657.621582
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.averagePower
                                           771.067256
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank0.totalIdleTime
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::IDLE 22855615048
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::REF 109241600000
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT 3139651317952
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.actEnergy
                                        1052086613.762582
# Energy for activate commands per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank1.preEnergy
                                        519299161.921046
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.readEnergy
                                        3406801247.139291
# Energy for read commands per rank (pJ) (Joule)
                                        1826961765.215440
system.mem ctrl.dram.rank1.writeEnergy
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.refreshEnergy 270838752737.947968
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.actBackEnergy 329616363731.653137
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.preBackEnergy 1175478952037.081787
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
system.mem_ctrl.dram.rank1.selfRefreshEnergy
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.totalEnergy
                                        1782739217290.326904
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank1.averagePower
                                           544.888826
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank1.totalIdleTime
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::IDLE 2641049451722
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::REF 109241600000
# Time in different power states (Tick)
system.mem_ctrl.dram.rank1.pwrStateTime::SREF
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT 521457481278
# Time in different power states (Tick)
system.mem ctrl.dram.rank1.pwrStateTime::ACT PDN
                                                            0
# Time in different power states (Tick)
system.mem ctrl.power state.pwrStateResidencyTicks::UNDEFINED
3271748533000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.membus.transDist::ReadReq
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::ReadResp
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::WriteReq
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::WriteResp
                                              7325791
# Transaction distribution (Count)
```

```
system.membus.transDist::LockedRMWReadReq
                                                    16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadResp
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteReq
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteResp
                                                      16
# Transaction distribution (Count)
system.membus.pktCount system.cpu.icache port::system.mem ctrl.port
95059286
                               # Packet count per connected requestor and
responder (Count)
system.membus.pktCount system.cpu.icache port::total
                                                          95059286
# Packet count per connected requestor and responder (Count)
system.membus.pktCount system.cpu.dcache port::system.mem ctrl.port
45799780
                               # Packet count per connected requestor and
responder (Count)
system.membus.pktCount system.cpu.dcache port::total
                                                          45799780
# Packet count per connected requestor and responder (Count)
system.membus.pktCount::total
                                            140859066
# Packet count per connected requestor and responder (Count)
system.membus.pktSize system.cpu.icache port::system.mem ctrl.port
380237144
                                # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.icache port::total
                                                       380237144
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::system.mem ctrl.port
                               # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::total
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total
                                            459479293
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops
# Total snoops (Count)
system.membus.snoopTraffic
                                                     0
# Total snoop traffic (Byte)
system.membus.snoopFanout::samples
                                             70429533
# Request fanout histogram (Count)
system.membus.snoopFanout::mean
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::stdev
                                                    0
# Request fanout histogram (Count)
system.membus.snoopFanout::underflows
                                                            0.00%
0.00% # Request famout histogram (Count)
                                             70429533
                                                         100.00%
system.membus.snoopFanout::0
100.00% # Request fanout histogram (Count)
```

```
system.membus.snoopFanout::1
                                                           0.00%
100.00% # Request fanout histogram (Count)
system.membus.snoopFanout::overflows
                                                           0.00%
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::min value
# Request fanout histogram (Count)
system.membus.snoopFanout::max value
                                                    0
# Request fanout histogram (Count)
system.membus.snoopFanout::total
                                             70429533
# Request fanout histogram (Count)
system.membus.power state.pwrStateResidencyTicks::UNDEFINED 3271748533000
# Cumulative time (in ticks) in various power states (Tick)
system.membus.reqLayer2.occupancy
                                         77755340000
# Layer occupancy (ticks) (Tick)
system.membus.reqLayer2.utilization
                                                  0.0
# Layer utilization (Ratio)
system.membus.respLayer0.occupancy 106964241192
# Layer occupancy (ticks) (Tick)
system.membus.respLayer0.utilization
                                                  0.0
# Layer utilization (Ratio)
system.membus.respLayer1.occupancy
                                     43751319264
# Layer occupancy (ticks) (Tick)
system.membus.respLayer1.utilization
                                                  0.0
# Layer utilization (Ratio)
system.membus.snoop filter.totRequests
# Total number of requests made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleRequests
# Number of requests hitting in the snoop filter with a single holder of
the requested data. (Count)
system.membus.snoop filter.hitMultiRequests
# Number of requests hitting in the snoop filter with multiple (>1)
holders of the requested data. (Count)
system.membus.snoop filter.totSnoops
# Total number of snoops made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleSnoops
# Number of snoops hitting in the snoop filter with a single holder of the
requested data. (Count)
system.membus.snoop filter.hitMultiSnoops
# Number of snoops hitting in the snoop filter with multiple (>1) holders
of the requested data. (Count)
system.workload.inst.arm
# number of arm instructions executed (Count)
system.workload.inst.quiesce
# number of quiesce instructions executed (Count)
```

----- End Simulation Statistics -----

## **Stats 4.4**

```
----- Begin Simulation Statistics -----
simSeconds
                                             3.387931
# Number of seconds simulated (Second)
simTicks
                                        3387931467000
# Number of ticks simulated (Tick)
finalTick
                                         3387931467000
# Number of ticks from beginning of simulation (restored from checkpoints
and never reset) (Tick)
                                         1000000000000
simFreq
# The number of ticks per simulated second ((Tick/Second))
hostSeconds
# Real time elapsed on the host (Second)
                                          23017532962
hostTickRate
# The number of ticks simulated per host second (ticks/s) ((Tick/Second))
hostMemory
# Number of bytes of host memory used (Byte)
simInsts
                                            36199500
# Number of instructions simulated (Count)
simOps
                                             76555494
# Number of ops (including micro ops) simulated (Count)
hostInstRate
# Simulator instruction rate (inst/s) ((Count/Second))
                                               520116
hostOpRate
# Simulator op (including micro ops) rate (op/s) ((Count/Second))
system.clk domain.clock
                                                1000
# Clock period in ticks (Tick)
system.clk domain.voltage domain.voltage
# Voltage in Volts (Volt)
                                           3387931467
system.cpu.numCycles
# Number of cpu cycles simulated (Cycle)
system.cpu.numWorkItemsStarted
# Number of work items this cpu started (Count)
system.cpu.numWorkItemsCompleted
# Number of work items this cpu completed (Count)
system.cpu.exec context.thread 0.numInsts
# Number of instructions committed (Count)
system.cpu.exec context.thread 0.numOps
                                            76555494
# Number of ops (including micro ops) committed (Count)
system.cpu.exec context.thread 0.numIntAluAccesses 76554574
# Number of integer alu accesses (Count)
system.cpu.exec context.thread 0.numFpAluAccesses
                                                          1471
# Number of float alu accesses (Count)
system.cpu.exec_context.thread_0.numVecAluAccesses
# Number of vector alu accesses (Count)
```

```
system.cpu.exec context.thread 0.numCallsReturns
                                                          373
# Number of times a function call or return occured (Count)
system.cpu.exec context.thread 0.numCondCtrlInsts
# Number of instructions that are conditional controls (Count)
system.cpu.exec context.thread 0.numIntInsts
# Number of integer instructions (Count)
system.cpu.exec context.thread 0.numFpInsts
                                                    1471
# Number of float instructions (Count)
system.cpu.exec context.thread 0.numVecInsts
                                                        0
# Number of vector instructions (Count)
system.cpu.exec context.thread 0.numIntRegReads
                                                    87007781
# Number of times the integer registers were read (Count)
system.cpu.exec context.thread 0.numIntRegWrites
                                                     58976338
# Number of times the integer registers were written (Count)
system.cpu.exec context.thread 0.numFpRegReads
# Number of times the floating registers were read (Count)
system.cpu.exec context.thread 0.numFpRegWrites
# Number of times the floating registers were written (Count)
system.cpu.exec context.thread 0.numVecRegReads
# Number of times the vector registers were read (Count)
system.cpu.exec context.thread 0.numVecRegWrites
# Number of times the vector registers were written (Count)
system.cpu.exec context.thread 0.numVecPredRegReads
# Number of times the predicate registers were read (Count)
system.cpu.exec context.thread 0.numVecPredRegWrites
# Number of times the predicate registers were written (Count)
system.cpu.exec context.thread 0.numCCRegReads
# Number of times the CC registers were read (Count)
system.cpu.exec context.thread 0.numCCRegWrites
                                                    24904504
# Number of times the CC registers were written (Count)
system.cpu.exec context.thread 0.numMiscRegReads
                                                     37276209
# Number of times the Misc registers were read (Count)
system.cpu.exec context.thread 0.numMiscRegWrites
                                                             0
# Number of times the Misc registers were written (Count)
                                                22899889
system.cpu.exec context.thread 0.numMemRefs
# Number of memory refs (Count)
system.cpu.exec context.thread 0.numLoadInsts
                                                  15574080
# Number of load instructions (Count)
system.cpu.exec context.thread 0.numStoreInsts
                                                    7325809
# Number of store instructions (Count)
system.cpu.exec context.thread 0.numIdleCycles
                                                   0.001000
# Number of idle cycles (Cycle)
system.cpu.exec_context.thread 0.numBusyCycles 3387931466.999000
# Number of busy cycles (Cycle)
system.cpu.exec context.thread 0.notIdleFraction
                                                     1.000000
# Percentage of non-idle cycles (Ratio)
```

```
system.cpu.exec context.thread 0.idleFraction
                                                0.000000
# Percentage of idle cycles (Ratio)
system.cpu.exec context.thread 0.numBranches
                                                 5126544
# Number of branches fetched (Count)
system.cpu.exec context.thread 0.statExecutedInstType::No OpClass
         0.00%
                   0.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntAlu
                                                                 53654589
          70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntMult
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::IntDiv
                                                                       28
         70.09% # Class of executed instruction. (Count)
system.cpu.exec_context.thread 0.statExecutedInstType::FloatAdd
                 70.09% # Class of executed instruction. (Count)
         0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatCmp
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatCvt
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMult
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMultAcc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::FloatDiv
       0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMisc
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatSqrt
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAdd
              70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdAddAcc
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAlu
       0.00%
                 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdCmp
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdCvt
                 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMisc
         0.00%
                 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMult
       0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdMultAcc
               70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShift
       0.00% 70.09% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::SimdShiftAcc
                70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdDiv
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSqrt
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAdd
               70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatAlu
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCmp
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatCvt
               70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatDiv
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMisc
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMult
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatMultAcc
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatSqrt
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAdd
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceAlu
               70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdReduceCmp
              70.09% # Class of executed instruction. (Count)
      0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceAdd
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdFloatReduceCmp
      0.00%
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAes
       0.00%
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdAesMix
               70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdShalHash
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha1Hash2
      0.00%
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash
      0.00% 70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdSha256Hash2
      0.00% 70.09% # Class of executed instruction. (Count)
```

```
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma2
                70.09% # Class of executed instruction. (Count)
       0.00%
system.cpu.exec context.thread 0.statExecutedInstType::SimdShaSigma3
              70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::SimdPredAlu
                70.09% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::MemRead
                        90.43% # Class of executed instruction. (Count)
15573939
            20.34%
system.cpu.exec context.thread 0.statExecutedInstType::MemWrite
             9.57%
                     100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemRead
         0.00%
                 100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::FloatMemWrite
                 100.00% # Class of executed instruction. (Count)
         0.00%
system.cpu.exec context.thread 0.statExecutedInstType::IprAccess
              100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::InstPrefetch
               100.00% # Class of executed instruction. (Count)
system.cpu.exec context.thread 0.statExecutedInstType::total
                                                               76555515
# Class of executed instruction. (Count)
system.cpu.interrupts.clk domain.clock
                                                16000
# Clock period in ticks (Tick)
system.cpu.mmu.dtb.rdAccesses
                                             15574084
# TLB accesses on read requests (Count)
system.cpu.mmu.dtb.wrAccesses
                                              7325810
# TLB accesses on write requests (Count)
system.cpu.mmu.dtb.rdMisses
                                                  421
# TLB misses on read requests (Count)
system.cpu.mmu.dtb.wrMisses
                                                28844
# TLB misses on write requests (Count)
system.cpu.mmu.dtb.walker.power state.pwrStateResidencyTicks::UNDEFINED
3387931467000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.mmu.itb.rdAccesses
                                                    0
# TLB accesses on read requests (Count)
system.cpu.mmu.itb.wrAccesses
                                             47529643
# TLB accesses on write requests (Count)
system.cpu.mmu.itb.rdMisses
                                                    0
# TLB misses on read requests (Count)
system.cpu.mmu.itb.wrMisses
                                                   56
# TLB misses on write requests (Count)
system.cpu.mmu.itb.walker.power state.pwrStateResidencyTicks::UNDEFINED
3387931467000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.cpu.power state.pwrStateResidencyTicks::ON 3387931467000
# Cumulative time (in ticks) in various power states (Tick)
```

```
system.cpu.thread 0.numInsts
                                                    0
# Number of Instructions committed (Count)
system.cpu.thread 0.numOps
                                                    0
# Number of Ops committed (Count)
system.cpu.thread 0.numMemRefs
# Number of Memory References (Count)
system.cpu.workload.numSyscalls
                                                   17
# Number of system calls (Count)
system.mem ctrl.avgPriority cpu.inst::samples 47529643.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.avgPriority cpu.data::samples 7256330.00
# Average QoS priority value for accepted requests (Count)
system.mem ctrl.priorityMinLatency
                                   0.00000022500
# per QoS priority minimum request to response latency (Second)
system.mem ctrl.priorityMaxLatency
                                        2.128645477500
# per QoS priority maximum request to response latency (Second)
system.mem ctrl.numReadWriteTurnArounds
                                                62023
# Number of turnarounds from READ to WRITE (Count)
system.mem ctrl.numWriteReadTurnArounds
# Number of turnarounds from WRITE to READ (Count)
system.mem ctrl.numStayReadState
# Number of times bus staying in READ state (Count)
system.mem ctrl.numStayWriteState
# Number of times bus staying in WRITE state (Count)
system.mem ctrl.readReqs
                                             63103726
# Number of read requests accepted (Count)
system.mem ctrl.writeReqs
                                              7325807
# Number of write requests accepted (Count)
system.mem ctrl.readBursts
                                             63103730
# Number of controller read bursts, including those serviced by the write
queue (Count)
system.mem ctrl.writeBursts
                                              7325807
# Number of controller write bursts, including those merged in the write
queue (Count)
system.mem ctrl.servicedByWrQ
                                              9310160
# Number of controller read bursts serviced by the write queue (Count)
system.mem ctrl.mergedWrBursts
                                              6333404
# Number of controller write bursts merged with an existing one (Count)
system.mem ctrl.neitherReadNorWriteReqs
# Number of requests that are neither read nor write (Count)
system.mem ctrl.avgRdQLen
# Average read queue length when enqueuing ((Count/Tick))
system.mem ctrl.avgWrQLen
# Average write queue length when enqueuing ((Count/Tick))
system.mem ctrl.numRdRetry
# Number of times read queue was full causing retry (Count)
```

```
system.mem ctrl.numWrRetry
# Number of times write queue was full causing retry (Count)
system.mem ctrl.readPktSize::0
                                              1001233
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::1
                                                    19
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::2
                                             14571444
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::3
                                              47531034
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::4
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::5
                                                     0
# Read request sizes (log2) (Count)
system.mem ctrl.readPktSize::6
# Read request sizes (log2) (Count)
system.mem ctrl.writePktSize::0
                                               3122099
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::1
                                                     3
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::2
                                               4201939
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::3
                                                  1766
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::4
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.writePktSize::5
# Write request sizes (log2) (Count)
system.mem_ctrl.writePktSize::6
                                                     0
# Write request sizes (log2) (Count)
system.mem ctrl.rdQLenPdf::0
                                              53793562
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::1
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::2
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::3
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::4
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::5
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::6
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::7
# What read queue length does an incoming req see (Count)
```

```
system.mem ctrl.rdQLenPdf::8
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::9
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::10
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::11
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::12
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::13
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::14
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::15
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::16
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::17
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::18
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::19
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::20
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::21
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::22
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::23
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::24
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::25
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::26
# What read queue length does an incoming reg see (Count)
system.mem ctrl.rdQLenPdf::27
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::28
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::29
# What read queue length does an incoming req see (Count)
system.mem ctrl.rdQLenPdf::30
# What read queue length does an incoming req see (Count)
```

```
system.mem ctrl.rdQLenPdf::31
# What read queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::0
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::1
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::2
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::3
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::4
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::5
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::6
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::7
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::8
                                                    1
# What write queue length does an incoming req see (Count)
system.mem_ctrl.wrQLenPdf::9
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::10
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::11
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::12
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::13
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::14
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::15
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::16
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::17
                                                62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::18
                                                 62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::19
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::20
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::21
                                                 62024
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::22
                                                 62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::23
                                                62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::24
                                                 62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::25
                                                62024
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::26
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::27
                                                 62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::28
                                                62024
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::29
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::30
                                                62024
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::31
                                                 62024
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::32
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::33
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::34
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::35
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::36
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::37
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::38
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::39
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::40
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::41
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::42
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::43
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::44
# What write queue length does an incoming req see (Count)
```

```
system.mem ctrl.wrQLenPdf::45
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::46
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::47
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::48
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::49
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::50
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::51
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::52
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::53
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::54
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::55
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::56
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::57
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::58
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::59
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::60
# What write queue length does an incoming reg see (Count)
system.mem ctrl.wrQLenPdf::61
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::62
# What write queue length does an incoming req see (Count)
system.mem ctrl.wrQLenPdf::63
# What write queue length does an incoming reg see (Count)
system.mem ctrl.rdPerTurnAround::samples
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::mean
                                          867.307160
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::gmean 304.355664
# Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::stdev 73227.667422
# Reads before turning the bus around for writes (Count)
```

```
system.mem ctrl.rdPerTurnAround::0-1.04858e+06 62022
                                                               100.00%
100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::1.78258e+07-1.88744e+07
       100.00% # Reads before turning the bus around for writes (Count)
system.mem ctrl.rdPerTurnAround::total
                                                62023
# Reads before turning the bus around for writes (Count)
system.mem ctrl.wrPerTurnAround::samples
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::mean
                                          16.000048
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::gmean
                                           16.000044
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::stdev
                                             0.012046
# Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::16
                                                62022
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::19
                                                           0.00%
100.00% # Writes before turning the bus around for reads (Count)
system.mem ctrl.wrPerTurnAround::total
                                                62023
# Writes before turning the bus around for reads (Count)
system.mem ctrl.bytesReadWrQ
# Total number of bytes read from write queue (Byte)
system.mem ctrl.bytesReadSys
                                           439535306
# Total read bytes from the system interface side (Byte)
system.mem ctrl.bytesWrittenSys
                                             19943987
# Total written bytes from the system interface side (Byte)
system.mem ctrl.avgRdBWSys
                                        129735595.38652852
# Average system read bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.avgWrBWSys
                                         5886774.03727423
# Average system write bandwidth in Byte/s ((Byte/Second))
system.mem ctrl.totGap
                                         3387931331000
# Total gap between requests (Tick)
system.mem ctrl.avgGap
                                             48103.84
# Average gap between requests ((Tick/Count))
system.mem ctrl.requestorReadBytes::cpu.inst
                                               380237144
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorReadBytes::cpu.data
                                               22056285
# Per-requestor bytes read from memory (Byte)
system.mem ctrl.requestorWriteBytes::cpu.data
                                                  1163629
# Per-requestor bytes write to memory (Byte)
system.mem ctrl.requestorReadRate::cpu.inst 112232832.246957615018
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorReadRate::cpu.data 6510251.229943194427
# Per-requestor bytes read from memory rate ((Byte/Second))
system.mem ctrl.requestorWriteRate::cpu.data 343462.968874747923
# Per-requestor bytes write to memory rate ((Byte/Second))
```

```
system.mem ctrl.requestorReadAccesses::cpu.inst
                                                  47529643
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorReadAccesses::cpu.data
                                                    15574087
# Per-requestor read serviced memory accesses (Count)
system.mem ctrl.requestorWriteAccesses::cpu.data
                                                      7325807
# Per-requestor write serviced memory accesses (Count)
system.mem ctrl.requestorReadTotalLat::cpu.inst 1224887811000
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorReadTotalLat::cpu.data 182313768000
# Per-requestor read total memory access latency (Tick)
system.mem ctrl.requestorWriteTotalLat::cpu.data 88885120788000
# Per-requestor write total memory access latency (Tick)
system.mem ctrl.requestorReadAvgLat::cpu.inst
                                               25771.03
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorReadAvgLat::cpu.data
                                                 11706.23
# Per-requestor read average memory access latency ((Tick/Count))
system.mem ctrl.requestorWriteAvgLat::cpu.data 12133150.76
# Per-requestor write average memory access latency ((Tick/Count))
system.mem ctrl.dram.bytesRead::cpu.inst
                                            380237144
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::cpu.data
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesRead::total
                                            439535306
# Number of bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::cpu.inst 380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesInstRead::total
                                             380237144
# Number of instructions bytes read from this memory (Byte)
system.mem ctrl.dram.bytesWritten::cpu.data
                                                19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.bytesWritten::total
                                             19943987
# Number of bytes written to this memory (Byte)
system.mem ctrl.dram.numReads::cpu.inst
                                          47529643
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::cpu.data
                                           15574083
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numReads::total
                                             63103726
# Number of read requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::cpu.data
                                              7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.numWrites::total
                                             7325807
# Number of write requests responded to by this memory (Count)
system.mem ctrl.dram.bwRead::cpu.inst
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwRead::cpu.data
                                             17502763
# Total read bandwidth from this memory ((Byte/Second))
```

```
system.mem ctrl.dram.bwRead::total
                                           129735595
# Total read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::cpu.inst 112232832
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwInstRead::total
                                            112232832
# Instruction read bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::cpu.data
                                              5886774
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwWrite::total
# Write bandwidth from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.inst
                                          112232832
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::cpu.data
                                             23389537
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.bwTotal::total
# Total bandwidth to/from this memory ((Byte/Second))
system.mem ctrl.dram.readBursts
                                            53793570
# Number of DRAM read bursts (Count)
system.mem ctrl.dram.writeBursts
                                               992371
# Number of DRAM write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::0
                                              126621
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::1
                                              126555
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::2
                                               127943
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::3
                                               126552
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::4
                                               126701
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::5 40486923
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::6
                                             7284384
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankRdBursts::7
                                              5387891
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::0
                                              118186
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::1
                                              116867
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::2
                                               116664
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::3
                                              116551
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::4
                                             116808
# Per bank write bursts (Count)
```

```
system.mem ctrl.dram.perBankWrBursts::5
                                              116455
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::6
                                               118233
# Per bank write bursts (Count)
system.mem ctrl.dram.perBankWrBursts::7
                                               172607
# Per bank write bursts (Count)
system.mem ctrl.dram.totQLat
                                         196846254000
# Total ticks spent queuing (Tick)
system.mem ctrl.dram.totBusLat
                                         403451775000
# Total ticks spent in databus transfers (Tick)
system.mem ctrl.dram.totMemAccLat
                                         1407201579000
# Total ticks spent from burst creation until serviced by the DRAM (Tick)
system.mem ctrl.dram.avgQLat
                                              3659.29
# Average queueing delay per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgBusLat
# Average bus latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.avgMemAccLat
                                             26159.29
# Average memory access latency per DRAM burst ((Tick/Count))
system.mem ctrl.dram.readRowHits
                                             48755173
# Number of row buffer hits during reads (Count)
system.mem ctrl.dram.writeRowHits
# Number of row buffer hits during writes (Count)
system.mem ctrl.dram.readRowHitRate
                                                90.63
# Row buffer hit rate for reads (Ratio)
system.mem ctrl.dram.writeRowHitRate
                                                81.97
# Row buffer hit rate for writes (Ratio)
system.mem ctrl.dram.bytesPerActivate::samples
                                                    5217285
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::mean
                                              336.027119
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::gmean
                                               262.139173
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::stdev 176.764011
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::0-63
                                                  454273
                                                              8.71%
8.71% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::64-127
                                                                5.60%
                                                    291986
14.30% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::128-191
                                                     629921
                                                                12.07%
26.38% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::192-255
                                                     679885
                                                                13.03%
39.41% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::256-319
                                                     166639
                                                                 3.19%
42.60% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::320-383
                                                     478304
                                                                 9.17%
51.77% # Bytes accessed per row activation (Byte)
```

```
system.mem ctrl.dram.bytesPerActivate::384-447
                                                     230113
                                                                4.41%
56.18% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::448-511
                                                      25557
                                                                 0.49%
56.67% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::512-575
                                                    2260607
                                                                43.33%
100.00% # Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesPerActivate::total
                                                 5217285
# Bytes accessed per row activation (Byte)
system.mem ctrl.dram.bytesRead
                                           1721394240
# Total bytes read (Byte)
system.mem ctrl.dram.bytesWritten
                                             31755872
# Total bytes written (Byte)
system.mem ctrl.dram.avgRdBW
                                           508.095945
# Average DRAM read bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.avgWrBW
                                             9.373233
# Average DRAM write bandwidth in MiBytes/s ((Byte/Second))
system.mem ctrl.dram.peakBW
                                              4266.00
# Theoretical peak bandwidth in MiByte/s ((Byte/Second))
system.mem ctrl.dram.busUtil
                                                12.13
# Data bus utilization in percentage (Ratio)
system.mem ctrl.dram.busUtilRead
                                                11.91
# Data bus utilization in percentage for reads (Ratio)
system.mem ctrl.dram.busUtilWrite
                                                 0.22
# Data bus utilization in percentage for writes (Ratio)
system.mem ctrl.dram.pageHitRate
                                                90.48
# Row buffer hit rate, read and write combined (Ratio)
system.mem ctrl.dram.power state.pwrStateResidencyTicks::UNDEFINED
3387931467000
                                    # Cumulative time (in ticks) in
various power states (Tick)
                                         15870651838.931707
system.mem ctrl.dram.rank0.actEnergy
# Energy for activate commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preEnergy
                                        5590692348.189857
# Energy for precharge commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.readEnergy
                                        92399364690.435654
# Energy for read commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.writeEnergy 1530307532.710258
# Energy for write commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.refreshEnergy 24220584765.927349
# Energy for refresh commands per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actBackEnergy 135013861347.384048
# Energy for active background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.preBackEnergy 2148532790.391415
# Energy for precharge background per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.actPowerDownEnergy
# Energy for active power-down per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.prePowerDownEnergy
# Energy for precharge power-down per rank (pJ) (Joule)
```

```
system.mem ctrl.dram.rank0.selfRefreshEnergy
                                                         0
# Energy for self refresh per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.totalEnergy 276773995313.910522
# Total energy per rank (pJ) (Joule)
system.mem ctrl.dram.rank0.averagePower
                                            81.694095
# Core power per rank (mW) (Watt)
system.mem ctrl.dram.rank0.totalIdleTime
# Total Idle time Per DRAM Rank (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::IDLE 21526133500
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::REF 113367020000
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::SREF
                                                         0
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::PRE PDN
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT 3253038313500
# Time in different power states (Tick)
system.mem ctrl.dram.rank0.pwrStateTime::ACT PDN
                                                             0
# Time in different power states (Tick)
system.mem ctrl.power state.pwrStateResidencyTicks::UNDEFINED
3387931467000
                                    # Cumulative time (in ticks) in
various power states (Tick)
system.membus.transDist::ReadReg
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::ReadResp
                                             63103710
# Transaction distribution (Count)
system.membus.transDist::WriteReq
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::WriteResp
                                              7325791
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadReg
                                                    16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWReadResp
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteReq
                                                     16
# Transaction distribution (Count)
system.membus.transDist::LockedRMWWriteResp
                                                      16
# Transaction distribution (Count)
system.membus.pktCount system.cpu.icache port::system.mem ctrl.port
                               # Packet count per connected requestor and
95059286
responder (Count)
system.membus.pktCount system.cpu.icache port::total
# Packet count per connected requestor and responder (Count)
system.membus.pktCount system.cpu.dcache port::system.mem ctrl.port
45799780
                               # Packet count per connected requestor and
responder (Count)
```

```
system.membus.pktCount system.cpu.dcache port::total
                                                          45799780
# Packet count per connected requestor and responder (Count)
system.membus.pktCount::total
                                            140859066
# Packet count per connected requestor and responder (Count)
system.membus.pktSize system.cpu.icache port::system.mem ctrl.port
380237144
                                # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.icache port::total
                                                        380237144
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::system.mem ctrl.port
79242149
                               # Cumulative packet size per connected
requestor and responder (Byte)
system.membus.pktSize system.cpu.dcache port::total
                                                         79242149
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.pktSize::total
                                            459479293
# Cumulative packet size per connected requestor and responder (Byte)
system.membus.snoops
# Total snoops (Count)
system.membus.snoopTraffic
                                                     0
# Total snoop traffic (Byte)
system.membus.snoopFanout::samples
                                             70429533
# Request fanout histogram (Count)
system.membus.snoopFanout::mean
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::stdev
                                                     0
# Request fanout histogram (Count)
system.membus.snoopFanout::underflows
                                                            0.00%
0.00% # Request famout histogram (Count)
system.membus.snoopFanout::0
                                             70429533
                                                          100.00%
100.00% # Request fanout histogram (Count)
system.membus.snoopFanout::1
                                                     \cap
                                                            0.00%
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::overflows
                                                            0.00%
                                                     0
100.00% # Request famout histogram (Count)
system.membus.snoopFanout::min value
                                                     \Omega
# Request fanout histogram (Count)
system.membus.snoopFanout::max value
# Request fanout histogram (Count)
system.membus.snoopFanout::total
                                             70429533
# Request fanout histogram (Count)
system.membus.power state.pwrStateResidencyTicks::UNDEFINED 3387931467000
# Cumulative time (in ticks) in various power states (Tick)
system.membus.reqLayer2.occupancy
                                         77755340000
# Layer occupancy (ticks) (Tick)
                                                   0.0
system.membus.reqLayer2.utilization
# Layer utilization (Ratio)
```

```
118807065000
system.membus.respLayer0.occupancy
# Layer occupancy (ticks) (Tick)
system.membus.respLayer0.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.respLayer1.occupancy 41604287000
# Layer occupancy (ticks) (Tick)
system.membus.respLayer1.utilization
                                                 0.0
# Layer utilization (Ratio)
system.membus.snoop filter.totRequests
# Total number of requests made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleRequests
# Number of requests hitting in the snoop filter with a single holder of
the requested data. (Count)
system.membus.snoop filter.hitMultiRequests
# Number of requests hitting in the snoop filter with multiple (>1)
holders of the requested data. (Count)
system.membus.snoop filter.totSnoops
# Total number of snoops made to the snoop filter. (Count)
system.membus.snoop filter.hitSingleSnoops
# Number of snoops hitting in the snoop filter with a single holder of the
requested data. (Count)
system.membus.snoop filter.hitMultiSnoops
# Number of snoops hitting in the snoop filter with multiple (>1) holders
of the requested data. (Count)
system.workload.inst.arm
                                                   0
# number of arm instructions executed (Count)
system.workload.inst.quiesce
# number of quiesce instructions executed (Count)
----- End Simulation Statistics -----
```