

An 88% Efficiency $2.4\mu\text{W}$ to $15.6\mu\text{W}$ Triboelectric Nanogenerator Energy Harvesting System Based on a Single-Comparator Control Algorithm

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Abstract— This paper presents an energy harvesting system (EHS) based on a triboelectric nanogenerator (TENG). A novel TENG HDL spice model was developed to optimize the proposed ultra-low power (ULP) EHS. The proposed TENG-EHS utilizes a novel single-comparator-control (SCC) algorithm for improving the power conversion efficiency (PCE). It modulates the switching frequency of the implemented switched capacitor charge pump (SCCP) in proportion to the load condition at a given applied vibration frequency (i.e. excitation frequency). Moreover, a novel hysteresis control technique was introduced. It regulates the input voltage at the maximum possible power point without IC breakdown, and adopts a dropout excess charge storage technique. The fabricated test chip in 65-nm CMOS technology achieves a peak PCE of 88% with $2.4\mu\text{W}$ to $15.6\mu\text{W}$ input power and power density of $39.59\mu\text{W}/\text{mm}^2$.

I. INTRODUCTION

The rapid growth of ultra-low power applications including IoT devices, implantable sensors, and wireless electronics raises the call for fully-autonomous power management circuit (PMC) design. In these applications, energy harvesters aim to assist or remove batteries as primary energy sources for PMC [1, 2]. Various energy harvesting devices such as photovoltaic (PV) cells, thermoelectric generators (TEG), and piezoelectric devices have been explored. Piezoelectric devices have been widely utilized for harvesting mechanical energy.

Recently, as a newly introduced mechanical energy scavenger, TENG has been excessively studied from the material engineering point of view. It has been demonstrated to harvest energy from horizontal, vertical, and rotational vibrations. Compared with piezoelectric transducers, which suffer from complex fabrication and high-cost [3], TENG has the features of simple fabrication, low cost, high flexibility, low weight, and small size [3], which makes it a promising power source. Moreover, it supports several harvesting modes [3, 4], allowing it to be employed as an adequate candidate for EHS for IoT applications. Fig. 1 illustrates how a TENG device operates. It generates electric power based on the coupling of triboelectrification and electrostatic induction using two materials with relatively opposite triboelectric (TE) properties, as explained in [3, 4]. The first TENG-EHS in an integrated circuit form was presented in [5]. It proposes a dual-input rectifier with a maximum power point tracking (MPPT) circuit. Although it achieves a 97% tracking efficiency, the control circuit suffers from modest power conversion efficiency (PCE)

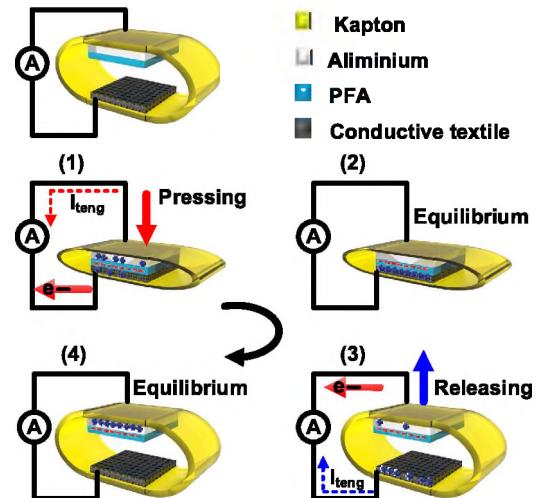


Fig. 1. The fabricated vertical contact TENG harvesting mechanism.

of 51.1%. This limited PCE stems from the high internal impedance (hundreds of $\text{M}\Omega$) and the limited output current ($<5\mu\text{A}$) of the TENG device. These undesirable characteristics entails the design of a smart control circuit that minimizes the intolerable conduction and switching losses within the implemented switched capacitor charge pump (SCCP) with minimum power consumption.

This work presents a novel TENG-EHS for harvesting energy from a fabricated vertical contact mode TENG device (Fig. 1). A conduction loss reduction technique is developed using an ULP single-comparator-control (SCC) algorithm. It follows a voltage conversion ratio (VCR) self-correction algorithm by modulating the SCCP switching frequency (f_{sw}) with respect to the load condition. The control circuit shows a 36% PCE improvement compared with [5]. Furthermore, a hysteresis-input-regulation-control (HIRC) technique is proposed for excess charge storage and input voltage regulation around the maximum possible power point. This minimizes tracking efficiency degradation, and prevents the EHS from breakdown due to high voltage. In addition, a HDL-based spice model of the employed TENG device has been developed. The developed spice model facilitates the optimization of the proposed TENG-EHS at various operating points. Experimental results demonstrate that the developed spice model shows high accuracy.

II. TENG CHARACTERIZATION AND SPICE MODEL

Fig. 2 shows the TENG output AC waveforms (V_{teng}) and their uneven peak values (i.e. V_{pos} and V_{neg}) which depend on the pressure and the TE materials, while V_{teng} frequency depends on f_{ex} . A characterization circuit was developed, as depicted in Fig. 2, to study the output characteristics of the TENG with the variation of f_{ex} under different load values (i.e. Z_{load}). In this work, a conventional full-wave rectifier (FWR) was employed to convert V_{teng} to a regulated DC-value (V_{rect}). The P-V characteristic curves, shown in Fig. 3, can be generated by varying Z_{load} from zero to ∞ . It can be shown that the TENG acts as a current limited voltage source. In addition, at a certain f_{ex} , the maximum power point voltage (V_{mpp}), at which the tracking efficiency is maximized, exceeds 30 V, which mandates high voltage (HV) technology process to regulate V_{rect} near V_{mpp} .

By investigating the theoretical model (Fig. 4 (a)) presented in [6], V_{teng} can be obtained as follows.

$$V_{teng}(t) = -\frac{Q}{S\epsilon_0} \left[\frac{d_1}{\epsilon_{r1}} + x(t) \right] + \frac{\sigma}{\epsilon_0} x(t) \quad (1)$$

Here, d_1 and S are the dielectric thickness and area respectively. While ' ϵ_{r1} ' and ' ϵ_0 ' are the dielectric constant and the air permittivity respectively. Q and $x(t)$ are the charges transferred and the time-variant distance between the two electrodes, respectively. V_{teng} can be further simplified based on the conventional model in [7] (Fig. 4 (b)) as follows

$$V_{teng}(t) = -\frac{Q}{C_{TENG}(x(t))} + V_{oc}(x(t)) \quad (2)$$

where C_{TENG} and V_{oc} are the time-variant capacitor and the open-circuit voltage within the TENG, respectively. Based on (2), V_{oc} and C_{TENG} are time-variant components and function of $x(t)$, defining V_{teng} value at a given time. Utilizing this information for TENG spice modelling and following (1) and (2), Fig. 4 (c) demonstrates the proposed TENG HDL-based spice model. Firstly, $x(t)$ is generated and varies with f_{ex} . Secondly, C_{TENG} and V_{oc} are calculated simultaneously based on (1) and using $x(t)$, as shown in Fig. 4 (c), to generate proper values for V_{teng} and TENG output current (I_{cap}). The experimental and the simulated results of the fabricated TENG and its proposed spice model, respectively, shown in Fig. 5, verify the accuracy of the deduced HDL spice model.

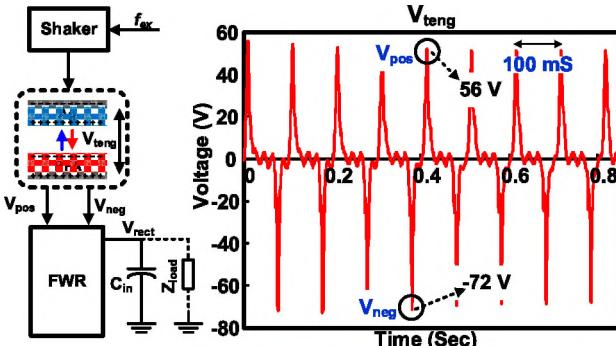


Fig. 2. TENG characterization circuit and AC output waveforms.

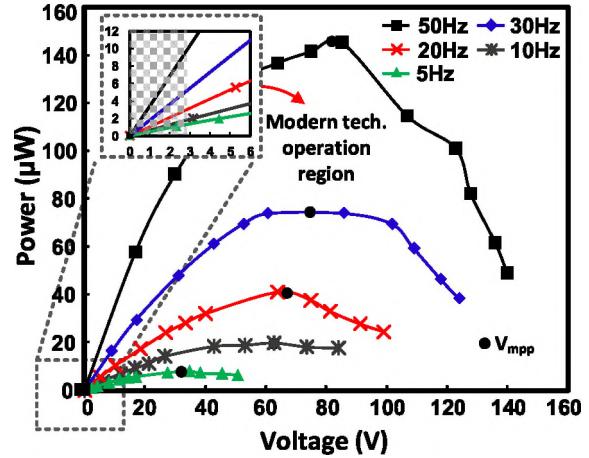


Fig. 3. Experimental P-V characteristic curves at different f_{ex} .

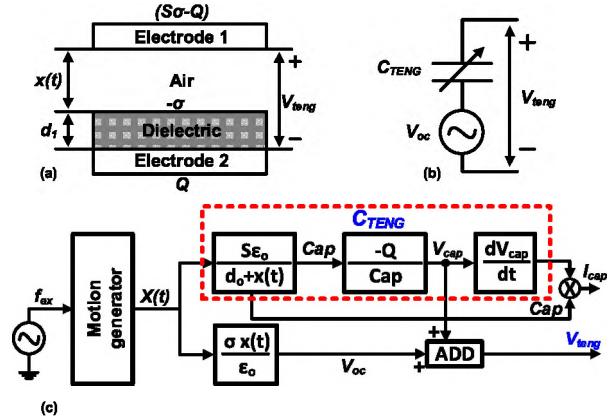


Fig. 4. TENG block diagram of (a) theoretical model, (b) conventional electrical model, and (c) proposed HDL spice model.

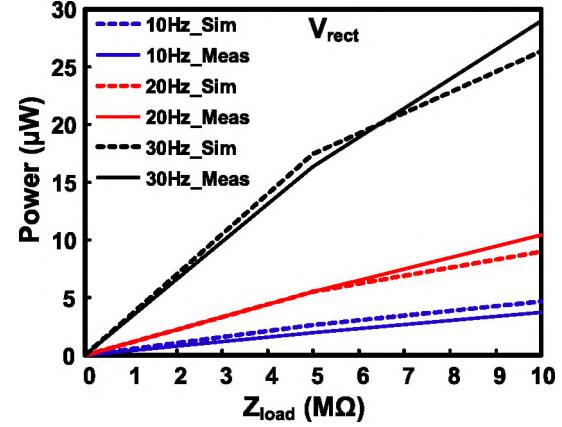


Fig. 5. The measured and simulated V_{rect} across different Z_{load} .

III. TENG-EHS ARCHITECTURE AND CIRCUIT IMPLEMENTATION

The proposed TENG-EHS architecture, shown in Fig. 6 comprises four main blocks, namely a doubler SCCP, dynamic latched comparators for the SCC algorithm and HIRC implementation, an excess energy storage circuit, and a digital core for executing the proposed SCC and HIRC algorithms. The

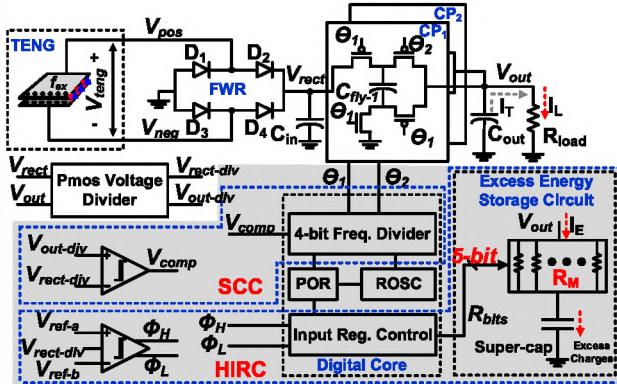


Fig. 6. Proposed TENG-EHS top architecture.

HV limitation of the employed 65-nm CMOS technology prevents V_{rect} from operating near V_{mpp} described in Fig. 3. Hence, the proposed TENG-EHS adopts a HIRC technique that maintains V_{rect} at the maximum power point within the technology operation region ($V_{mpp\text{-max}}$) depicted in Fig. 3. Moreover, HIRC reduces the harvested energy loss by developing an excess energy storage circuit. For a non-isolating TENG-EHS, the V_{rect} value is defined by the total output current (I_T) and f_{ex} . I_T is composed of load current (I_L) and excess charges storage current (I_E) (Fig. 6). The I_E flow rate is controlled by altering the total resistance R_M , which consists of a binary-weighted resistor matrix set by 5-bit digital signal (R_{bits}). Hence, the proposed HIRC regulates V_{rect} around $V_{mpp\text{-max}}$ by indirectly modulating I_E through R_{bits} with respect to I_L and f_{ex} variations. Fig. 7 (a) describes the proposed HIRC block diagram. The outputs of the two latched comparators (Φ_H and Φ_L) are stored in a 2-bit register and fed to a 5-bit counter. The later controls the R_M value through a 5-bit digital signal (R_{bits}). Following the logic table in Fig. 7 (b), at light I_L and/or high f_{ex} , $V_{rect\text{-div}}$ goes above V_{ref-a} (i.e. $\Phi_H=0$, and $\Phi_L=1$), hence the 5-bit counter decrements R_{bits} so that R_M decreases (i.e. I_E increases) to compensate for the decrease in I_L or the increase in f_{ex} . Likewise, at high I_L and/or low f_{ex} , $V_{rect\text{-div}}$ drops below V_{ref-b} , then R_{bits} increments to decrease I_E . Finally, at both scenarios, I_E is used to store the excess charges in a supercapacitor. A part of the stored energy is lost in R_M due to the HV limitation of the process technology while maintaining V_{rect} near $V_{mpp\text{-max}}$.

A doubler SCCP with a gain of 0.5 is implemented to provide a regulated output voltage (V_{out}) at ~1.2 V. Due to the limited power around $V_{mpp\text{-max}}$ (Fig. 3), an SCC algorithm was proposed to minimize the conduction and switching losses within the SCCP, and improve the PCE. Basically, for efficient harvested power conversion, the VCR (i.e. 0.5) must be kept constant across various load conditions. When the VCR deviates from 0.5 due to a variation in I_L , the SCCP f_{sw} must be adjusted to avoid unnecessary high f_{sw} at light loads (i.e. switching loss) and insufficient f_{sw} (i.e. conduction loss) at heavy loads. Thus, the SCC algorithm adopts a proposed event/time driven technique. It consists of a single-comparator that compares V_{out} with V_{rect}

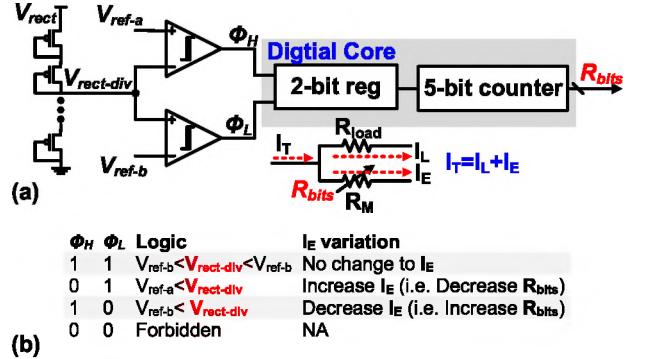


Fig. 7. HIRC (a) block diagram, and (b) truth and logic table.

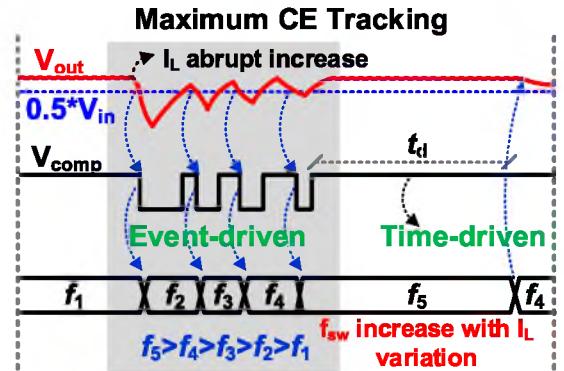


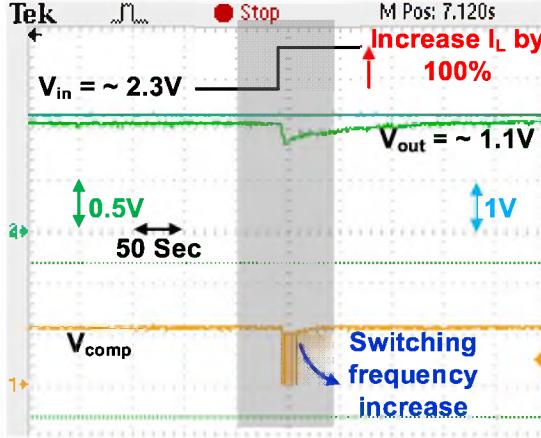
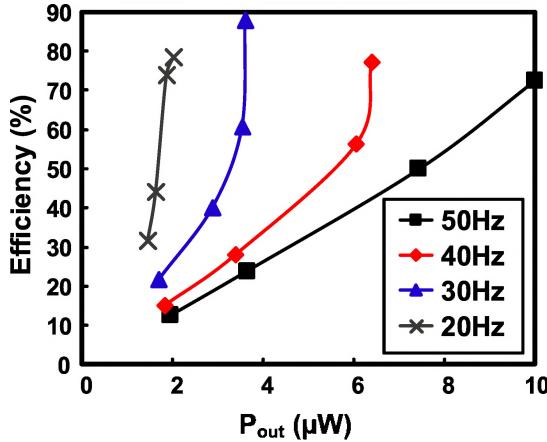
Fig. 8. Proposed single-comparator control timing diagram.

after an appropriate voltage division (Fig. 6), followed by a 4-bit frequency divider. The 4-bit frequency divider divides the ring oscillator (ROSC) output frequency by a 4-bit digital value ‘N’. Finally, ‘N’ is set, according to ‘ V_{comp} ’ (Fig. 6) to modulate f_{sw} in proportion to I_L variation, adjusting the VCR to 0.5. Following the timing diagram depicted in Fig. 8, if $V_{out} < 0.5V_{rect}$, ‘N’ is decremented one bit per V_{comp} negative edge (event-driven), increasing f_{sw} . Likewise, If $V_{out} > 0.5V_{rect}$, f_{sw} is decreased by incrementing ‘N’ one bit after a defined time ‘ t_d ’ (time-driven). At steady state, V_{out} oscillates around $0.5V_{rect}$. Thus, PCE along with the voltage conversion efficiency (VCE) can be increasingly improved.

IV. MEASUREMENTS RESULTS

The proposed TENG-EHS was designed and fabricated in 65-nm CMOS process. Fig. 9 shows the performance of the proposed SCC algorithm. When I_L increases, the comparator transmits its pulses to the 4-bit frequency divider (Fig. 6), to modulate f_{sw} accordingly, maintaining the VCR around 0.5. f_{sw} increases one step per V_{comp} negative edge to restore V_{out} to its regulated value (Fig. 8), improving the PCE as well as the VCE.

The PCE values at different f_{ex} across the output power range of the proposed TENG-EHS are recorded in Fig. 10. The tested TENG-EHS chip achieves a peak PCE of 88% at f_{ex} 30 Hz. The PCE results validates the implemented SCC algorithm for minimizing the conduction and the switching losses within the SCCP. Moreover, the ultra-low power consumption of the

Fig. 9. The proposed SCC algorithm response at I_L variation.Fig. 10. Power conversion efficiency at different f_{ex} across the load range

dynamic comparators, the voltage dividers, and the digital core boosts the PCE across the output power range.

Fig. 11 shows the test chip microphotography along with a comparison table with the TENG-EHS prior art in literature [5]. The proposed TENG-EHS occupies a silicon area of 0.394 mm^2 and exhibits a peak PCE of 88%, showing an almost a 36% improvement compared with [5]. In addition, it shows a $39.59 \mu\text{W/mm}^2$ power density while the prior work in [5] achieves $7.3 \mu\text{W/mm}^2$. Fig. 12 illustrates the measurement setup of the proposed TENG-EHS. A power amplifier is used to accurately control the f_{ex} and the pressure of the vibration generated by a commercial mini-shaker. It agitates one plate of the TENG while the other plate is fixed on a horizontal surface.

V. CONCLUSION

This work proposes a TENG-EHS with a ULP control circuit. Firstly, a TENG spice model is developed for optimizing the proposed EHS. In addition, a novel SCC algorithm is proposed to reduce the losses within the SCCP, and improve the PCE and VCE. The proposed TENG-EHS achieves a peak PCE of 88% with 36% improvement over prior art. Finally, a HIRC algorithm was developed to prevent the fabricated chip from

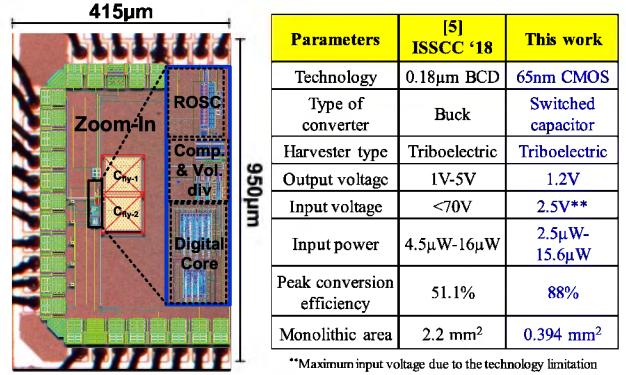


Fig. 11. TENG-EHS die photo and comparison table with Prior Arts.

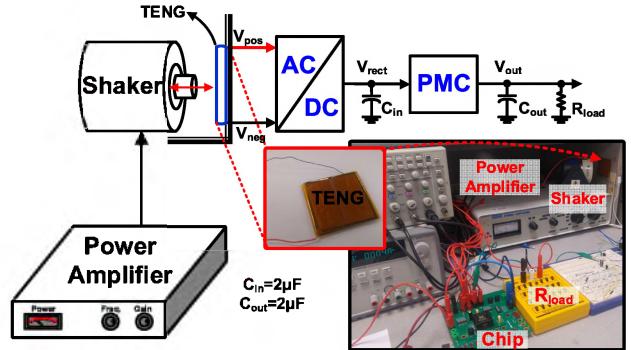


Fig. 12. Measurement setup of the tested TENG-EHS.

breakdown and store the excess TENG harvested energy. The implemented digital core is synthesized and applicable to any CMOS technology.

REFERENCES

- [1] K. Rawy, T. Yoo, and T. T. H. Kim, "An 88% Efficiency 0.1-300- μW Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes," *IEEE Journal of Solid-State Circuits*, pp. 1-12, 2018.
- [2] X. Liu and E. Sánchez-Sinencio, "An 86% Efficiency 12 μW Self-Sustaining PV Energy Harvesting System With Hysteresis Regulation and Time-Domain MPPT for IOT Smart Nodes," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 1424-1437, 2015.
- [3] R. Hinche, W. Seung, and S.-W. Kim, "Recent Progress on Flexible Triboelectric Nanogenerators for SelfPowered Electronics," *ChemSusChem*, vol. 8, pp. 2327-2344, 2015.
- [4] Z. L. Wang, "Triboelectric Nanogenerators as New Energy Technology for Self-Powered Systems and as Active Mechanical and Chemical Sensors," *ACS Nano*, vol. 7, pp. 9533-9557, 2013/11/26 2013.
- [5] I. Park, J. Maeng, D. Lim, M. Shim, J. Jeong, and C. Kim, "A 4.5-to-16 μW Integrated Triboelectric EnergyHarvesting System Based on High-Voltage Dual-Input Buck Converter with MPPT and 70V Maximum Input Voltage," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 146-148.
- [6] S. Niu, S. Wang, L. Lin, Y. Liu, Y. Sheng Zhou, Y. Hu, et al., *Theoretical study of contact-mode triboelectric nanogenerators as an effective power source* vol. 6, 2013.
- [7] S. Niu, Y. Liu, Y. S. Zhou, S. Wang, L. Lin, and Z. L. Wang, "Optimization of Triboelectric Nanogenerator Charging Systems for Efficient Energy Harvesting and Storage," *IEEE Transactions on Electron Devices*, vol. 62, pp. 641-647, 2015.