CSIE 2344, Spring 2019 — Homework 4

Due June 3 (Monday) at Noon

There are 96 points in total. Points will be deducted if no appropriate intermediate step is provided.

When you submit your homework on Gradescope, please select the corresponding page(s) of each problem.

1 Counter (36pts)

Design a 3-bit counter which counts CBA in the sequence: 001, 011, 010, 110, 111, 101, 100, and repeats.

1. (6pts) Use D flip-flops. Derive a minimum sum-of-products expression for D_C.
2. (6pts) Use T flip-flops. Derive a minimum sum-of-products expression for T_C.
3. (12pts) Use S-R flip-flops. Derive a minimum sum-of-products expression for S_B and R_B.
4. (12pts) Use J-K flip-flops. Derive a minimum sum-of-products expression for J_A and K_A.

Answer: The truth table and the Karnaugh maps of C^+, B^+, A^+ are shown in Figure 1.

C	B	A	C^+	B^+	A^+
0	0	0	X	X	X
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	1

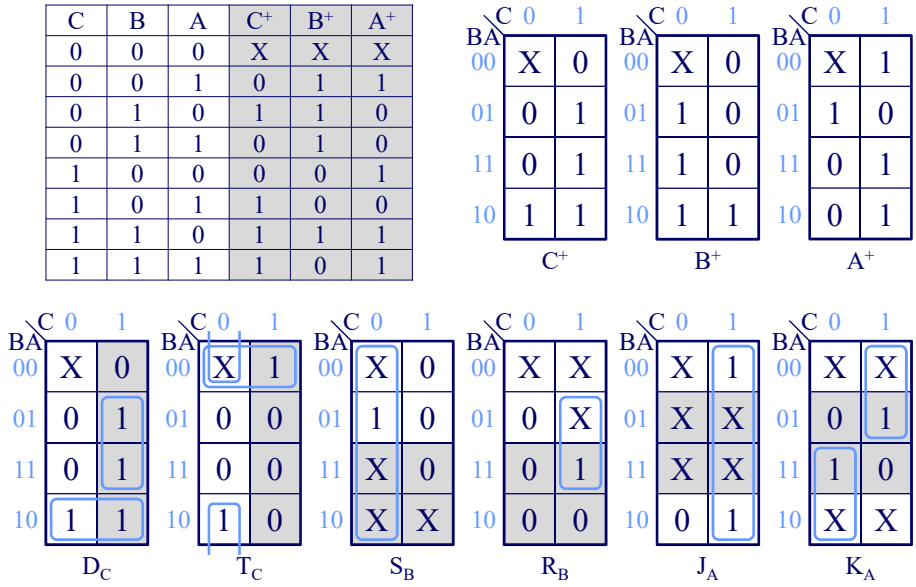


Figure 1: The Karnaugh maps.

1. The Karnaugh map of D_C is shown in Figure 1. It is derived from the Karnaugh map of C^+ without any change, and we get $D_C = CA + BA'$.

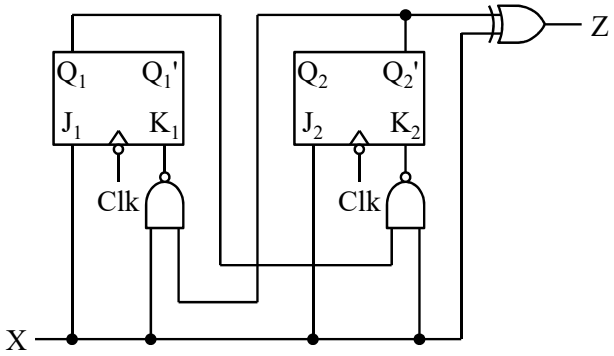
2. The Karnaugh map of T_C is shown in Figure 1. It is derived from the Karnaugh map of C^+ by complementing the $C = 1$ half, and we get $T_C = C'A' + B'A'$.

3. The Karnaugh maps of S_B and R_B are shown in Figure 1. They are derived from the Karnaugh map of B^+ by "replacing 1's with X's for the $B = 1$ half" and "replacing 0's with X's and 1's with 0's for the $B = 0$ half and complementing the $B = 1$ half", respectively. As a result, we get $S_B = C'$ and $R_B = CA$.

4. The Karnaugh maps of J_A and K_A are shown in Figure 1. They are derived from the Karnaugh map of A^+ by "filling in with X's for the $A = 1$ half" and "filling in with X's for the $A = 0$ half and complementing the $A = 1$ half", respectively. As a result, we get $J_A = C$ and $K_A = C'B + CB'$.

2 State Table and State Graph Construction (12pts)

Given the following circuit,



1. (6pts) Construct the state table.

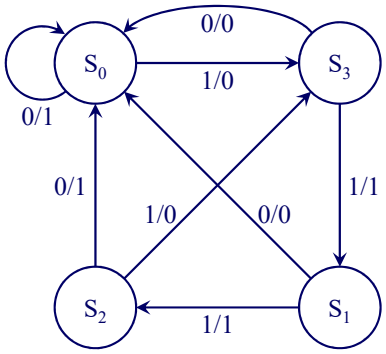
2. (6pts) Construct the state graph.

Answer:

1. $Q_1^+ = J_1Q_1' + K_1'Q_1 = XQ_1' + XQ_2'Q_1$, $Q_2^+ = J_2Q_2' + K_2'Q_2 = XQ_2' + XQ_1Q_2$, and $Z = XQ_2 + X'Q_2'$, so the state table is shown below.

Present State Q_1Q_2	Next State $Q_1^+Q_2^+$		Z	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00 (S_0)	00	11	1	0
01 (S_1)	00	10	0	1
10 (S_2)	00	11	1	0
11 (S_3)	00	01	0	1

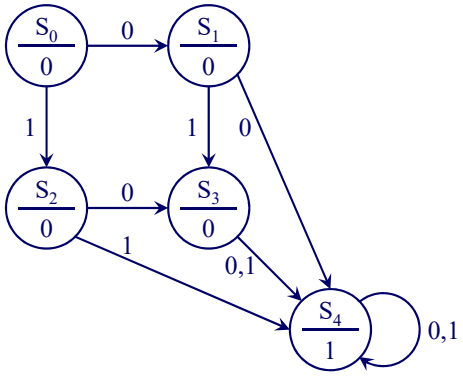
2. The state graph is shown below.



3 State Graph Derivation (6pts)

A sequential circuit has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's OR at least two 1's have occurred as inputs, regardless of the order of occurrence. Draw a state graph (Moore type) for the circuit (five states are sufficient).

Answer: The state graph is shown below.



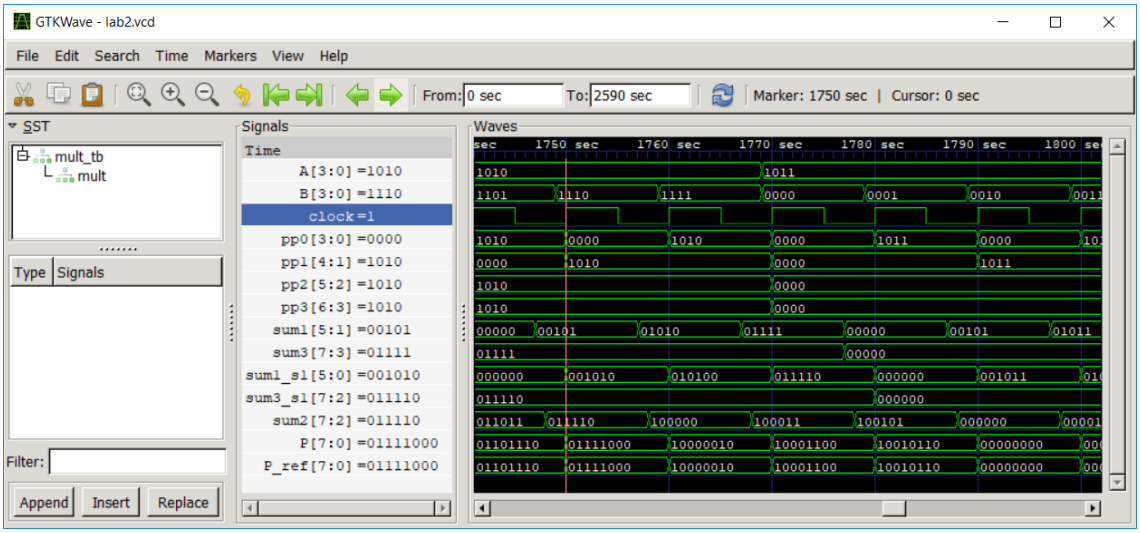
4 Lab 2 — Part 1 (18pts)

Replace <index> in lab2.v with proper indexes, but leave the rest of the code unchanged.

1. (12pts) Print out the module mult_fast.
2. (6pts) Show the waveform with the settings in lab2.sav (should include 1750 to 1800 sec).

Answer:

1. Please check NTU COOL.
2. The example waveforms are shown below.



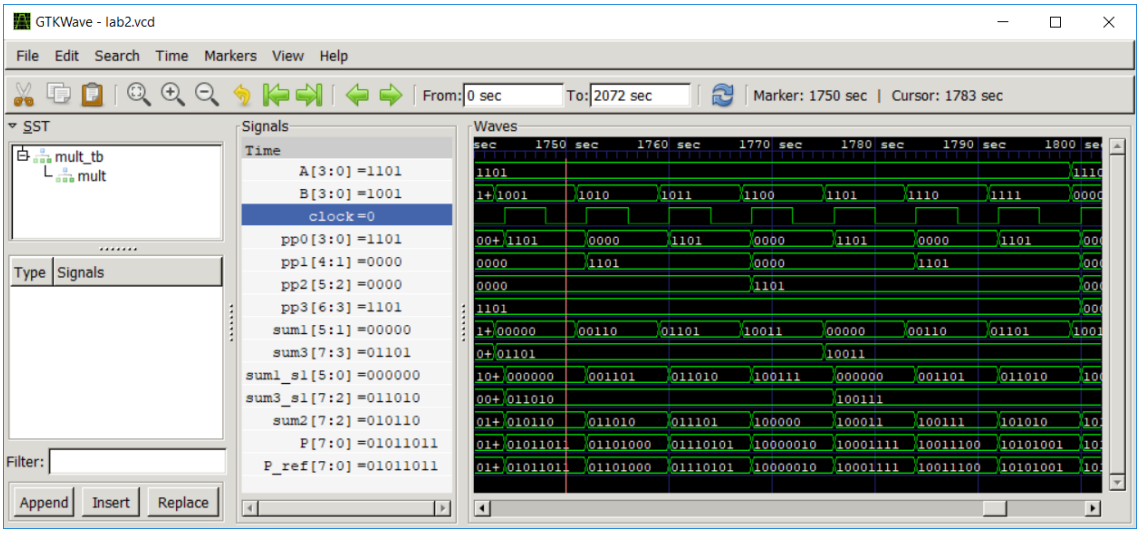
5 Lab 2 — Part 2 (12pts)

Minimize the clock cycle by changing the delays in the module mult_tb.

1. (6pts) What is the minimum clock cycle?
2. (6pts) Show the waveform with the settings in lab2.sav (should include 1750 to 1800 sec).

Answer:

1. 8 seconds.
2. The example waveforms are shown below.



6 Lab 2 — Part 3 (12pts)

Assume the clock cycle is 10 microseconds.

1. (6pts) What is the throughput (operations per second)?
2. (6pts) What is the latency (worst case waiting time from the input becomes steady to the register of the last stage refreshes)?

Answer:

1. 100,000 operations per second.
2. 30 microseconds.