CSIE 2344, Spring 2019 — Final Exam Solution Sketch

Name: _____ SID: _____ Email: _____

1 Multiple-Choice Questions (4pts)

Pick ONE of the choices for each question. No explanation is required.

_____ 1. (1pt) A "pure-play semiconductor foundry" is a company that does not offer a significant amount of IC products of its own design, but instead operates semiconductor fabrication plants focused on producing ICs for other companies. Regarding the market share in the first quarter of 2019, the world's largest pure-play semiconductor foundry is

1. Globalfoundries.
2. Intel.
3. Samsung.
4. TSMC.

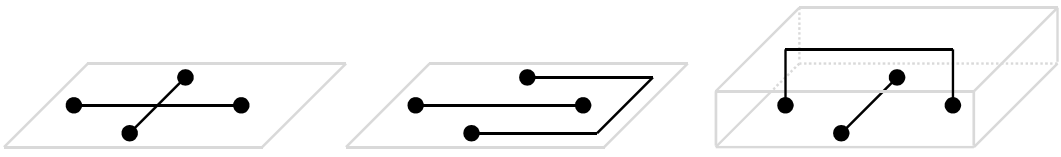
_____ 2. (1pt) "IC Compiler II" is a product of Synopsys. It is

1. Document.
2. Hardware.
3. Software.

_____ 3. (1pt) Regarding the business model, which of the following descriptions is the most precise?

1. MediaTek pays to Synopsys, and MediaTek pays to TSMC.
2. MediaTek pays to Synopsys, and TSMC pays to MediaTek.
3. Synopsys pays to MediaTek, and MediaTek pays to TSMC.
4. Synopsys pays to MediaTek, and TSMC pays to MediaTek.

_____ 4. (1pt) Which one of the following routing results for two netlists is NOT feasible?



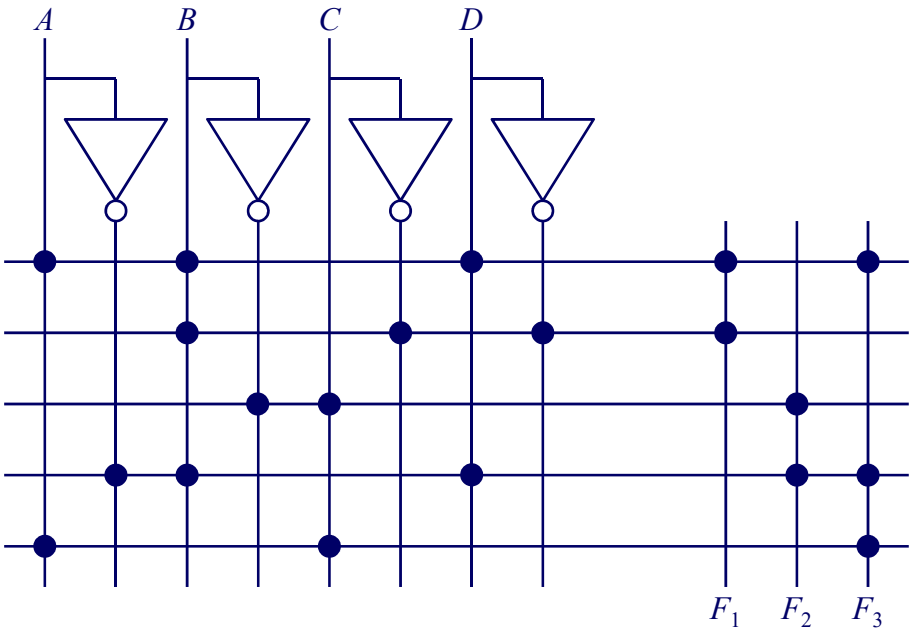
1. 2. 3.

Answer: 4,3,1,1.

2 Programmable Logic Array (8pts)

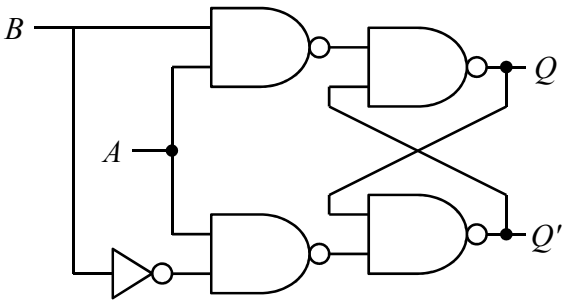
$F_1 = ABD + BC'D'$ has been implemented below. Implement $F_2 = B'C + A'BD$ and $F_3 = AC + BD$ by adding "•" below (adding lines is not allowed). No explanation is required.

Answer:



3 Latch (8pts)

Given the latch, complete the following truth table. No explanation is required.



A	B	Q	Q^+
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Answer: 0,1,0,1,0,0,1,1.

4 Counter (28pts)

Design a 3-bit counter which counts CBA in the sequence: 001, 100, 101, 111, 110, 010, 011, and repeats. No explanation is required.

1. (4pts) Complete the following truth table.
2. (4pts) Complete the following Karnaugh map for C^+.
3. (4pts) Complete the following Karnaugh map for B^+.
4. (4pts) Use a J-K flip-flop and complete the following Karnaugh map for J_C.
5. (4pts) Use an S-R flip-flop and complete the following Karnaugh map for S_B.

   Answer:

C	B	A	C^+	B^+	A^+
0	0	0	X	X	X
0	0	1	1	0	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	1	1	0

BA \ C	0	1
00	X	1
01	1	1
11	0	1
10	0	0

C^+

BA \ C	0	1
00	X	0
01	0	1
11	0	1
10	1	1

B^+

BA \ C	0	1
00	X	X
01	1	X
11	0	X
10	0	X

J_C

BA \ C	0	1
00	X	0
01	0	1
11	0	X
10	X	X

S_B

6. (4pts) Derive a minimum sum-of-products expression for J_C. $J_C =$ _____

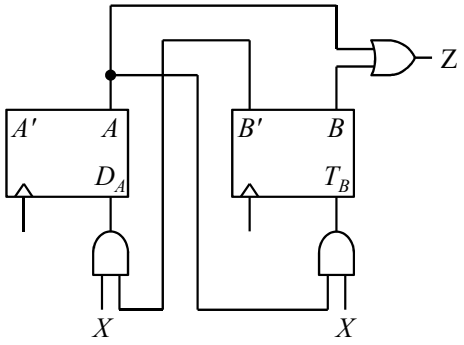
   Answer: $J_C = B'$.

7. (4pts) Derive a minimum sum-of-products expression for S_B. $S_B =$ _____

   Answer: $S_B = AC$.

5 Circuit Analysis (12pts)

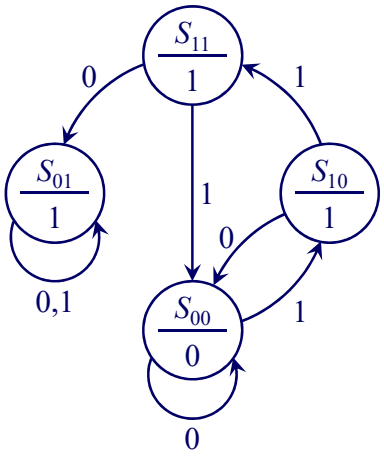
Given the circuit including one D flop-flop and one T flop-flop. No explanation is required.



1. (8pts) Complete the following transition table.
2. (4pts) Complete the following state graph where S_{ij} represents the state $(A, B) = (i, j)$.

Answer:

AB	A^+B^+		Z
	$X=0$	$X=1$	
00	00	10	0
01	01	01	1
11	01	00	1
10	00	11	1



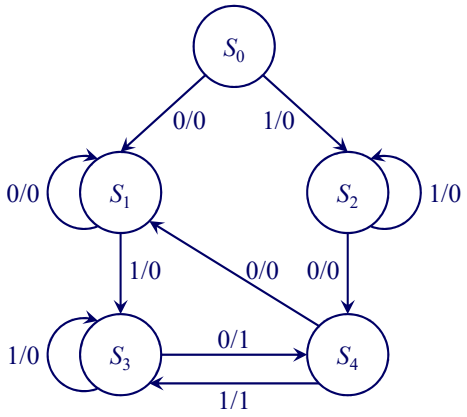
6 State Graph (8pts)

A detector detects a 101 sequence and a sequence starting by 0, ending by 0, having no 0 between the two 0's, and having a positive number of 1's between the two 0's, *i.e.*, 010, 0110, 01110, 011110, ... The following is example inputs and outputs:

$$X = 0110001101110$$
$$Z = 0001000011001$$

Draw a Mealy machine for the detector.

Answer: S_0: reset, S_1: received 0 (00 or after reset), S_2: received 1 (not after a 0), S_3: received 1 (after a 0), S_4: received 10.



7 Circuit Equivalence (8pts)

Given the state tables of two circuits, determine whether the two circuits are equivalent. If yes, list all equivalent states (*e.g.*, $S_0 \equiv A$); otherwise, list all states (in both state tables) which have no equivalent state (*e.g.*, S_0 in the first state table and A in the second state table). You can use the empty table, but it is not required.

	Next State		Z
	$X=0$	$X=1$	
S_0	S_3	S_1	0
S_1	S_0	S_1	0
S_2	S_0	S_2	0
S_3	S_0	S_3	0

	Next State		Z
	$X=0$	$X=1$	
A	E	A	1
B	F	B	1
C	E	D	0
D	E	C	0
E	B	D	0
F	B	C	0

S_0						
S_1						
S_2						
S_3						
	A	B	C	D	E	F

Answer: No. Considering the equivalence in the other table, every state has no equivalent state. Considering the equivalence in the same table, every state has an equivalent state: $S_0 \equiv S_1 \equiv S_2 \equiv S_3$, $A \equiv B$, $C \equiv D$, $E \equiv F$.

8 Rules Derivation (8pts)

Given the truth table of a new flip-flop: Y flip-flop.

1. (6pts) Complete the following table by deriving its rules from a next state map to an input map.
2. (2pts) Does this flip-flop have any limitation in counter design?

Y	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	0

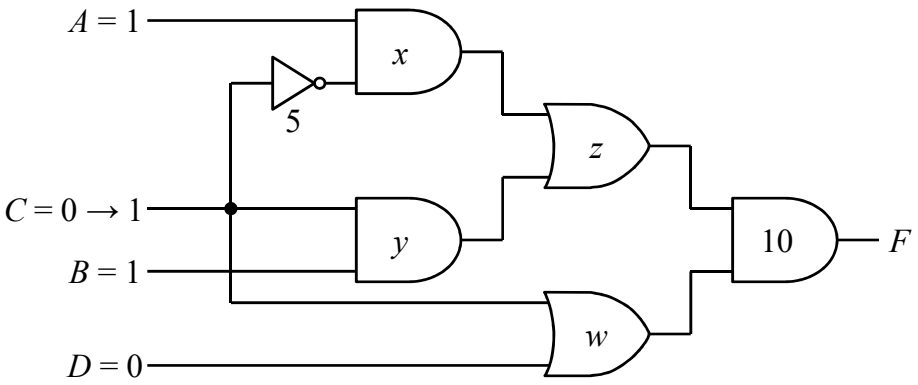
Type of FF	Input	Rules from Next State Map to Input Map	
		Q = 0 Half of Map	Q = 1 Half of Map
D	D	No change	No change
T	T	No change	Complement
Y	Y		

Answer:

1. For $Q = 0$ half, no change. For $Q = 1$ half, replace 0's with X's and replace 1's with "not implementable".
2. The flip-flop cannot implement a counter where one bit has two consecutive 1's.

9 Dynamic Hazard (16pts)

Given the circuit.



1. (8pts) The transition (A, B, C, D) from $(1, 1, 0, 0)$ to $(1, 1, 1, 0)$ has a potential dynamic hazard, depending on the propagation delays of the gates. Assuming $5, 10, w, x, y, z$ are the propagation delays of the corresponding gates, what is the necessary and sufficient condition of w, x, y, z that there is no dynamic hazard for the transition?

2. (8pts) Assuming $x = y$, what is the necessary and sufficient condition of w, x, y, z that there is no dynamic hazard for the circuit (all transitions)? Justify your answer.

Answer:

1. $w \geq 5 + x + z$ or $5 + x \geq y$.

2. C is the only input having three paths to the output, so we only need to consider another transition from $(1, 1, 1, 0)$ to $(1, 1, 0, 0)$. Note that a propagation delay is non-negative.

$$
\begin{aligned}
& ((w \geq 5 + x + z) \vee (5 + x \geq y)) \wedge ((w \leq 5 + x + z) \vee (5 + x \leq y)) \\
\iff & ((w \geq 5 + x + z) \vee (5 + x \geq x)) \wedge ((w \leq 5 + x + z) \vee (5 + x \leq x)) \\
\iff & ((w \geq 5 + x + z) \vee (T)) \wedge ((w \leq 5 + x + z) \vee (F)) \\
\iff & (T) \wedge (w \leq 5 + x + z) \\
\iff & w \leq 5 + x + z,
\end{aligned}
$$

   which is also equivalent to $w \leq 5 + y + z$.