Digital Systems Design and Laboratory
[0. Course Introduction]

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Introduction to Myself

- B.S. Student
  - 2001.09--2005.06, CSIE Department, NTU
- M.S. Student
  - 2005.09--2007.06, GIEE (EDA Group), NTU
- Ph.D. Student
  - 2009.08--2015.08, EECS Department, UC Berkeley
- Researcher
  - 2015.09--2018.07, Systems and Software Division, Toyota InfoTechnology Center (Mountain View, CA)
- Assistant Professor
  - 2018.08--, CSIE Department, NTU

And You Are?

- ❑ Department?
- ❑ Year?
- ❑ Enrolled or auditing?
- ❑ Waiting list?
- ❑ Career goal?

Reasons of Teaching This Course

- EDA background in my M.S. years
  - What is Electronic Design Automation (EDA) ?
- And?

Reasons of Taking This Course

- Get some units to graduate
- Learn fundamental knowledge of "logic" and "hardware"
  - Let's talk about my recruiting experience at CKSH...
  - You should be better than a pure software programmer
    - Software is running on hardware
    - Hardware implementation is usually faster than software implementation
      - Disadvantage?
  - You may work in the "hardware" industry in Taiwan
    - No matter what your role (software engineer, hardware engineer, etc.) is
- Broaden your vision
  - Software cannot be missing in the hardware industry

Websites, Office Hour, and TA

- Basic information
  - https://www.csie.ntu.edu.tw/~cwlin/teaching/2344.html
- Slides, homework assignments, homework solutions, announcement, and discussion
  - NTU COOL: https://cool.ntu.edu.tw/courses/232
  - Add your name and email to the spreadsheet if you cannot sign in now
  - You are mandatory to check the announcement there
- Homework submission and grading
  - Gradescope: https://www.gradescope.com/courses/34376
  - Use the entry code 9KKP26 to sign up
  - Homework 0 (optional) for you to practice how to use it
- Office hour: by appointment?
- TA: Tzu-Hsu Yu

Let's set them up now

Lecture Schedule (Tentative)

Date	Topic	Note
Feb 18	[0] Course Introduction [1] Number Systems	Homework 0 Posted
Feb 25	[2] Boolean Algebra [3] Boolean Algebra (Continued)	Homework 1 Posted
Mar 4	[4] Applications of Boolean Algebra	---
Mar 11	[5] Karnaugh Maps [6] Quine-McCluskey Method	Homework 1 Due (noon)
Mar 18	[7] Multi-Level Gate Circuits	Homework 2 Posted
Mar 25	[8] Combinational Circuit Design	---
? Apr 1	[9] Multiplexers, Decoders, and Programmaable Logic Devices	Homework 2 Due (noon)
Apr 8	Midterm	---
Apr 15	Lab 1	Homework 3 Posted
Apr 22	[11] Latches and Flip-Flops [12] Registers and Counters	---
Apr 29	[13] Analysis of Clocked Sequential Circuits	---
May 6	[14] Derivation of State Graphs and Tables	Homework 3 & Lab 1 Due (noon)
May 13	Lab2	Homework 4 Posted
May 20	[15] Reduction of State Tables	---
May 27	[16] Sequential Circuit Design	---
Jun 3	To Be Decided	Homework 4 & Lab 2 Due (noon)
Jun 10	[16] Overview of Computer-Aided Design (Electronic Design Automation)	---
Jun 17	Final Exam	---

2 Weeks for HW1

2 Weeks for HW2

1 Week for Midterm

3 Weeks for HW3 and Lab 1

3 Weeks for HW4 and Lab 2

2 Weeks for Final Exam

Lecture Plan

- We may use 50 minutes for practice
  - It is better to bring pens or pencils
- Any lecture policy?

Textbook

- C. H. Roth, Jr. and L. L. Kinney, Fundamentals of Logic Design, 7th Edition
  - It is not mandatory to buy it

Homework

- Homework is due at **noon**
  - **No late homework is accepted**
    - Though the submission site will be open until 1:30pm
  - Exception: you email Chung-Wei and **get the approval before the deadline (noon)**
- You are encouraged to work on homework in study groups, but you must write up the solutions on your own

Midterm and Final Exam

❑ Midterm

- ➢ You can bring 1 page of single sided A4 note
- ➢ You can ask (= challenge) for regrading (based on problems) before a deadline, and then we will regrade them
  - For each problem
    - If your score becomes higher, you win the challenge
    - Otherwise, you lose the challenge
  - Starting from the 3rd failed challenge, you get additional deduction

❑ Final

- ➢ You can bring 2 pages of single sided A4 note
- ➢ Same regrading policy

Grading

- Homework/Lab: 26%
  - Homework 1: 5%
  - Homework 2: 5%
  - Homework 3 + Lab 1: 8%
  - Homework 4 + Lab 2: 8%
- Midterm: 34%
- Final Exam: 40%
- Bonus
- Academic Dishonesty = Failing by Default

- Grading philosophy?

Q&A