Digital Systems Design and Laboratory
Spring 2019
Lab 1 Hints

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Lab1:
https://docs.google.com/presentation/d/1ZVtwYdc9ZvPP_TGaImBmhOHKjKporxjmLe0kAVMO6iU

Agenda

- Requirements
- Concepts to Clarify
- FAQ

Requirements

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- Implement a 3-bit adder **`adder_rtl`** using RTL modeling.
- Implement a 3-bit carry-lookahead adder **`cla_gl`** using gate-level modeling, only the gates provided in `gates.v` (with delays) are allowed to use.
- Print out your source codes and attach it with your Homework 3.
- Show the waveform of `cla_gl.S[2:0]` on input transitions:
  (1) from 000 + 000 + 0 to 001 + 000 + 1
  (2) from 111 + 000 + 0 to 000 + 111 + 0
- Find the maximum propagation delay of `cla_gl` and one of the corresponding input transitions.
- Assume that only 2-input gates are used. Derive the number of levels needed in an n-bit carry-lookahead adder as a function of n.

Hints

- **`adder_rtl`** should be simple to implement, I did it in one line.
- The outputs of **`adder_rtl`** and **`cla_gl`** should be the same at steady state. If they're different, maybe there's some mistake in **`cla_gl`** since it's complicated.
- Implement your adders in `adders.v`. The output and input signals are given.
- Do not modify `gates.v`.
- Only minor changes should be done to `lab1.v`.
- Use system tasks and GTKWave to debug.

- Feel free to email me for any questions. (address on the first page)
- And please remember to bring your laptop at Lab2!

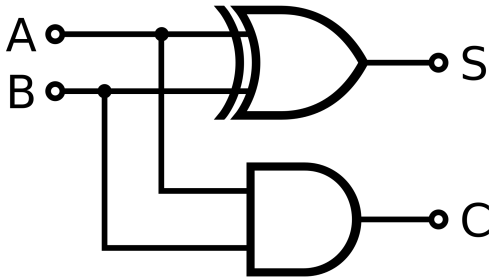
Concepts to Clarify

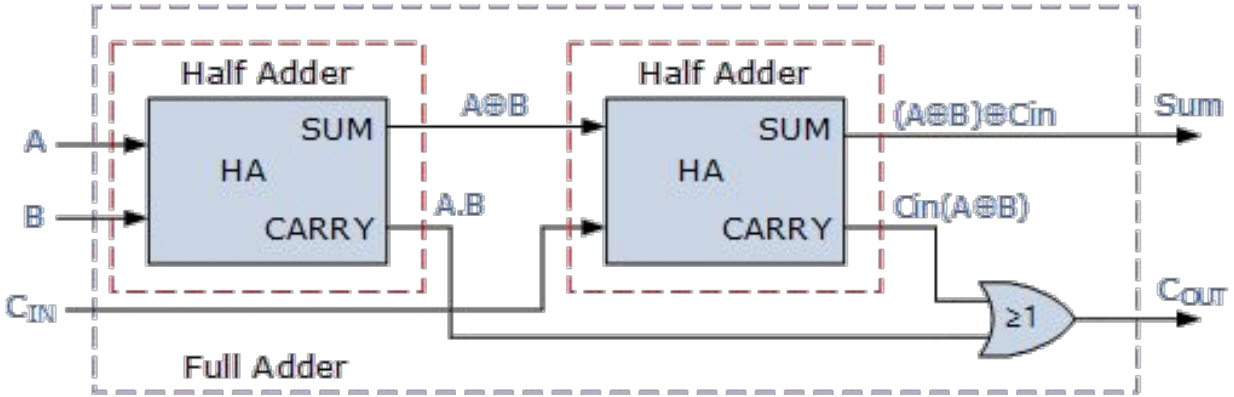
Hardware description language (HDL)

- Verilog is not C. ~~Please stop writing C code with Verilog~~
- HDLs are more like blueprints of circuits
- HDLs don't "execute", "call", or "return" after synthesis
- Synthesizer: HDL → circuit design
- Compiler (`iverilog`): HDL (`.v`) → model (`.vvp`)
- Simulator (`vvp`): model (`.vvp`) → simulated result (`.vcd`)

Half adder and full adder

HA: `assign {C, S} = A+B;` FA: `assign {Cout, S} = A+B+Cin;`



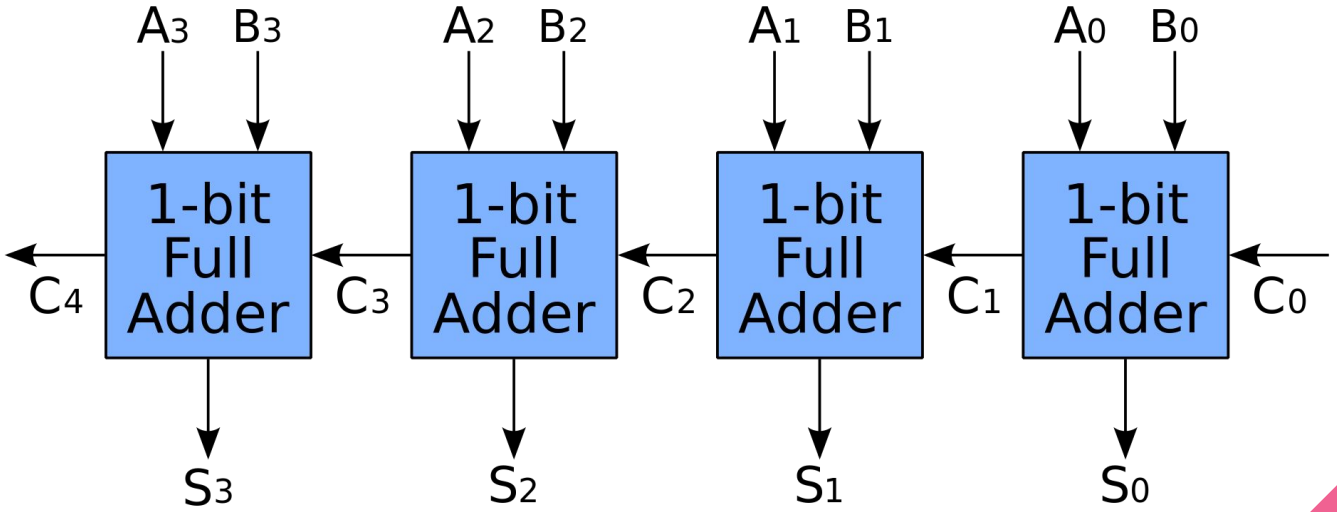


https://en.wikipedia.org/wiki/Adder_(electronics)
https://www.electronics-tutorials.ws/combination/comb_7.html

Ripple-carry adder

Notice that $carry_n$ depends on $carry_{n-1}$

Where is the longest propagation path?



https://en.wikipedia.org/wiki/Adder_(electronics)

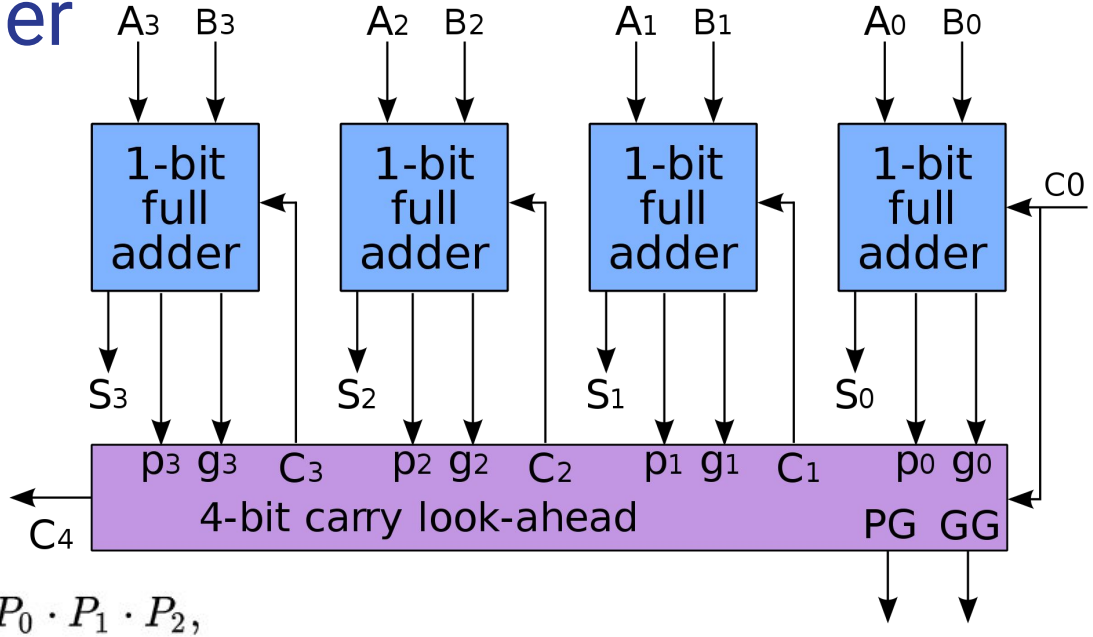
Carry-lookahead adder

$$G_i = A_i \cdot B_i.$$

Pi can be either:

$$P_i = A_i \oplus B_i,$$

$$P_i = A_i + B_i.$$



$$C_1 = G_0 + P_0 \cdot C_0,$$

$$C_2 = G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1,$$

$$C_3 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2,$$

$$C_4 = G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3.$$

PG and GG don't have to be implemented in the assignment.

https://en.wikipedia.org/wiki/Carry-lookahead_adder

Levels Needed

How many levels of gates are needed to derive C3 in the following two implementations?

$$
\begin{aligned}
C_1 &= G_0 + P_0 \cdot C_0, \\
C_2 &= G_1 + P_1 \cdot C_1, \\
C_3 &= G_2 + P_2 \cdot C_2, \\
C_4 &= G_3 + P_3 \cdot C_3.
\end{aligned}
$$

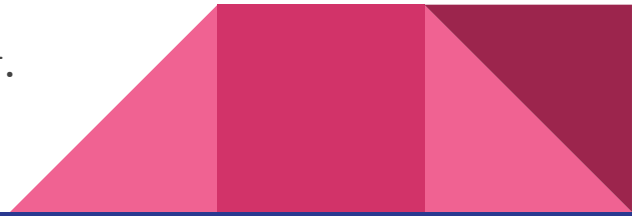
$$
\begin{aligned}
C_1 &= G_0 + P_0 \cdot C_0, \\
C_2 &= G_1 + G_0 \cdot P_1 + C_0 \cdot P_0 \cdot P_1, \\
C_3 &= G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2, \\
C_4 &= G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3.
\end{aligned}
$$

FAQ

4. Source Code

Print out your `cla_gl` and `adder_rtl` source code.

- What is `rca_gl`?
  It's a reference for gate level modeling. You don't have to use it in Hw1.
- Results of the two adders are different.
  Those might be hazards. Just inspect the steady states.
- Submit only the implementation code segments.
- You may use modules to simplify things. E.g. You may want to use the provided FA module or write your own modules,
  but they have to be based on the gates in `adders.v`.

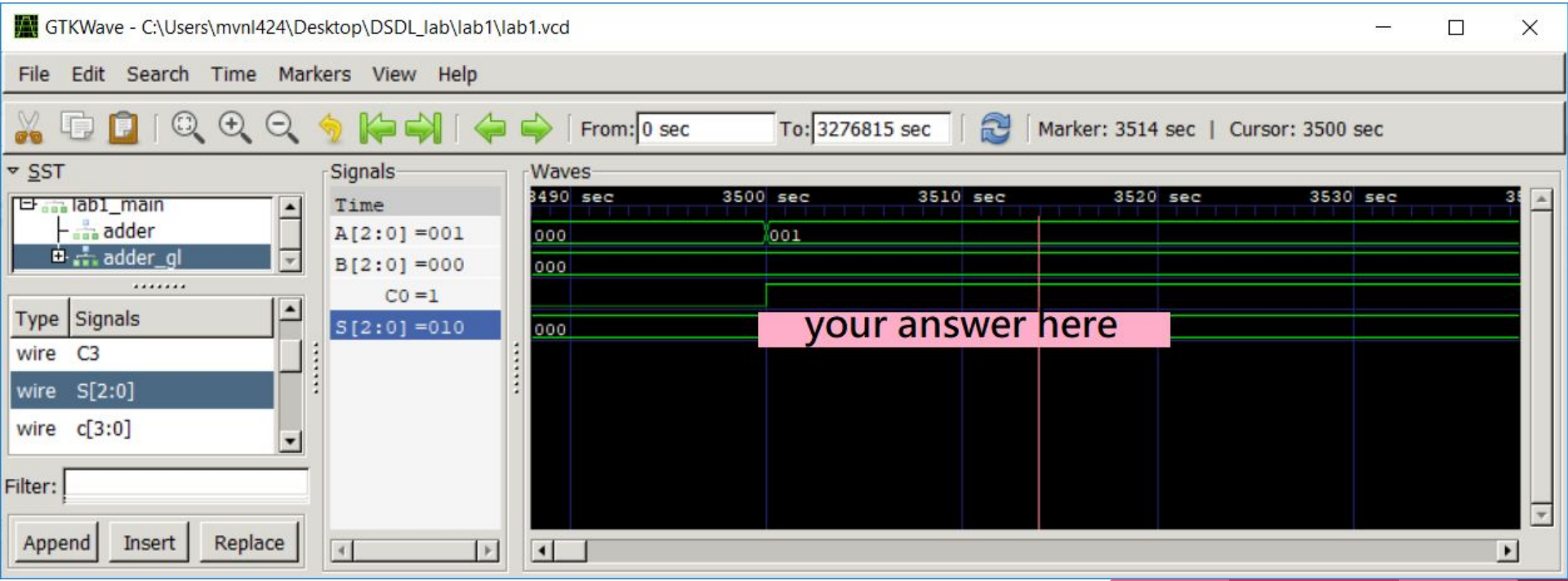


5. Waveform

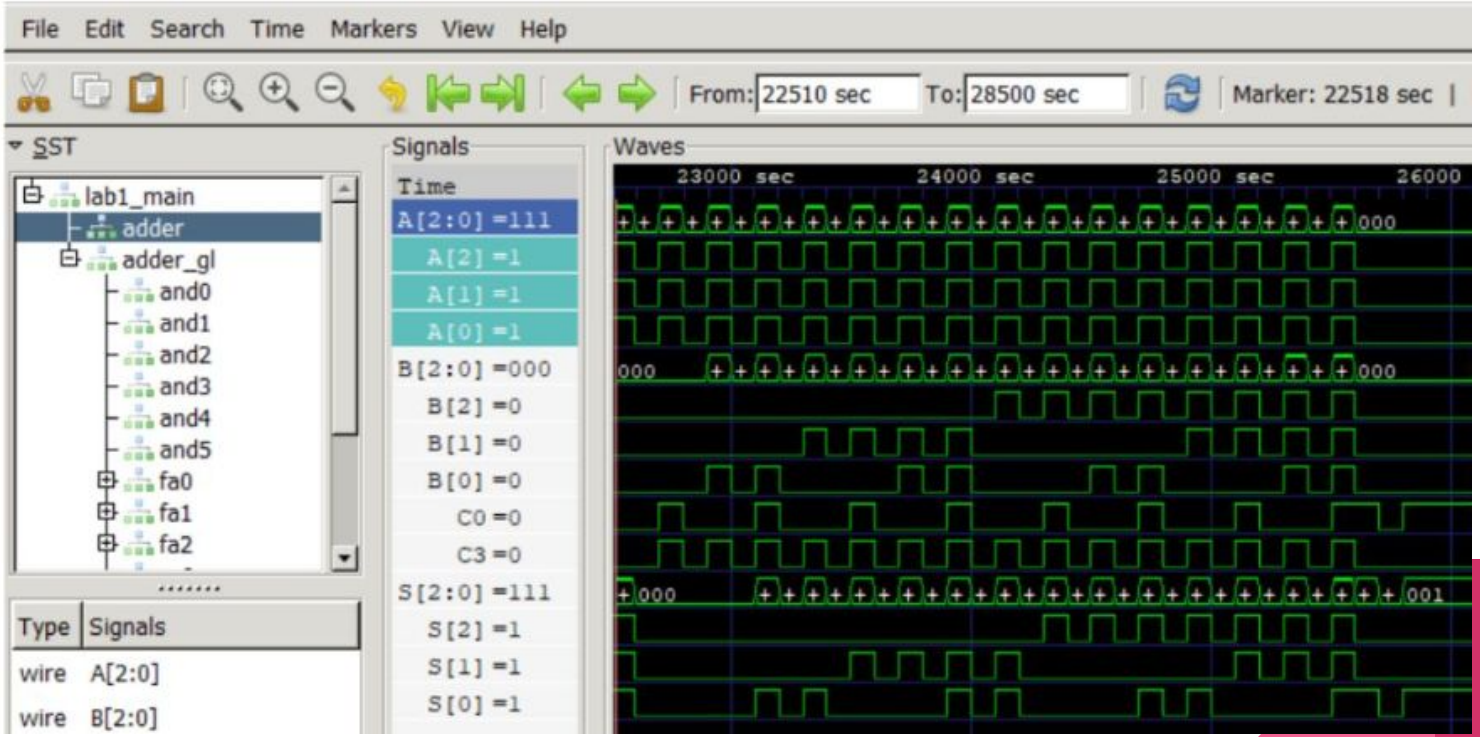
Show the waveform of `cla_gl.S[2:0]` on input transitions `000+000+0→001+000+1` and `111+000+0→000+111+0`.

- How to zoom in and zoom out?
- Submit only the required transitions.
- Make sure that every bit of every state can be clearly read.
- Include time labels.
- Feel free to modify the input sequence or even write your own test bench.
- `gtkwave lab1.vcd lab1.sav`

5. Waveform (Example)



5. Waveform (Please don’t submit this QAQ)



6. Propagation Delay

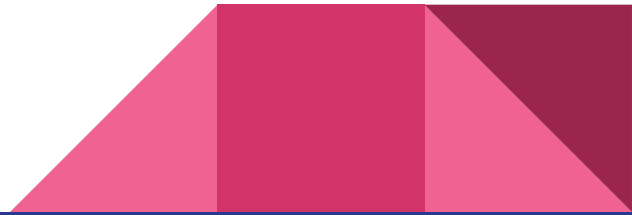
Find the maximum propagation delay of `cla_gl` and one of the corresponding input transitions.

- My friend has a slightly higher delay than mine. Is it normal?
  Yes. Just make sure you implementation is correct, and the delay is in a reasonable range (e.g. delay of CLAs should be shorter than RCAs).

7. Some Derivation

Assume that only 2-input gates are used. Derive the number of levels needed in an n-bit carry-lookahead adder as a function of n.

- 2-input XOR and XNOR are also allowed.
- Can we submit only the result without intermediate steps?
  No. The derivation process and simple explanation are required.
- It should be an **integer-valued sublinear** function.
- Big O notation will not be accepted. Please give the exact expression.



Homework 3
Due on 5/10 1:30pm