CSIE 2344, Spring 2019 — Homework 4

Due June 3 (Monday) at Noon

There are 96 points in total. Points will be deducted if no appropriate intermediate step is provided.

When you submit your homework on Gradescope, please select the corresponding page(s) of each problem.

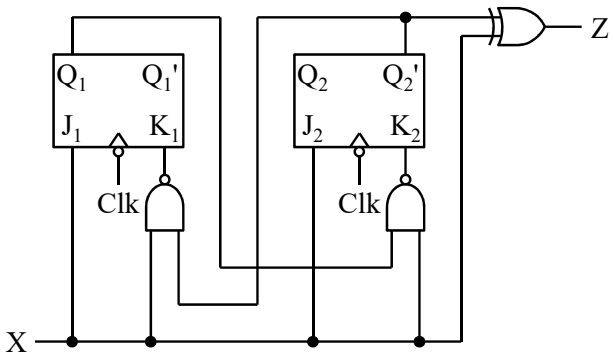
1 Counter (36pts)

Design a 3-bit counter which counts CBA in the sequence: 001, 011, 010, 110, 111, 101, 100, and repeats.

1. (6pts) Use D flip-flops. Derive a minimum sum-of-products expression for D_C.
2. (6pts) Use T flip-flops. Derive a minimum sum-of-products expression for T_C.
3. (12pts) Use S-R flip-flops. Derive a minimum sum-of-products expression for S_B and R_B.
4. (12pts) Use J-K flip-flops. Derive a minimum sum-of-products expression for J_A and K_A.

2 State Table and State Graph Construction (12pts)

Given the following circuit,



1. (6pts) Construct the state table.
2. (6pts) Construct the state graph.

3 State Graph Derivation (6pts)

A sequential circuit has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's OR at least two 1's have occurred as inputs, regardless of the order of occurrence. Draw a state graph (Moore type) for the circuit (five states are sufficient).

4 Lab 2 — Part 1 (18pts)

Replace <index> in lab2.v with proper indexes, but leave the rest of the code unchanged.

1. (12pts) Print out the module mult_fast.
2. (6pts) Show the waveform with the settings in lab2.sav (should include 1750 to 1800 sec).

5 Lab 2 — Part 2 (12pts)

Minimize the clock cycle by changing the delays in the module mult_tb.

1. (6pts) What is the minimum clock cycle?
2. (6pts) Show the waveform with the settings in lab2.sav (should include 1750 to 1800 sec).

6 Lab 2 — Part 3 (12pts)

Assume the clock cycle is 10 microseconds.

1. (6pts) What is the throughput (operations per second)?
2. (6pts) What is the latency (worst case waiting time from the input becomes steady to the register of the last stage refreshes)?