Digital Systems Design and Laboratory
[21. Course Summary]

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We would like to thank Prof. Hui-Ru Jiang (NTU) for contributing the lecture material

Lecutre Schedule

Date	Topic	Note
Feb 18	[0] Course Introduction [1] Number Systems and Conversion	Homework 0 Posted
Feb 25	[2] Boolean Algebra	Homework 1 Posted
Mar 4	[3] Boolean Algebra (Continued) [4] Applications of Boolean Algebra	---
Mar 11	[4] Applications of Boolean Algebra [5] Karnaugh Maps	Homework 1 Due (noon)
Mar 18	[5] Karnaugh Maps [6] Quine-McCluskey Method [7] Multi-Level Gate Circuits	Homework 2 Posted
Mar 25	[7] Multi-Level Gate Circuits [8] Combinational Circuit Design	---
Apr 1	[8] Combinational Circuit Design [9] Multiplexers, Decoders, and Programmable Logic Devices	Homework 2 Due (noon)
Apr 8	Midterm	---
Apr 15	Lab 1	Homework 3 Posted
Apr 22	[9] Multiplexers, Decoders, and Programmable Logic Devices [11] Latches and Flip-Flops	---
Apr 29	[11] Latches and Flip-Flops [12] Registers and Counters	---
May 6	Guest Talk (Synopsys) Guest Talk (Prof. Yao-Wen Chang)	Homework 3 & Lab 1 Due (noon, May 10)
May 13	Guest Talk (MediaTek) Guest Talk (Prof. Hui-Ru Jiang) [12] Registers and Counters [13] Analysis of Clocked Sequential Circuits	Homework 4 Posted
May 20	Guest Talk (Prof. Jie-Hong Jiang) Lab 2	---
May 27	[13] Analysis of Clocked Sequential Circuits [14] Derivation of State Graphs and Tables [15] Reduction of State Tables	---
Jun 3	Lab Demo	Homework 4 & Lab 2 Due (noon)
Jun 10	[15] Reduction of State Tables [16] Sequential Circuit Design [21] Course Summary	---
Jun 17	Final Exam	---

Final Exam

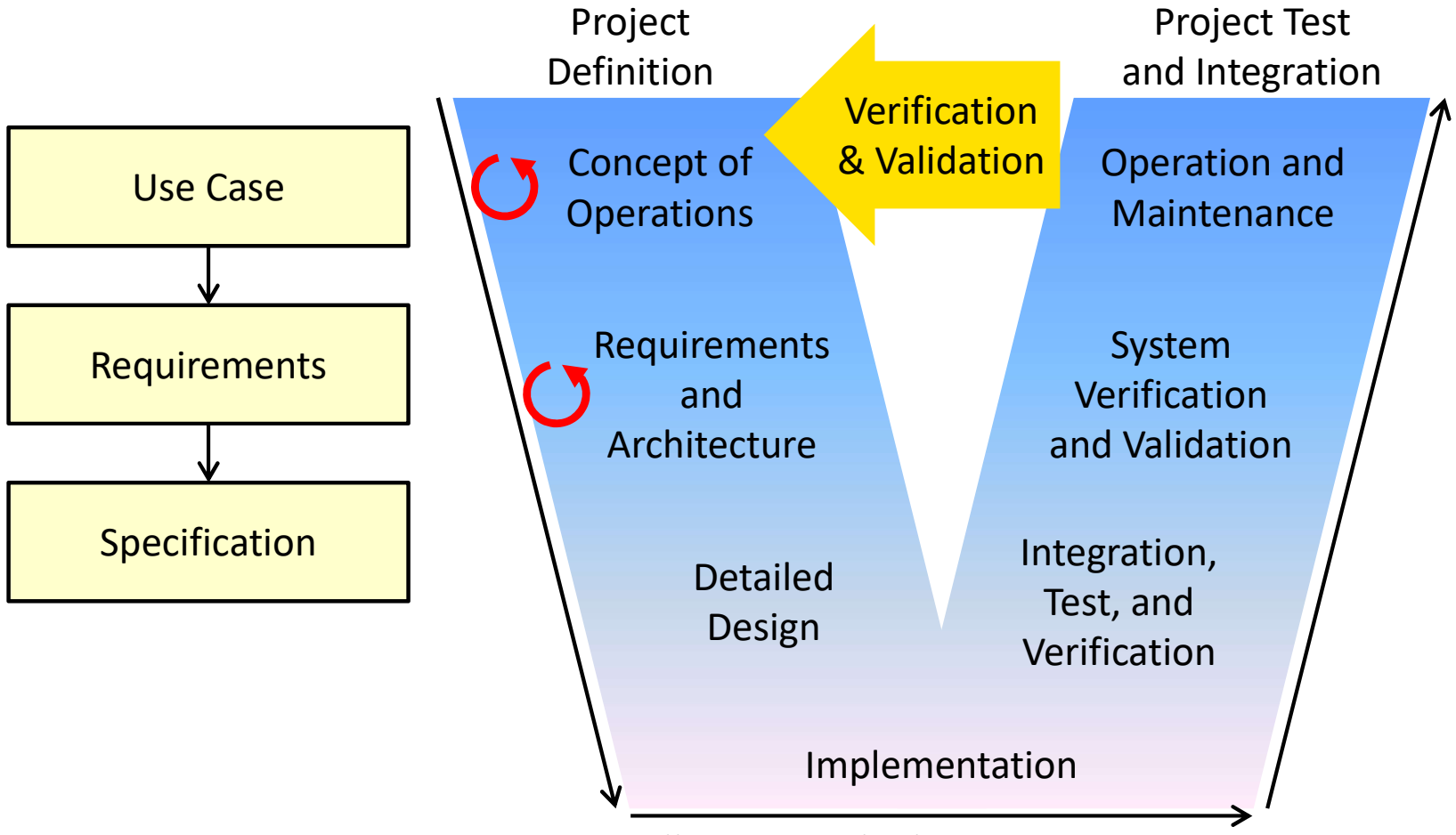
- 1:30pm (length TBD) on June 17
- **ALL** material until June 10, except Unit 6
  - Focus more on
    - [8] Hazards
    - [9] Multiplexers, Decoders, and Programmable Logic Devices
    - [11] Latches and Flip-Flops
    - [12] Registers and Counters
    - [13] Analysis of Clocked Sequential Circuits
    - [14] Derivation of State Graphs and Tables
    - [15] Reduction of State Tables
    - [16] Sequential Circuit Design
  - May have few high-level questions on guest talks and labs
- You can bring 2 pages of single sided A4 note

Reasons of Taking This Course

- Get some units to graduate
- Learn fundamental knowledge of "logic" and "hardware"
  - Let's talk about my recruiting experience at CKSH...
  - You should be better than a pure software programmer
  - You may work in the "hardware" industry in Taiwan
- Broaden your vision
  - Software cannot be missing in the hardware industry

V Model

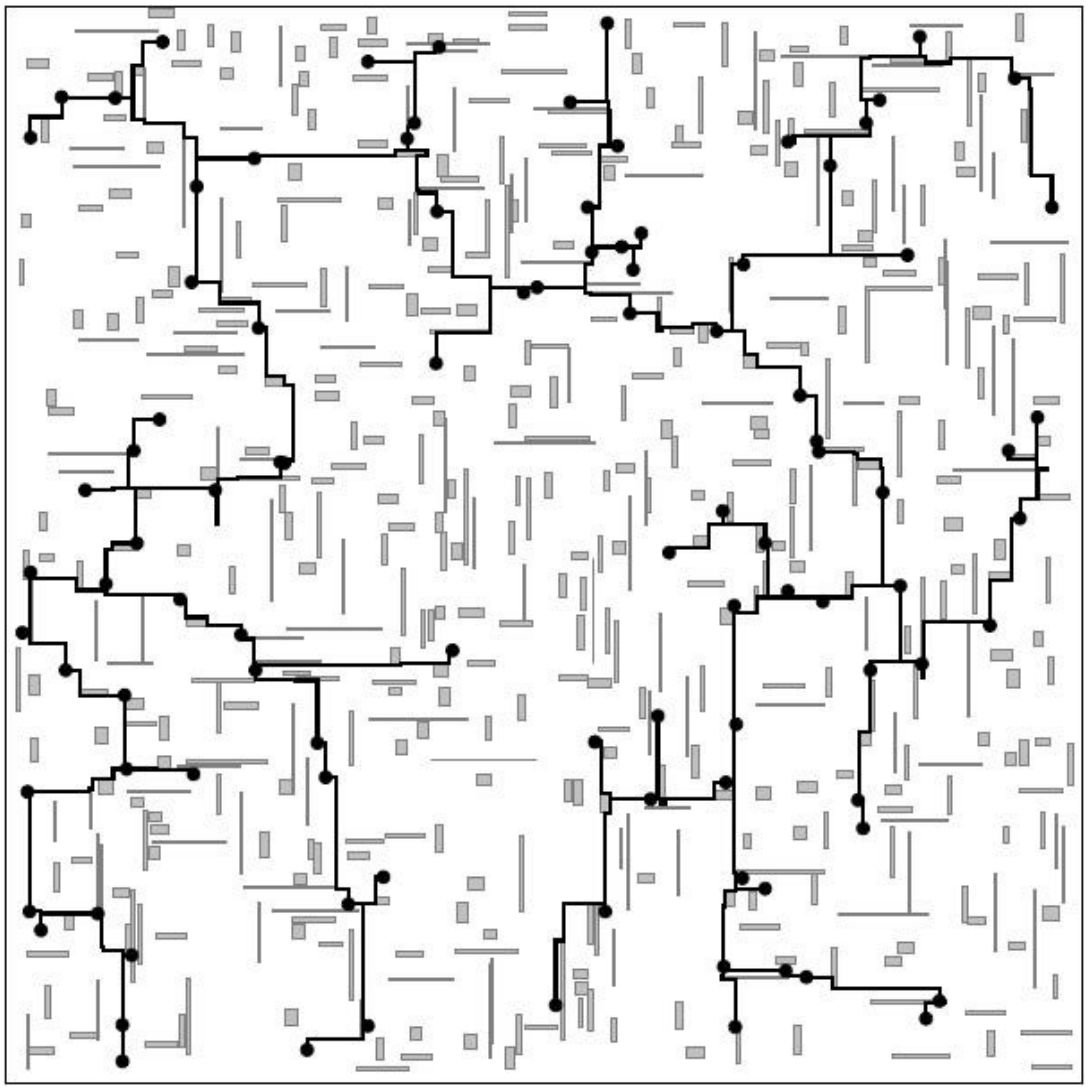
- Consider different design metrics
  - Cost, number of gates, number of gate inputs, performance, etc.
- Assist system designers for early design decisions



https://en.wikipedia.org/wiki/V-Model_(software_development)

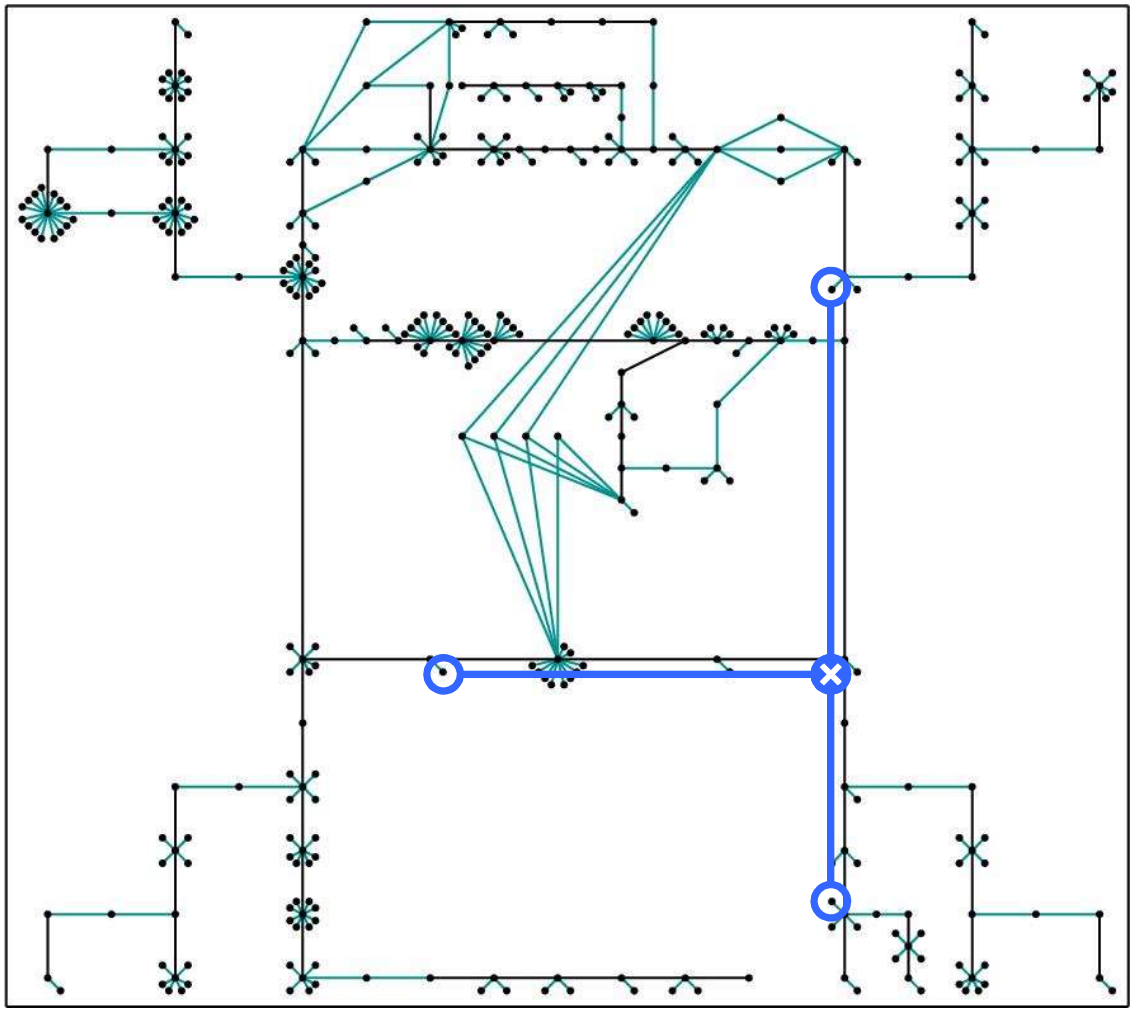
Systematic Solution

- Examples
  - Karnaugh map
  - Routing



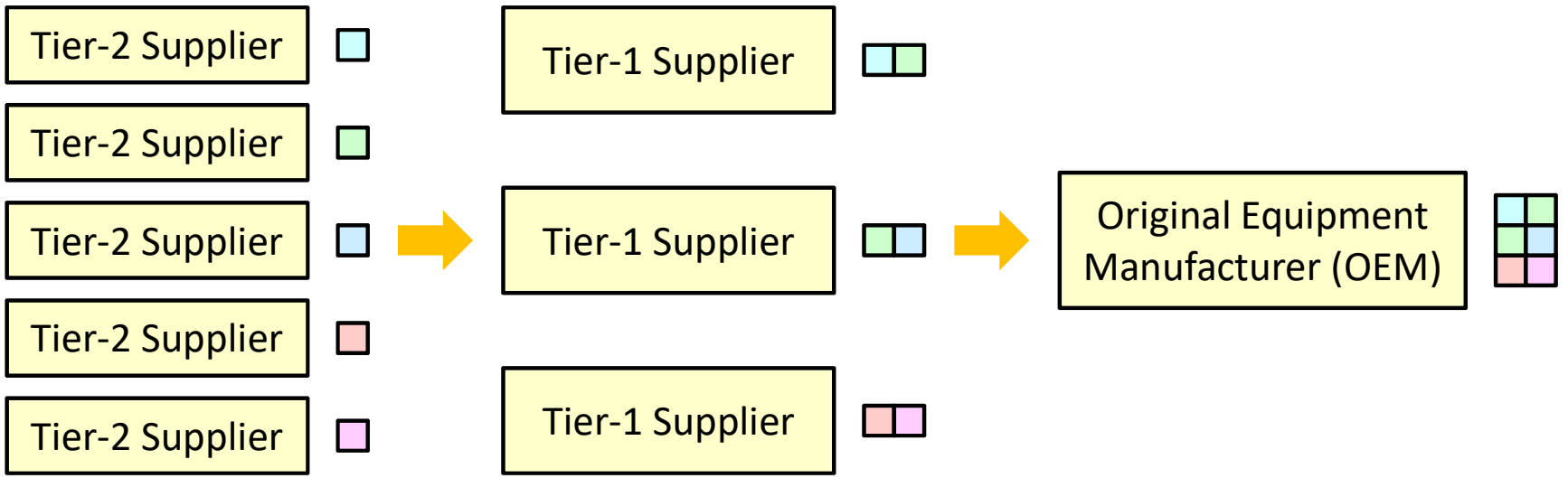
Not Limited to Circuit Design! (1/2)

- The wiring weight of a system can be up to 30kg
  - The third heaviest and costliest component in an automotive system (after the chassis and the engine)
  - Netlist ○ ○ ○
    - A set of "parts" to be connected
  - Splice ⊗
    - Used for connecting more than two wires
    - Steiner vertex!
  - Where to put splices?
    - Steiner tree problem



Not Limited to Circuit Design! (2/2)

https://www.amatechinc.com/resources/blog/tier-1-2-3-automotive-industry-supply-chain-explained



What's Next? (Last Slide)

- Final exam on June 17
  - Regrade request due on June 24
- Following coursework
  - [CSIE3340] Computer Architecture
  - [CSIE3110] Formal Languages and Automata Theory
  - Optional: [EE3020] Integrated Circuit Design
    - More after that
  - Optional: [EE3012] Introduction to Electronic Design Automation
    - More after that
- After graduation (less than two years from now?)
  - Industry
  - Graduate program at NTU?
  - Graduate program abroad?

Thanks!

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