CSIE 2344, Spring 2019 — Homework 3

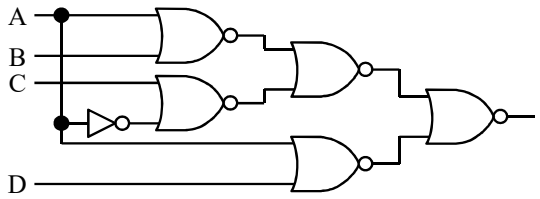
Due May 6 (Monday) at Noon

There are 96 points in total. Points will be deducted if no appropriate intermediate step is provided.

When you submit your homework on Gradescope, please select the corresponding page(s) of each problem.

1 Hazards (16pts)

This question is the same as the first one in Discussion of Week 7. Consider the three-level NOR circuit below and find all static and dynamic hazards in this circuit.

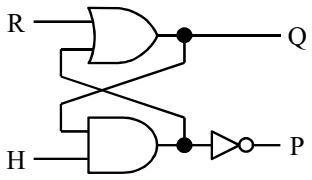


2 MUXes and Three-State Buffers (8pts)

Show how to make an 8-to-1 MUX using two 4-to-1 MUXes, two three-state buffers, and one inverter.

3 Latch (16pts)

A latch can be constructed from an OR gate, an AND gate, and an inverter connected as follows.



1. What restriction must be placed on R and H so that P will always equal Q' (under steady-state conditions)?
2. Construct a next-state table and derive the characteristic (next-state) equation for the latch.

4 Lab 1 — Source Code (24pts)

1. (16pts) Print out your `cla_gl` source code and attach it with your Homework 3.
2. (8pts) Print out your `adder_rtl` source code and attach it with your Homework 3.

We may ask you to demo on May 13 or Jun 3. Points will be deducted if your demo fails. ***You can only demo with the source code same as that you submit***.

5 Lab 1 — Waveform (16pts)

1. Show the waveform of `cla_gl`.S[2:0] on input transition from $000 + 000 + 0$ to $001 + 000 + 1$.
2. Show the waveform of `cla_gl`.S[2:0] on input transition from $111 + 000 + 0$ to $000 + 111 + 0$.

6 Lab 1 — Propagation Delay (8pts)

Find the maximum propagation delay of `cla_gl` and one of the corresponding input transitions.

7 Lab 1 — Some Derivation (8pts)

Assume that only 2-input gates are used. Derive the number of levels needed in an n-bit carry-lookahead adder as a function of n.