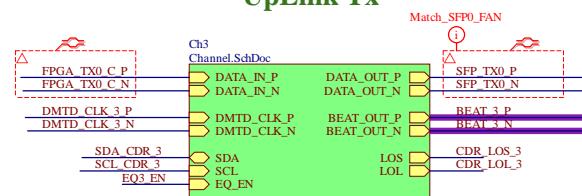


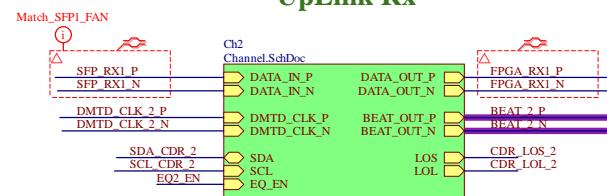
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Dedicated to GT 1 (Channel 1) on Quad 0 and SFP 1

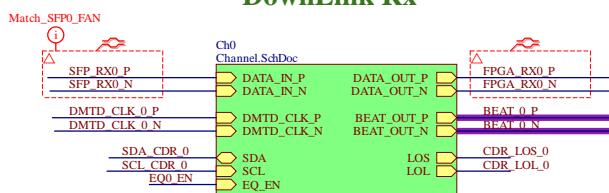
UpLink Tx



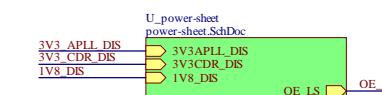
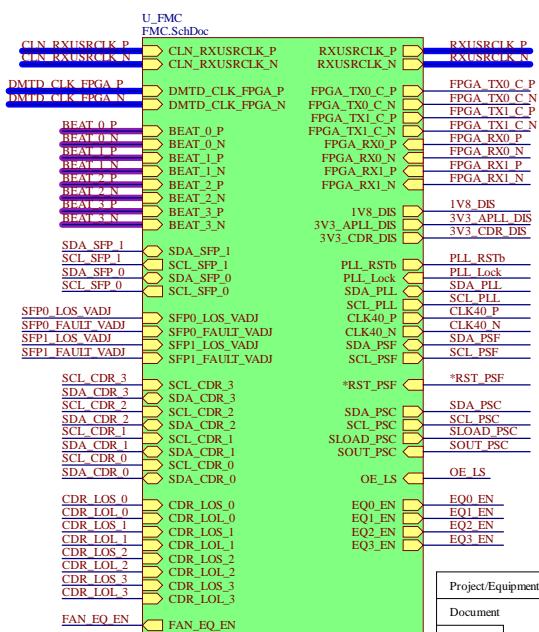
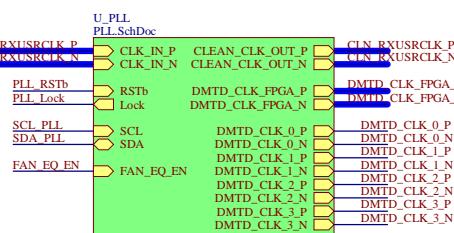
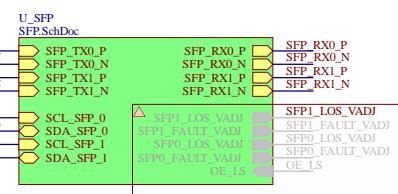
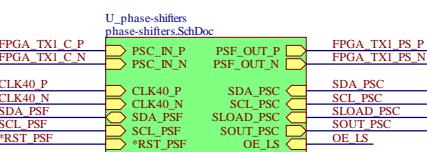
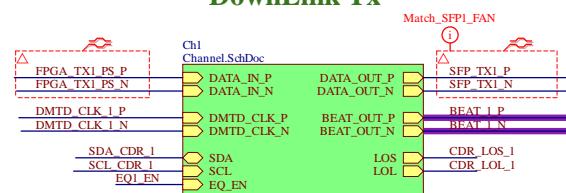
UpLink Rx



DownLink Rx



DownLink Tx



Project Options > Options >

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4. Net identifier scope: Automatic (Hierarchical)
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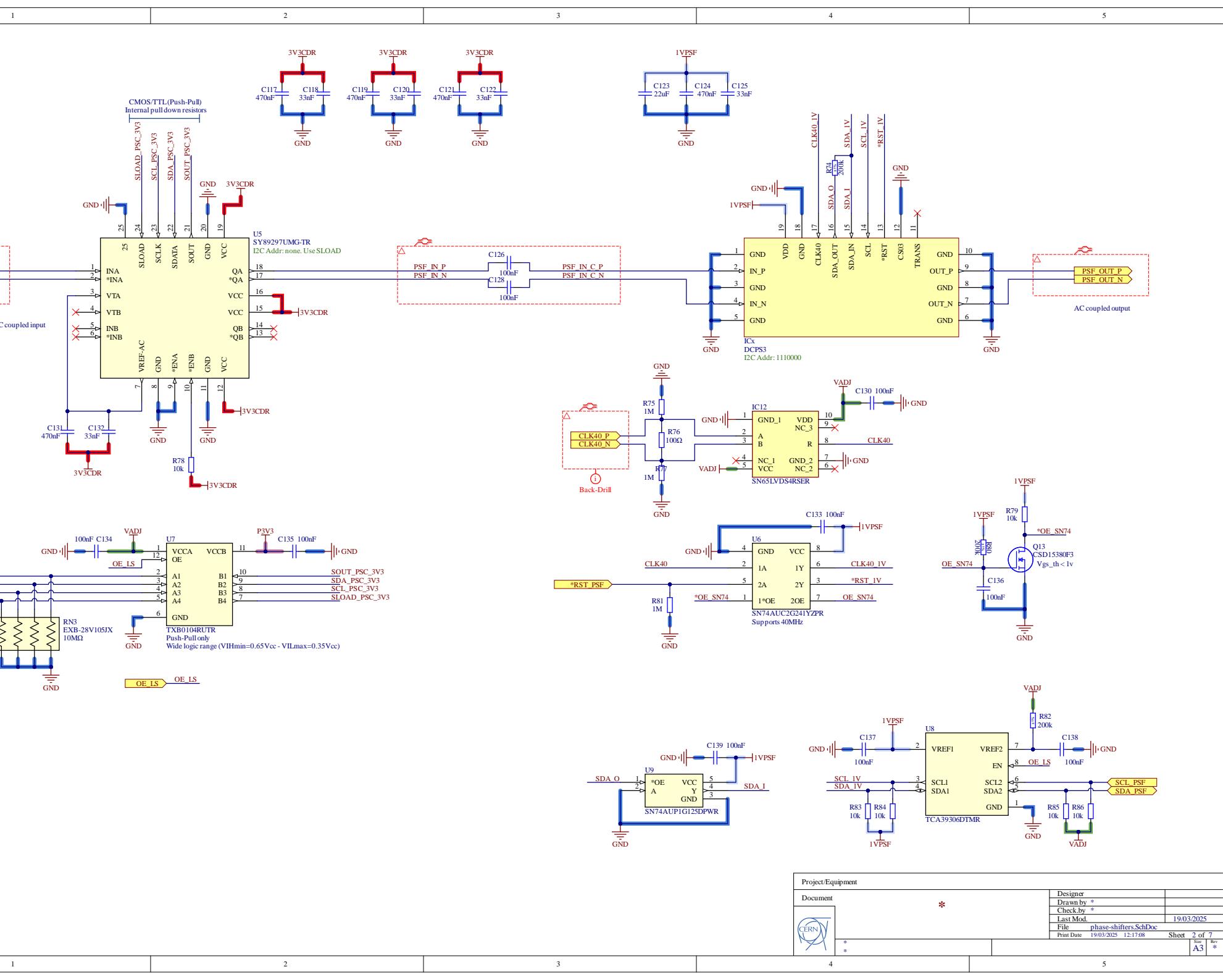
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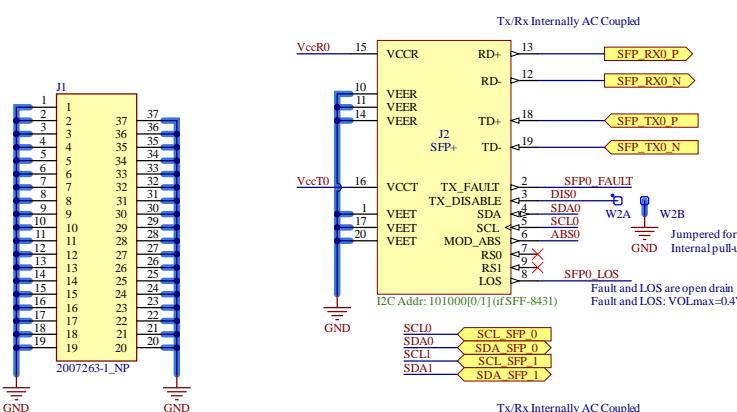


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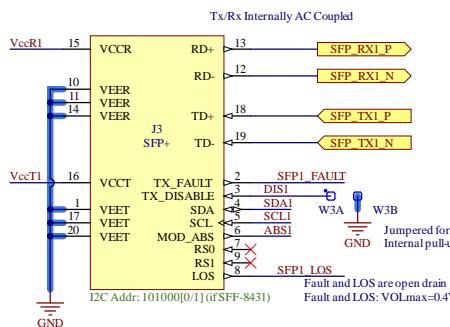
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Size	A3
Rev	*



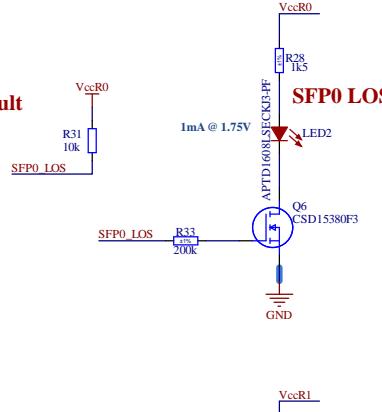
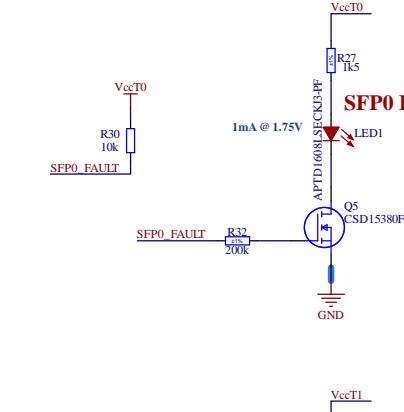
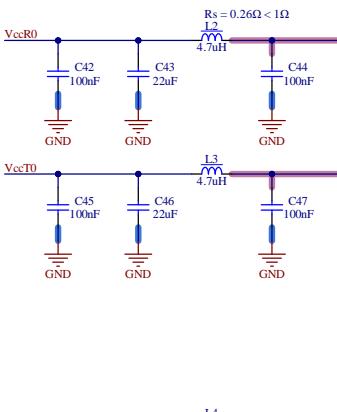
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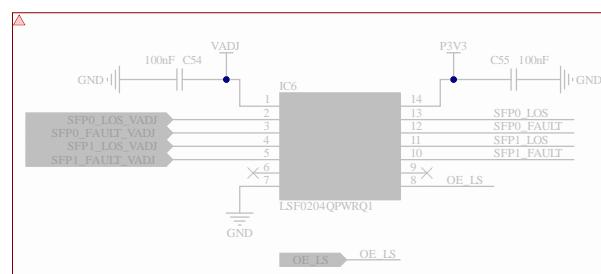
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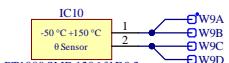
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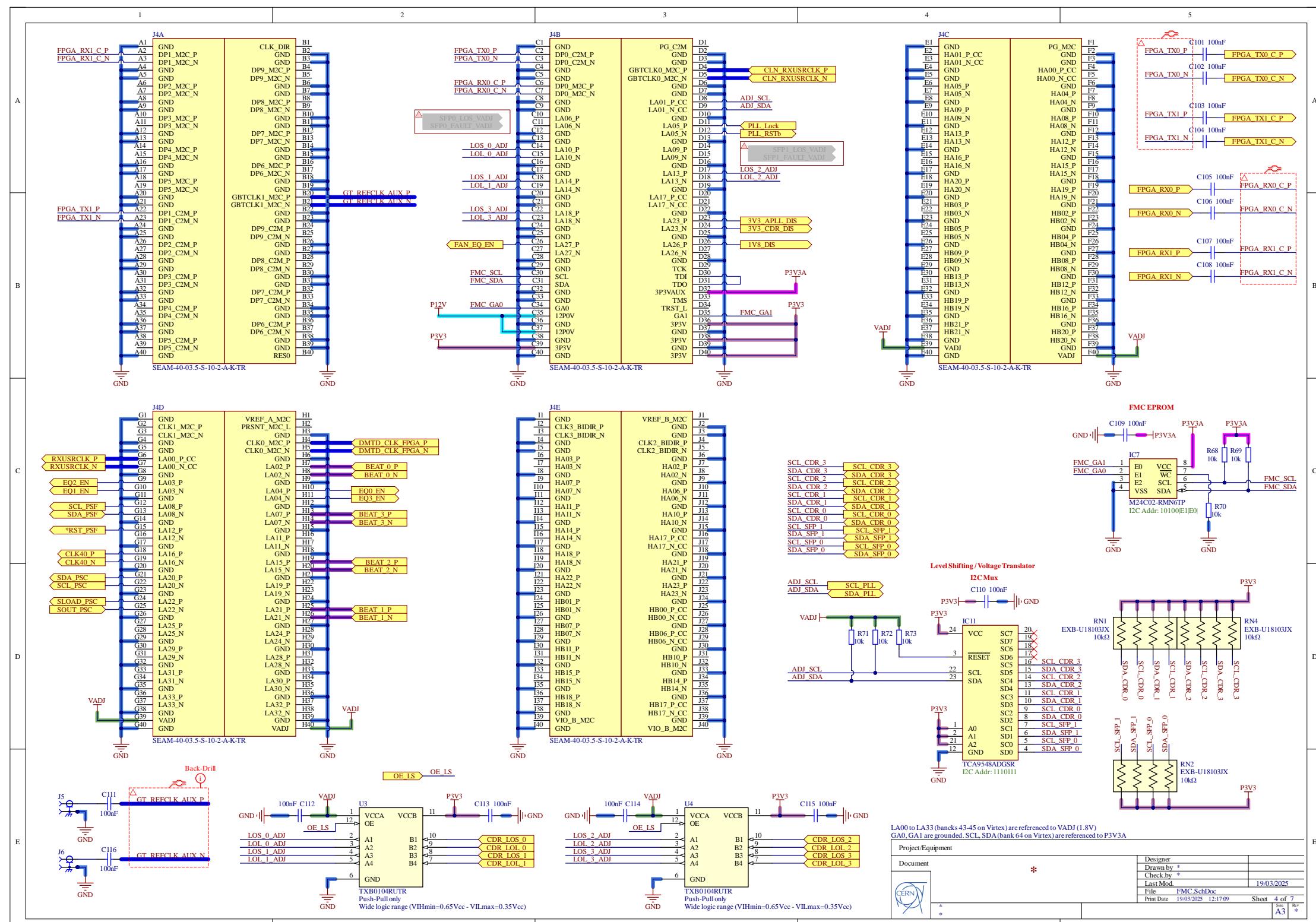
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Temperature Sensor



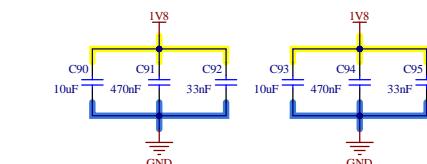
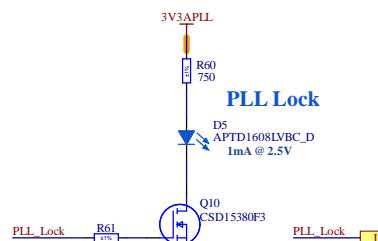
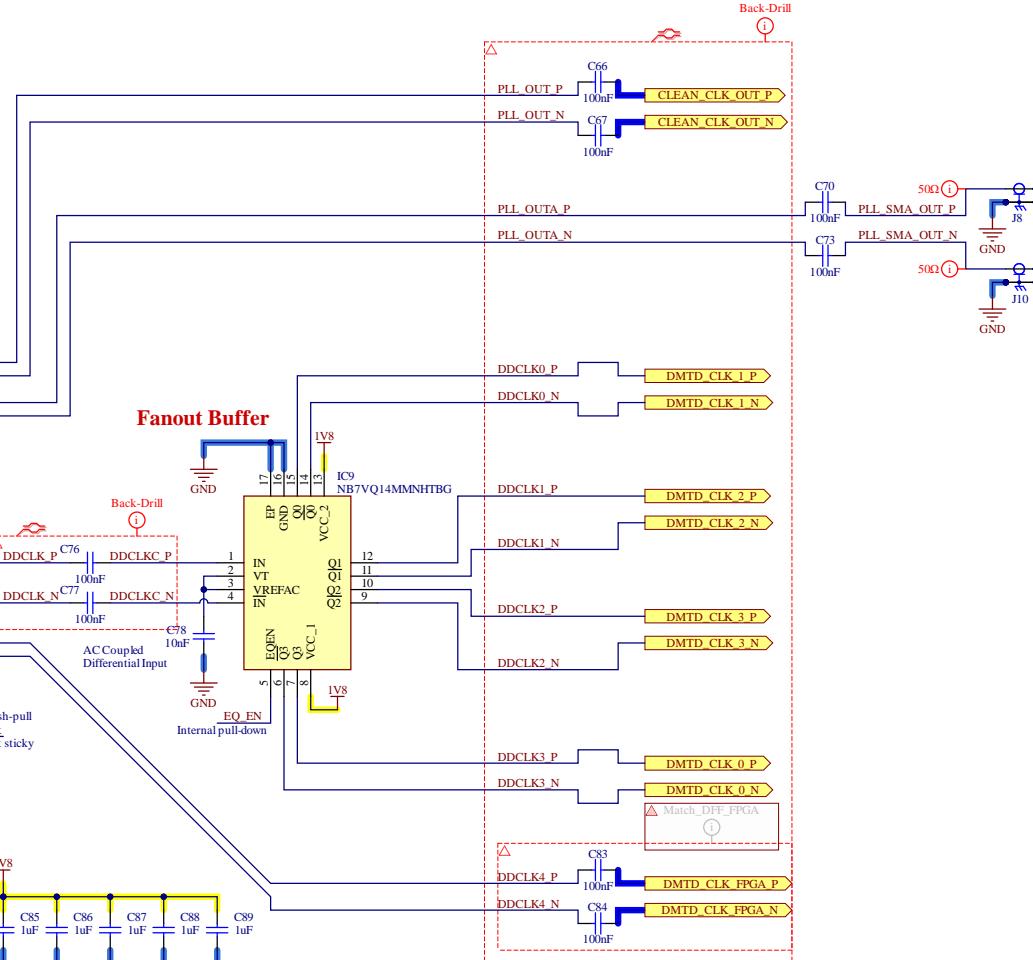
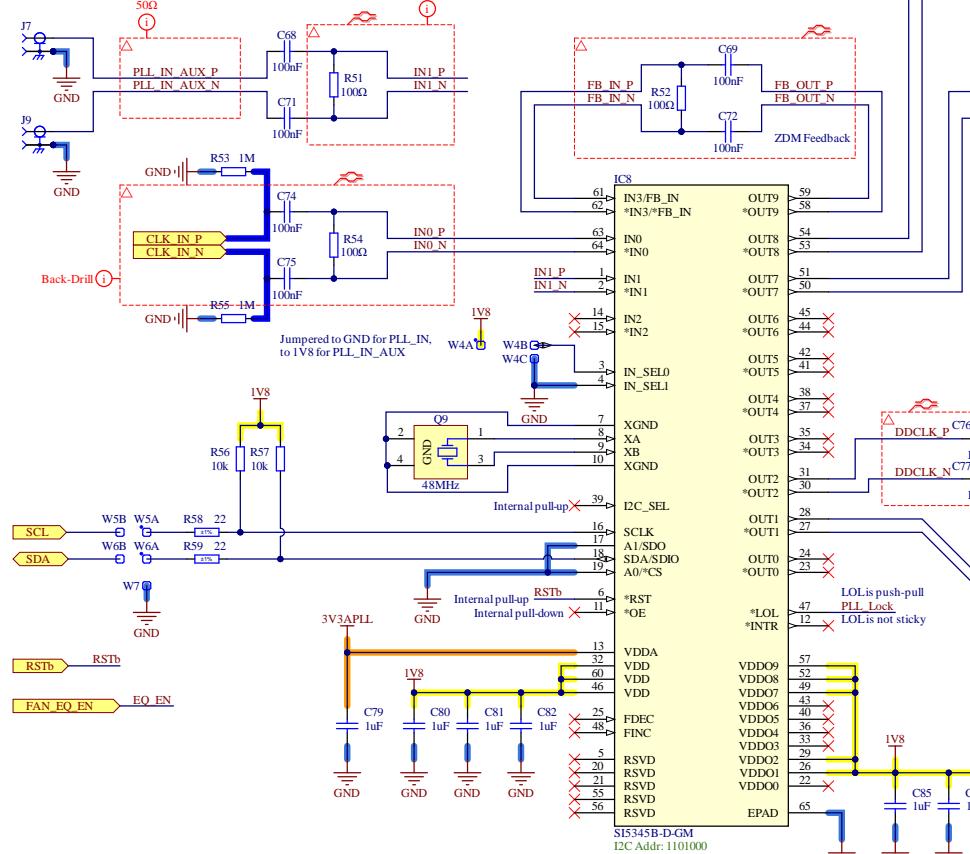
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Print Date 19.03.2025 12:17:09		Sheet 3 of 7	
		Rev A3	*



LA00 to LA33 (banks 43-45 on Virtex) are referenced to VADJ (1.8V)
GA0, GA1 are grounded. SCL, SDA (bank 64 on Virtex) are referenced to P3V3A

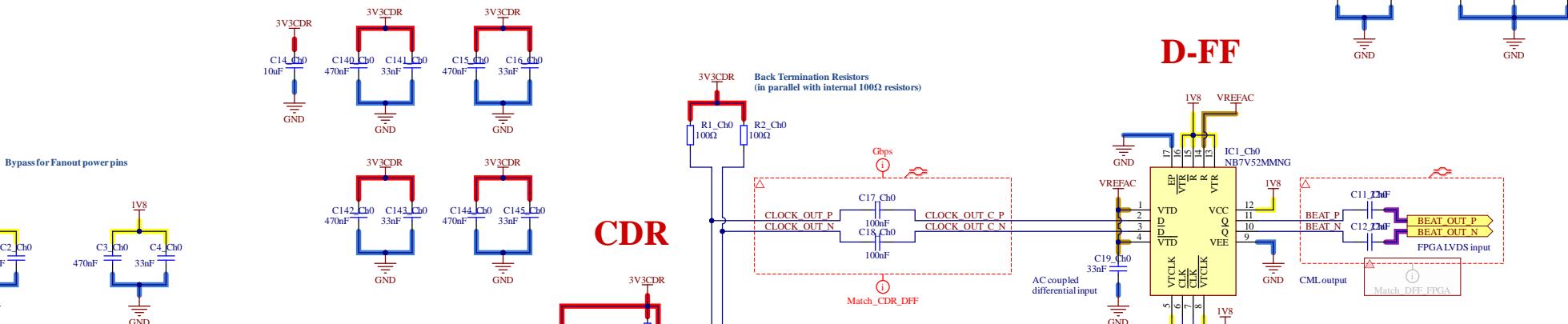
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Jitter Cleaner PLL

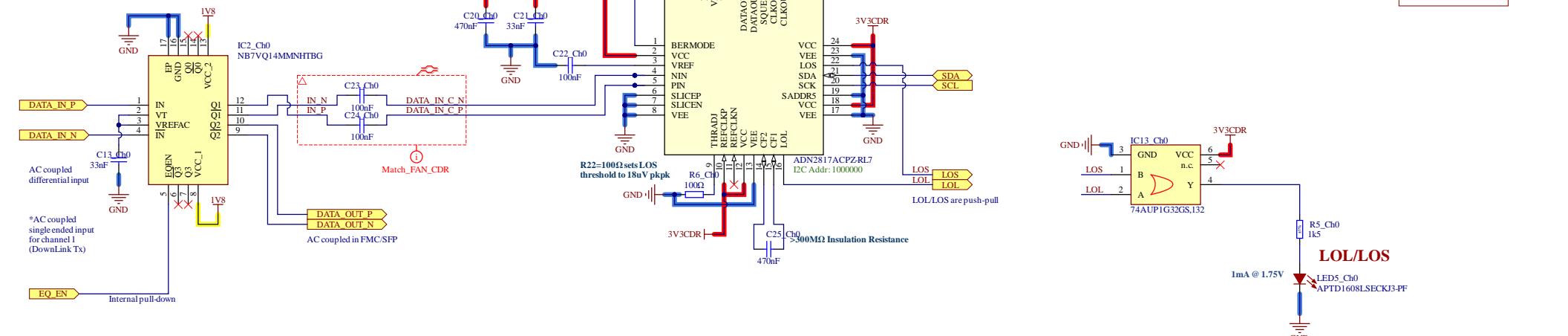


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Bypass for D-FF power pins



Fanout Buffer



Project/Equipment Phase Stable Link

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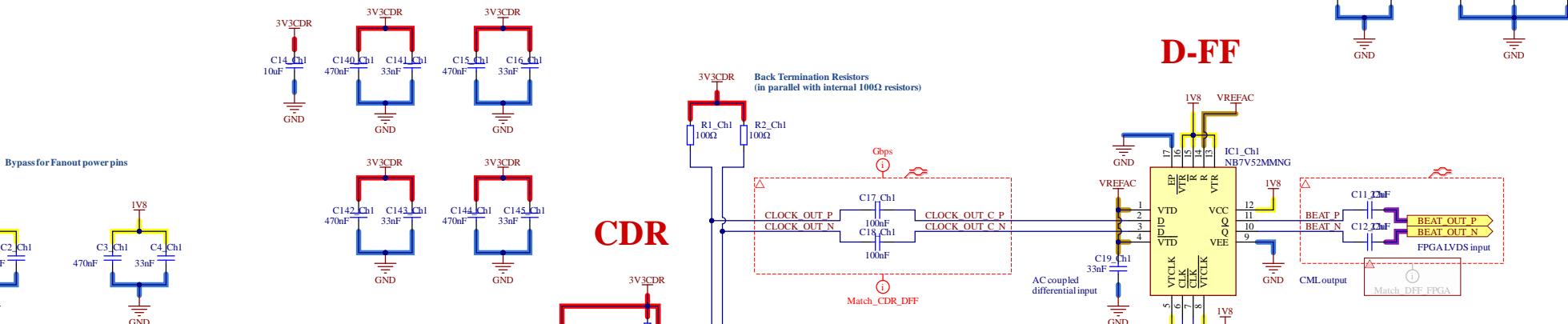


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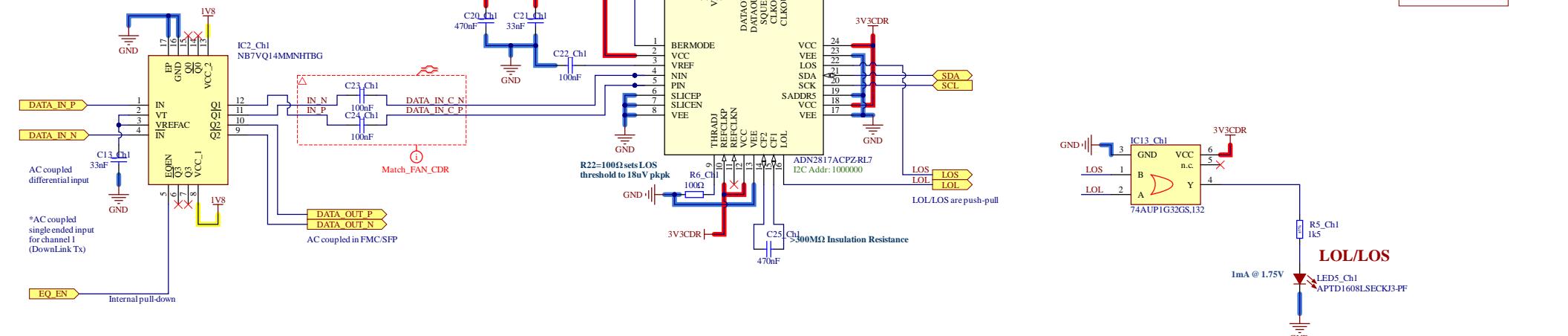
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Check by: E.Orzes F.Martina S.Baron	
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Size:	A3 Rev: 1.0

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CERN Geneva 23 - Switzerland

Bypass for D-FF power pins



Fanout Buffer



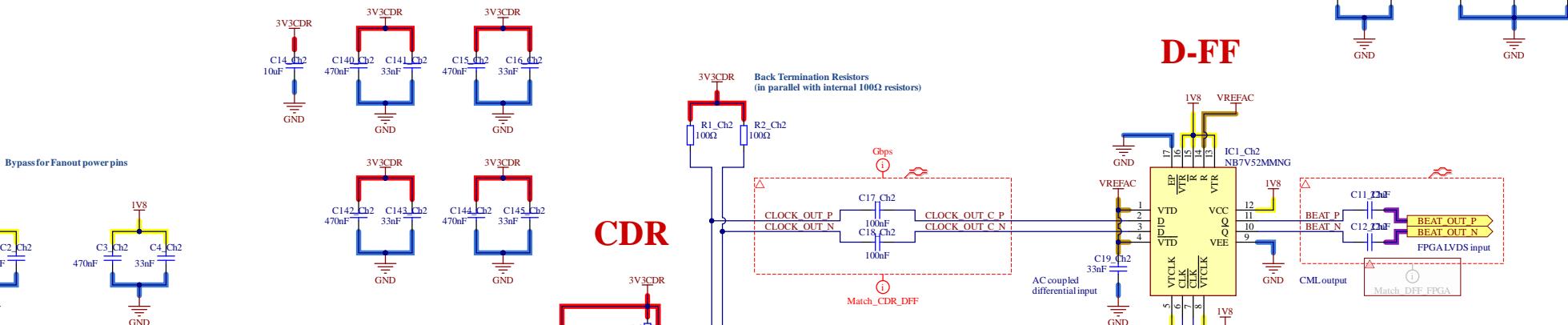
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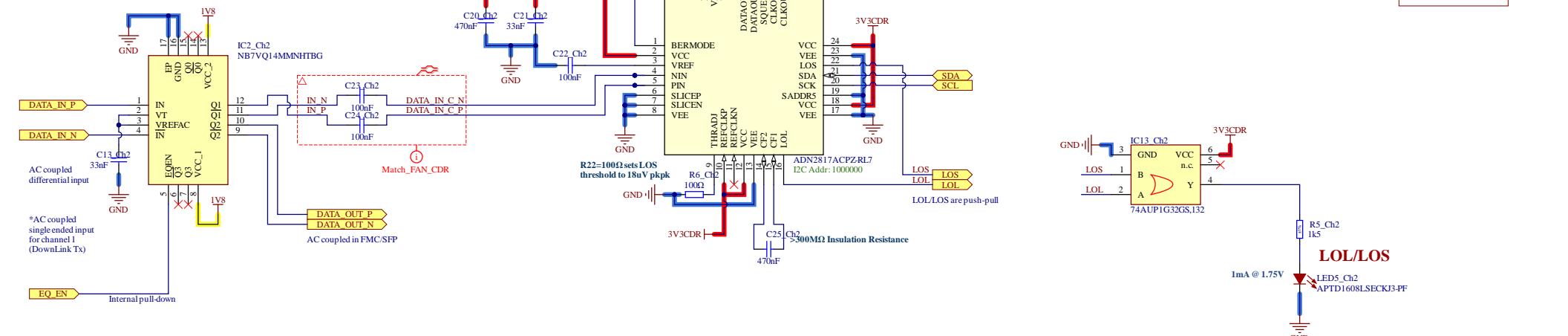
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Bypass for D-FF power pins



Fanout Buffer



Project/Equipment Phase Stable Link

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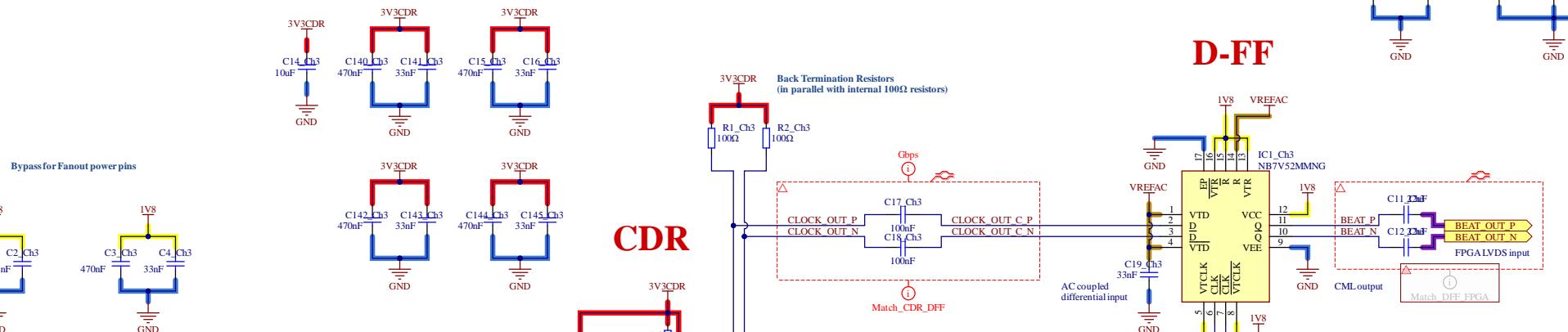


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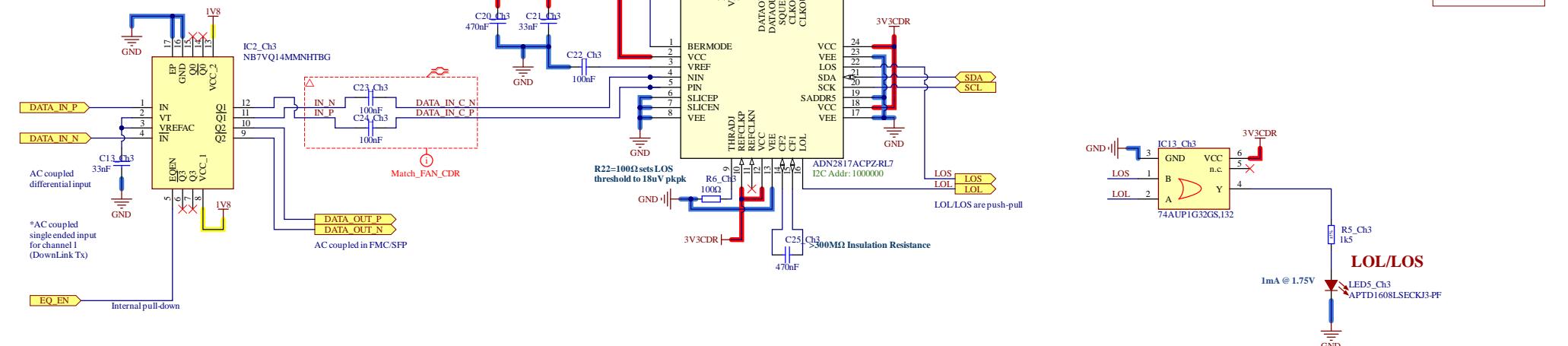
CDR, Fanout, D-FF

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Bypass for D-FF power pins



Fanout Buffer



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Document EP-ESE



CDR, Fanout, D-FF

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Rev A3	Size 1.0

