Dedicated to GT 0 (Channel 0) on Quad 0 and SFP 0

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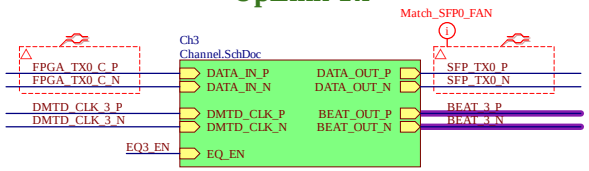

Dedicated to GT 1 (Channel 1) on Quad 0 and SFP 1

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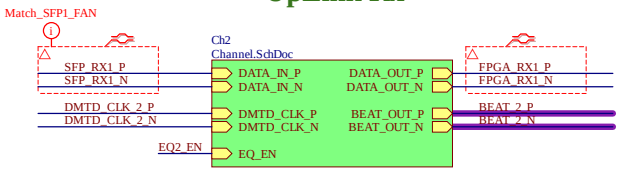

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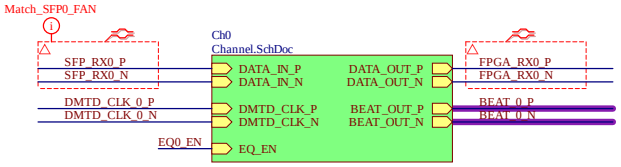

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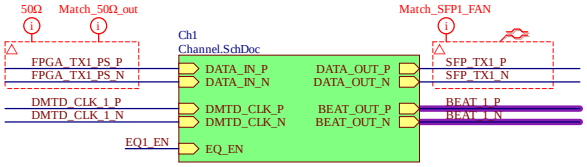

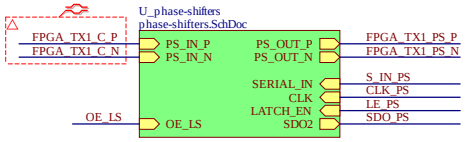

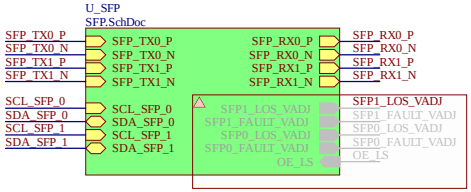

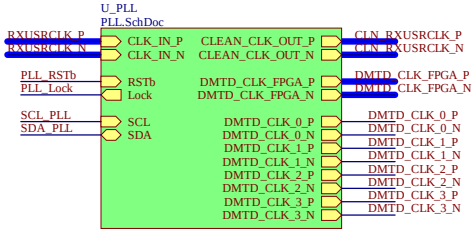

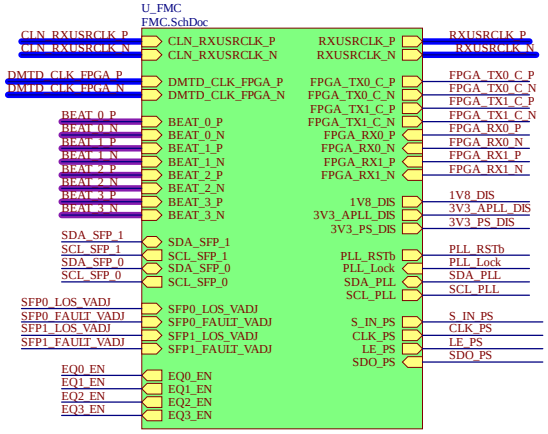

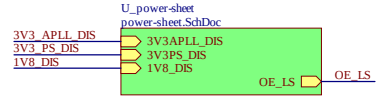

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5. Automatic cross reference disabled

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Rev	*

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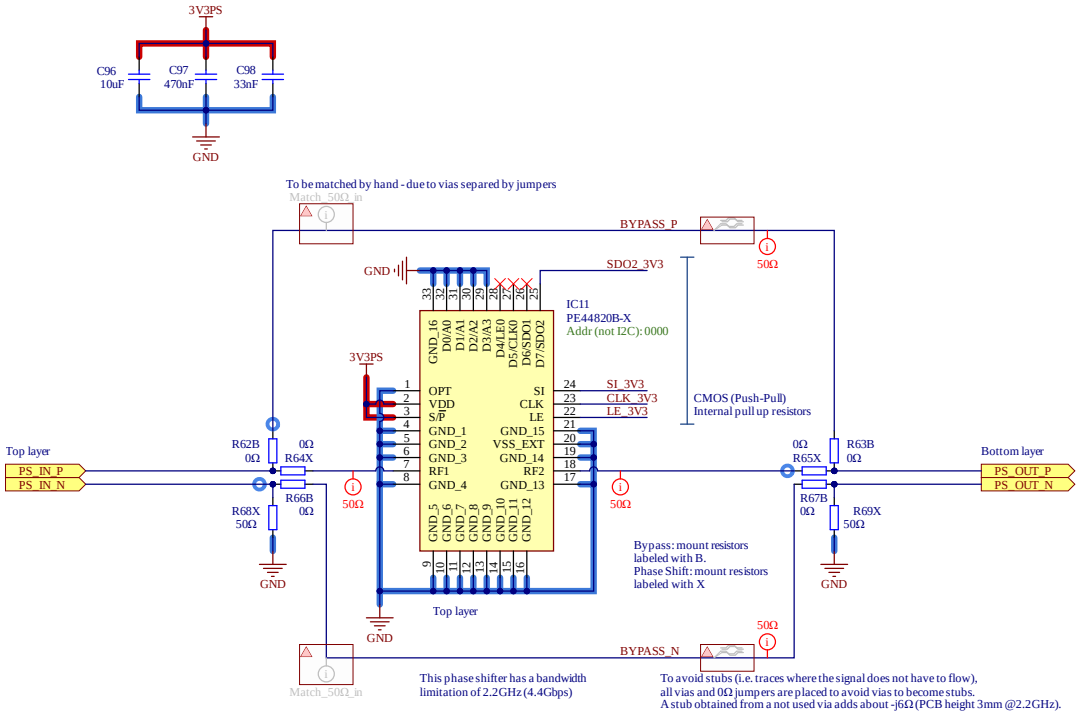

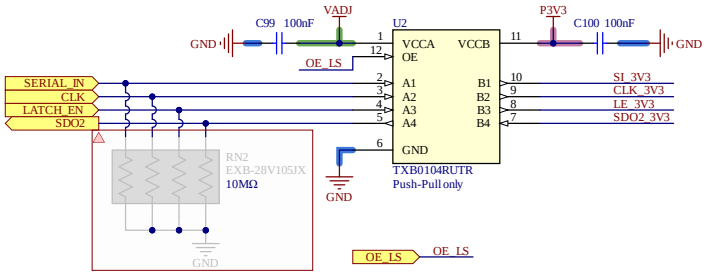

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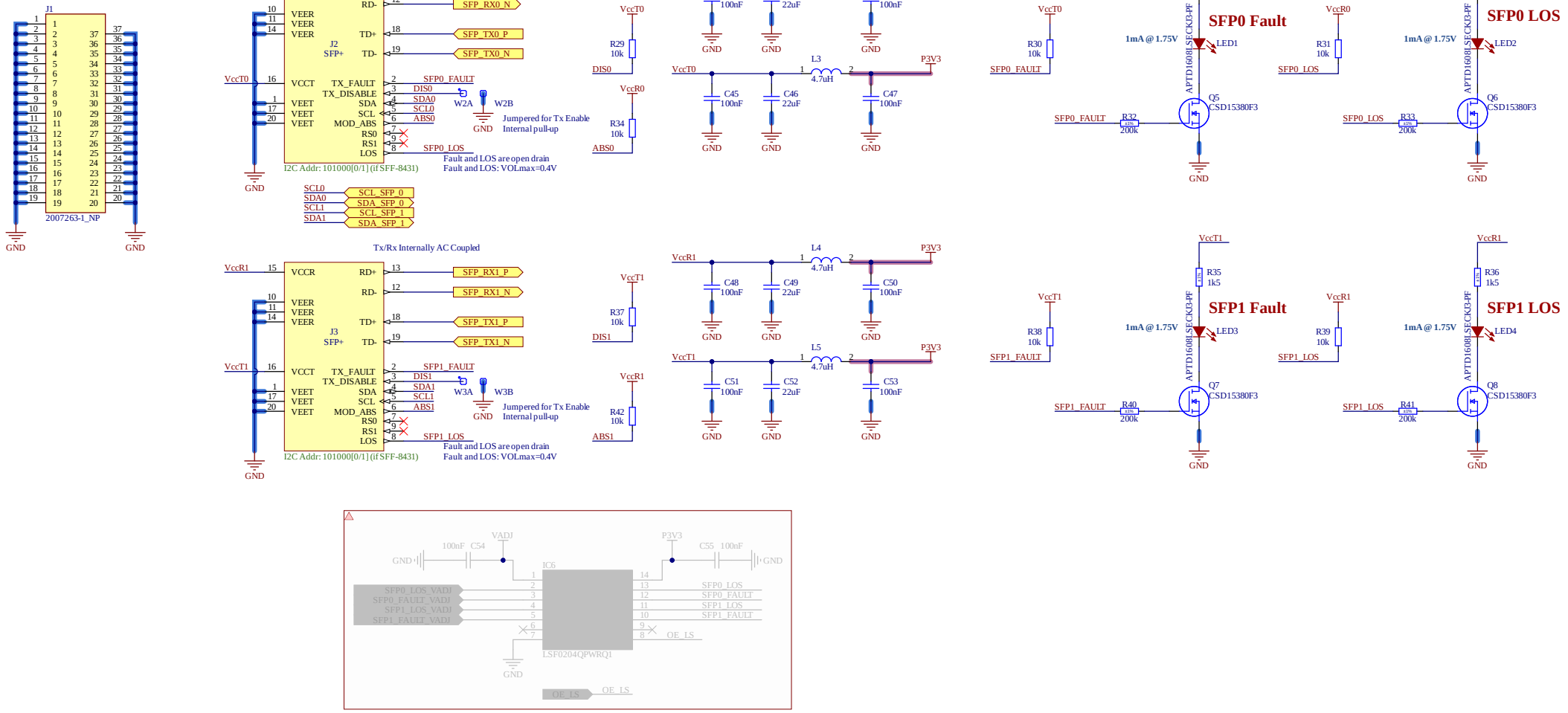

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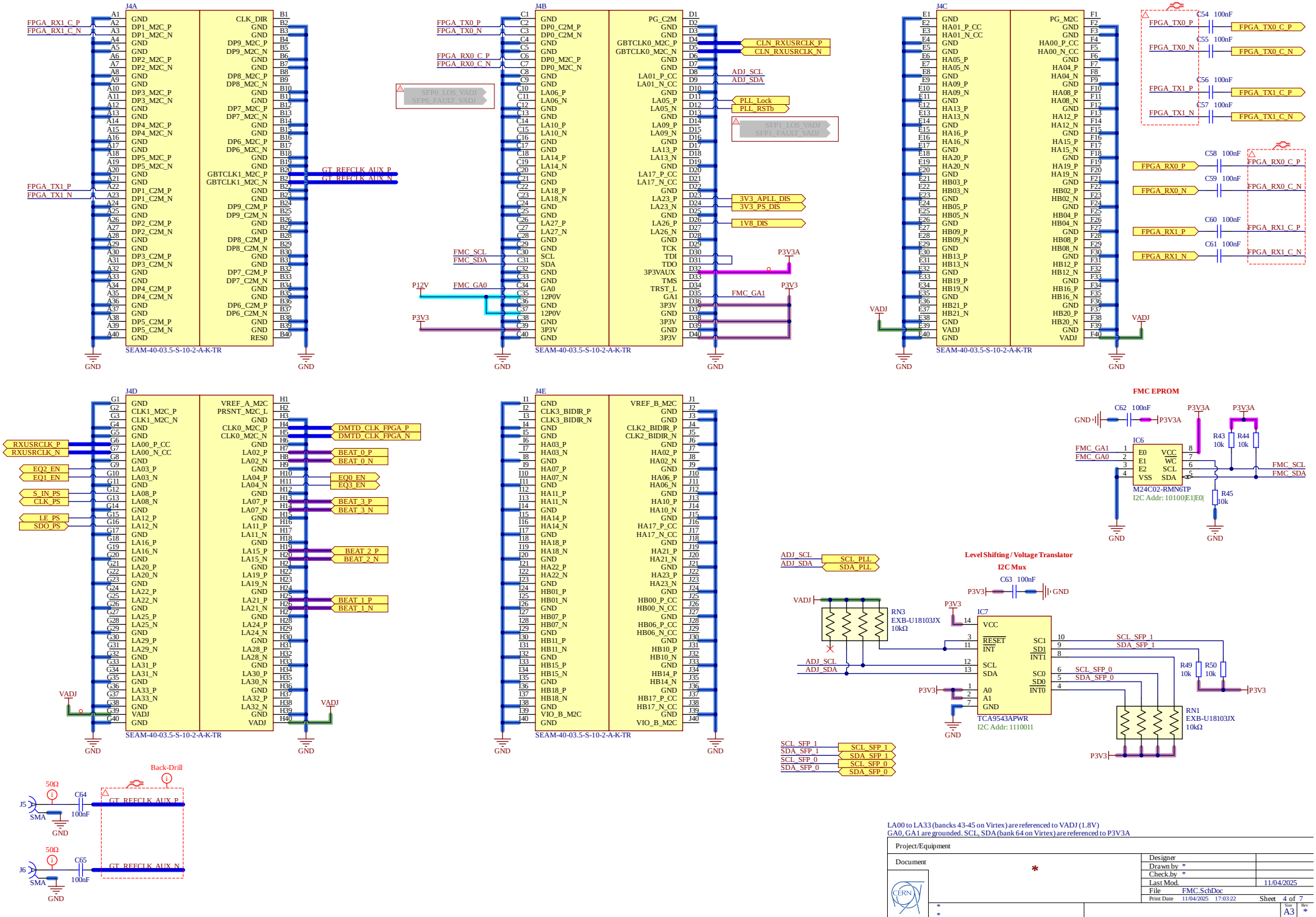
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GT_REFCLK_AUX_P
GT_REFCLK_AUX_N
J4B
SEAM-40-03.5-S-10-2-A-K-TR
FPGA_TX0_P
FPGA_TX0_N
FPGA_RX0_C_P
FPGA_RX0_C_N
SFP0_LOS_VADJ
SFP0_FAULT_VADJ
CLN_RXUSRCLK_P
CLN_RXUSRCLK_N
ADJ_SCL
ADJ_SDA
PLL_Lock
PLL_RSTb
SFP1_LOS_VADJ
SFP1_FAULT_VADJ
3V3_APLL_DIS
3V3_PS_DIS
1V8_DIS
FMC_SCL
FMC_SDA
FMC_GA0
FMC_GA1
P12V
P3V3A
P3V3
J4C
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VADJ
C54 100nF
C55 100nF
C56 100nF
C57 100nF
C58 100nF
C59 100nF
C60 100nF
C61 100nF
J4D
SEAM-40-03.5-S-10-2-A-K-TR
RXUSRCLK_P
RXUSRCLK_N
EQ2_EN
EQ1_EN
S_IN_PS
CLK_PS
LE_PS
SDO_PS
DMTD_CLK_FPGA_P
DMTD_CLK_FPGA_N
BEAT_0_P
BEAT_0_N
EQ0_EN
EQ3_EN
BEAT_3_P
BEAT_3_N
BEAT_2_P
BEAT_2_N
BEAT_1_P
BEAT_1_N
J4E
SEAM-40-03.5-S-10-2-A-K-TR
FMC EPROM
IC6
M24C02-RMN6TP
I2C Addr: 10100|E1|E0|
C62 100nF
R43 10k
R44 10k
R45 10k
Level Shifting / Voltage Translator
I2C Mux
IC7
TCA9543APWR
I2C Addr: 1110011
RN3
EXB-U18103JX
10kΩ
RN1
EXB-U18103JX
10kΩ
C63 100nF
R49 10k
R50 10k
SCL_PLL
SDA_PLL
SCL_SFP_1
SDA_SFP_1
SCL_SFP_0
SDA_SFP_0
Back-Drill
50Ω
J5
J6
SMA
C64
C65
100nF
LA00 to LA33 (bancks 43-45 on Virtex) are referenced to VADJ (1.8V)
GA0, GA1 are grounded. SCL, SDA (bank 64 on Virtex) are referenced to P3V3A
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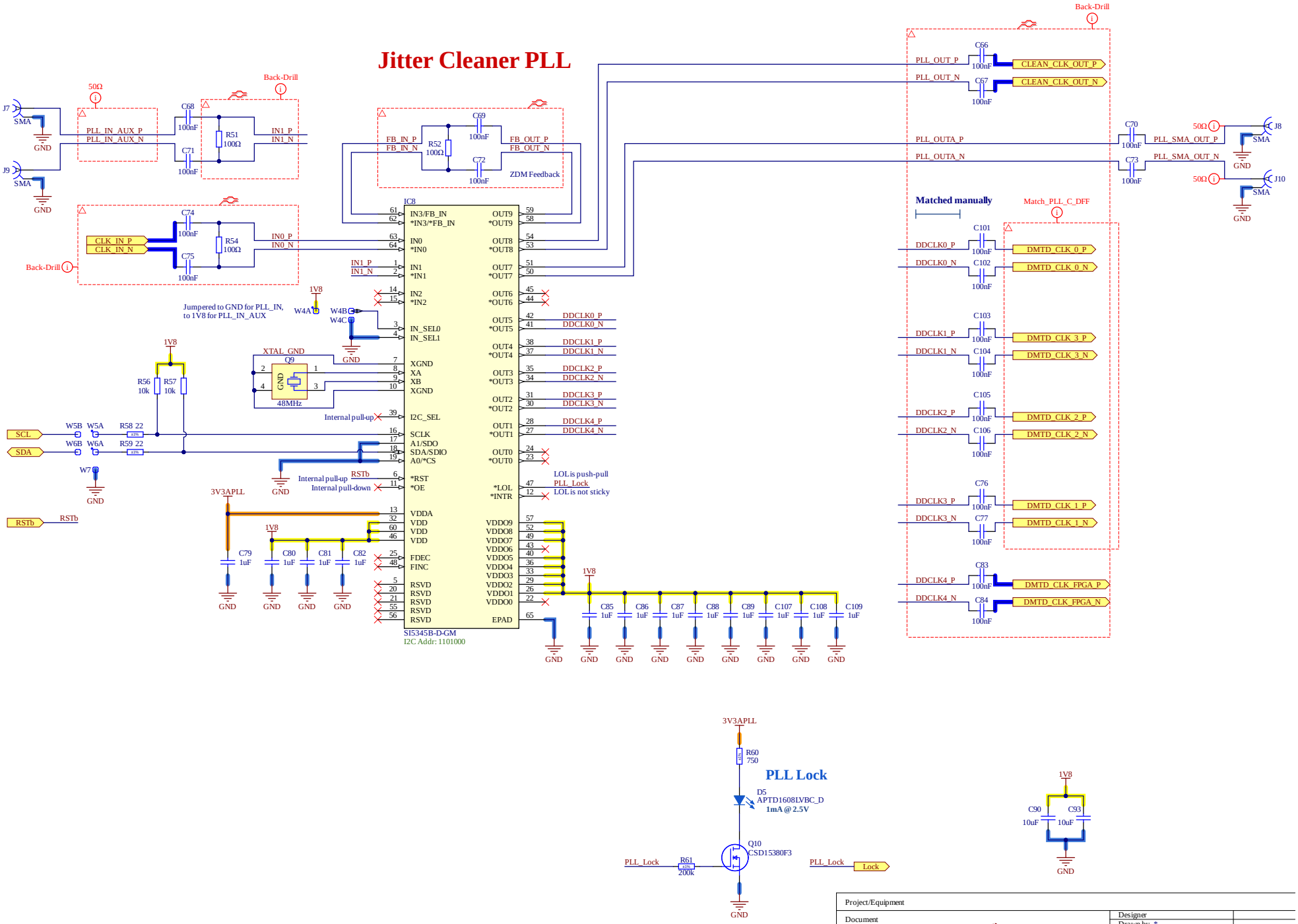
Jitter Cleaner PLL



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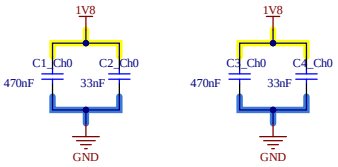
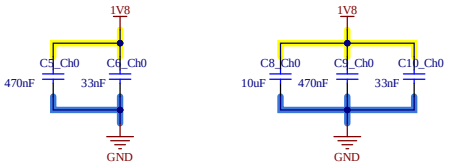
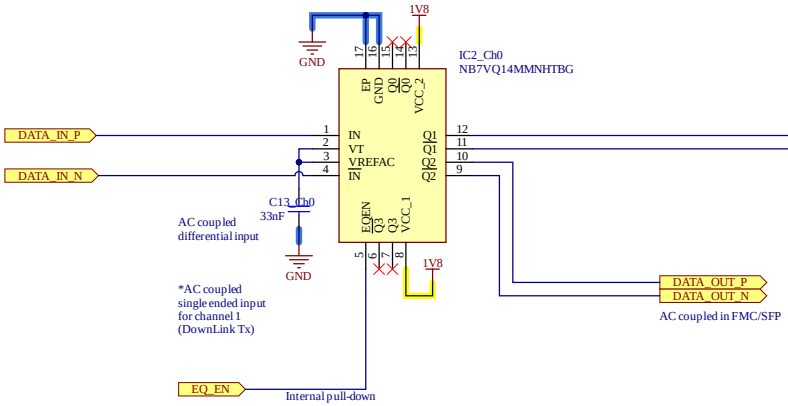
Bypass for Fanout power pins

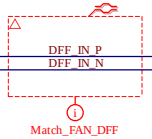


Bypass for D-FF power pins



Fanout Buffer





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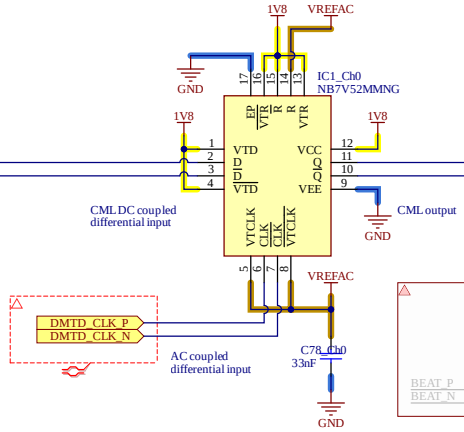

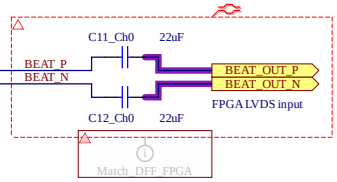

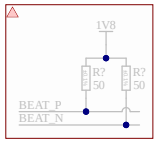

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		Check.by	E.Orzes F.Martina S.Baron
		Last Mod.	03/04/2025
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EP-ESE / CERN	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	Size	A3
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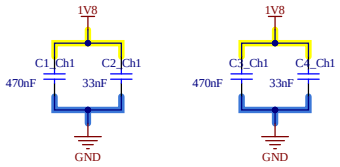
Bypass for Fanout power pins



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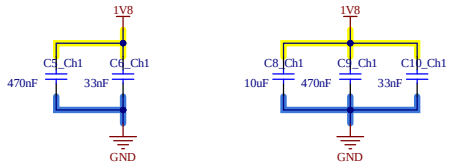

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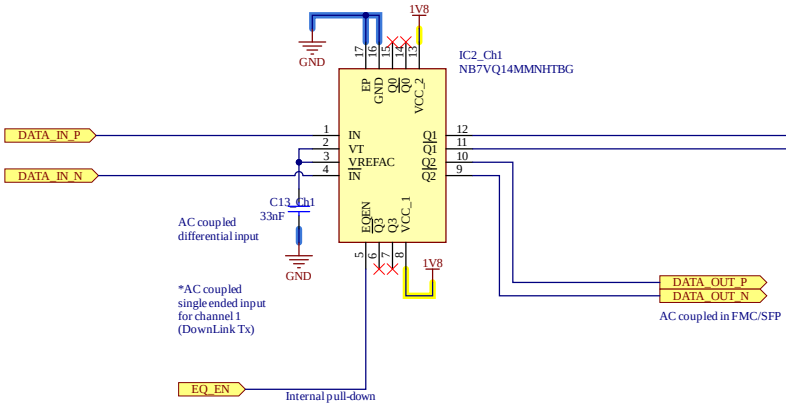

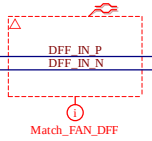

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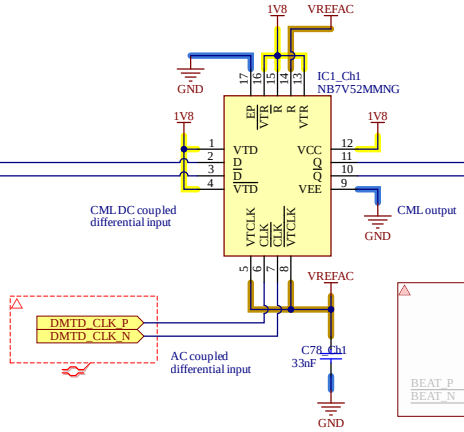

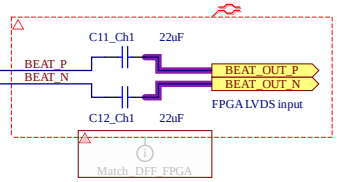

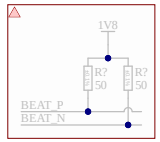

Project/Equipment	Phase Stable Link		
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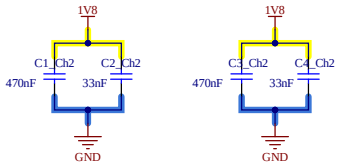
Bypass for Fanout power pins



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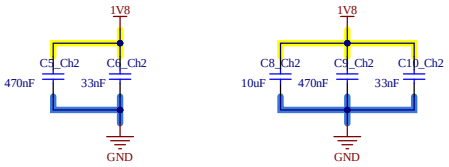

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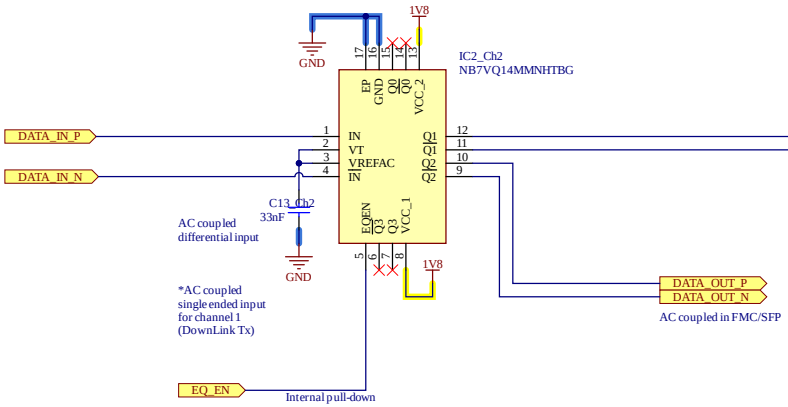

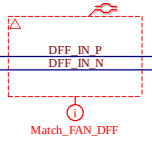

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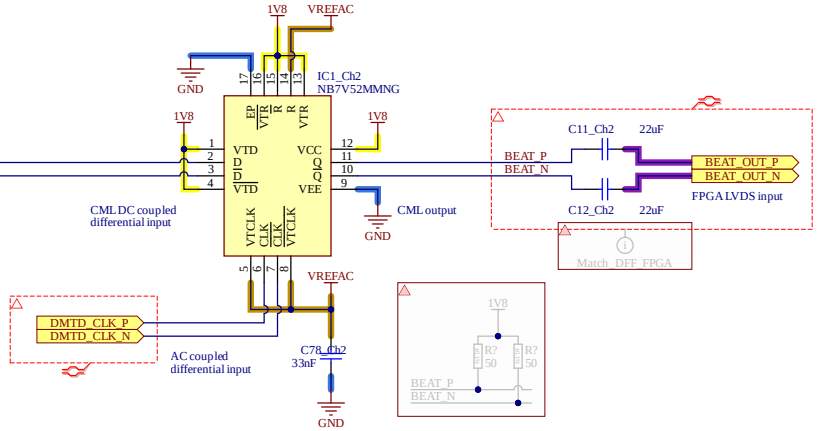

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		Check.by	E.Orzes F.Martina S.Baron
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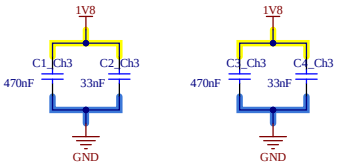
Bypass for Fanout power pins



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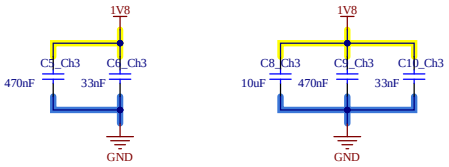

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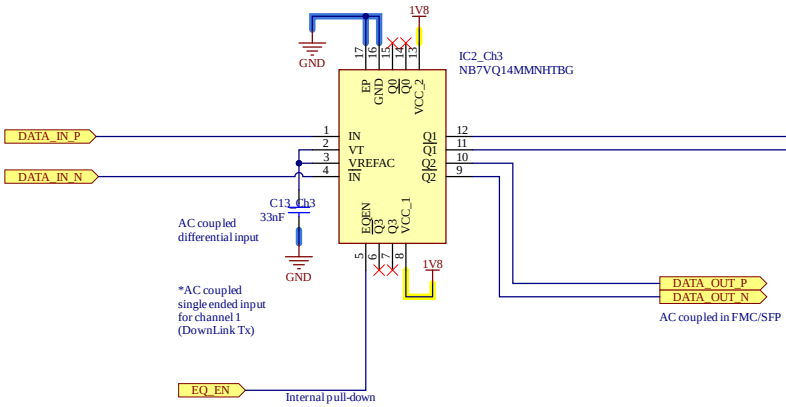

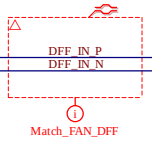

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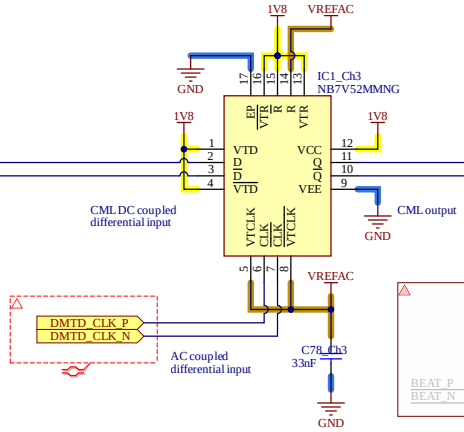

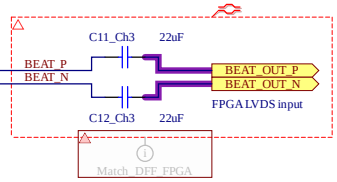

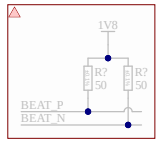

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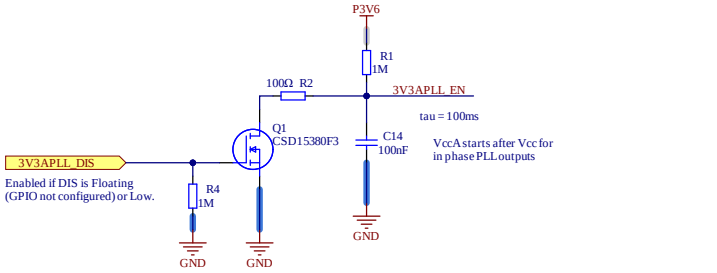
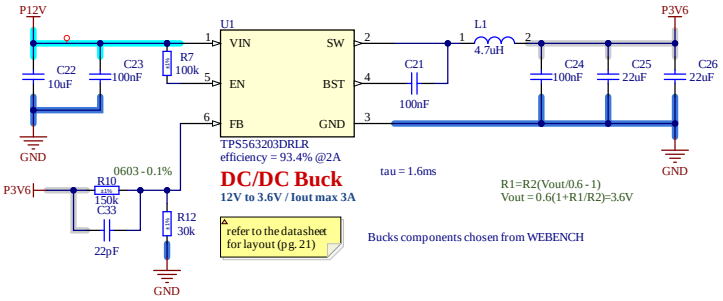
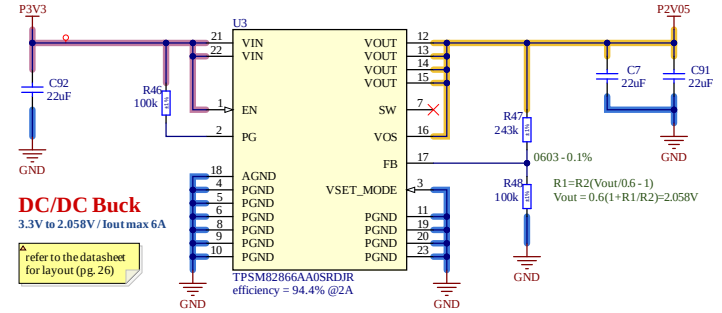
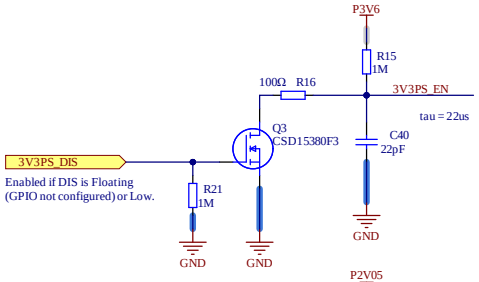
CH-1211 Genève 23 - Switzerland

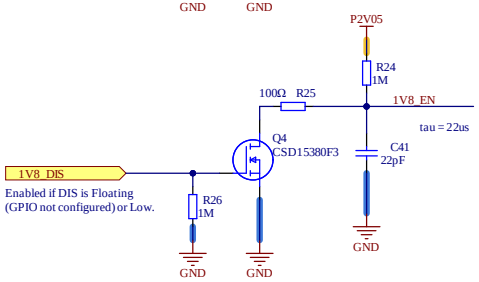
Linear Regulators

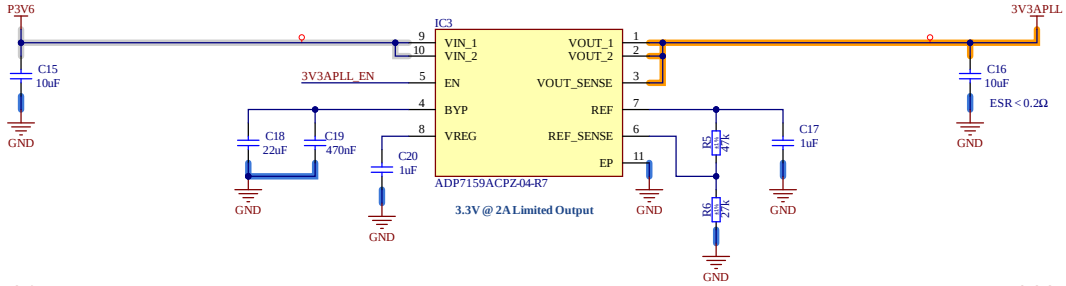


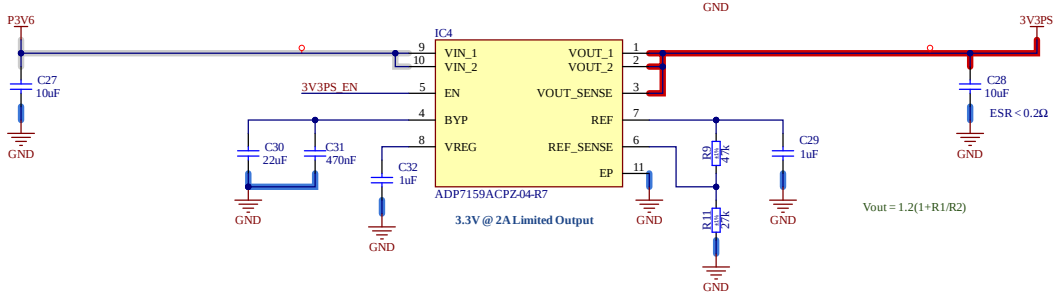


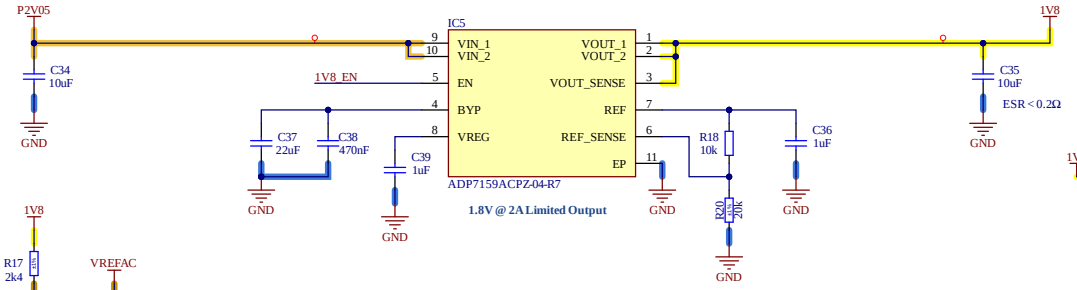


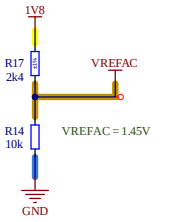


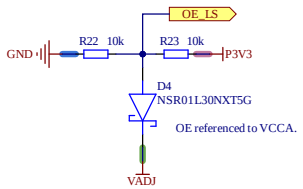












Project/Equipment	Phase Stable Link		
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