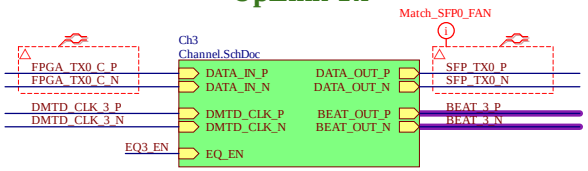
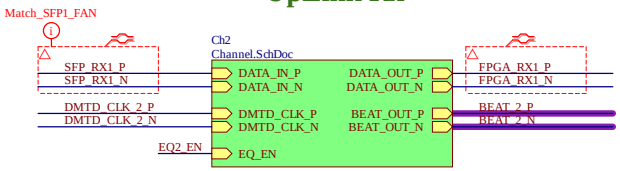
Dedicated to GT 0 (Channel 0) on Quad 0 and SFP 0

UpLink Tx

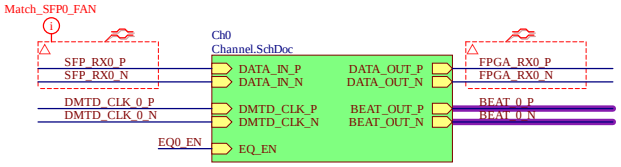


Dedicated to GT 1 (Channel 1) on Quad 0 and SFP 1

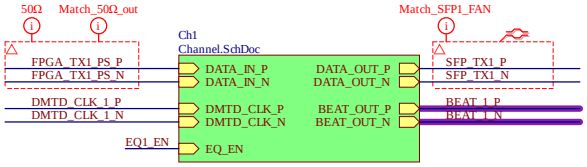
UpLink Rx

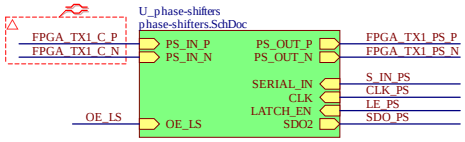


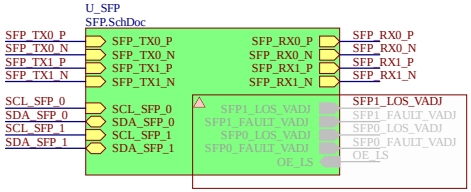
DownLink Rx

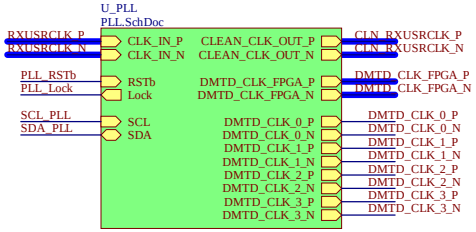


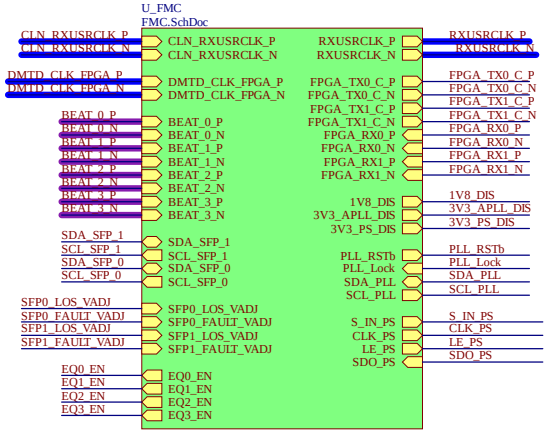
DownLink Tx

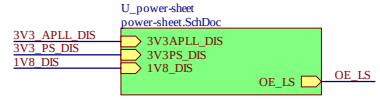












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3. Append sheet number to local nets (NO)
4. Net identifier scope: Automatic (Hierarchical)
5. Automatic cross reference disabled

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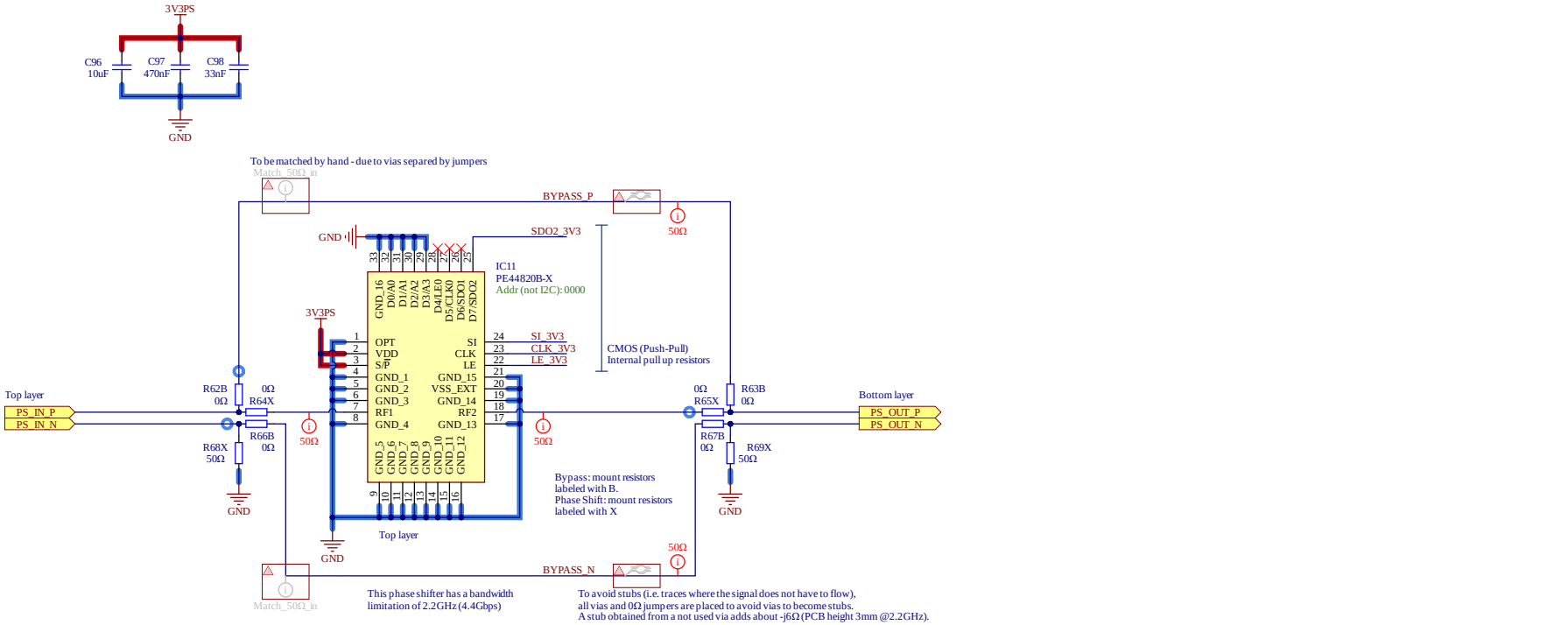

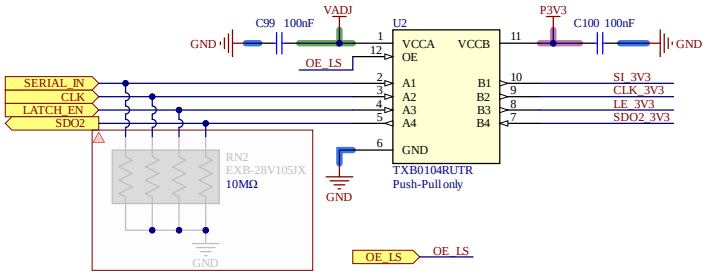

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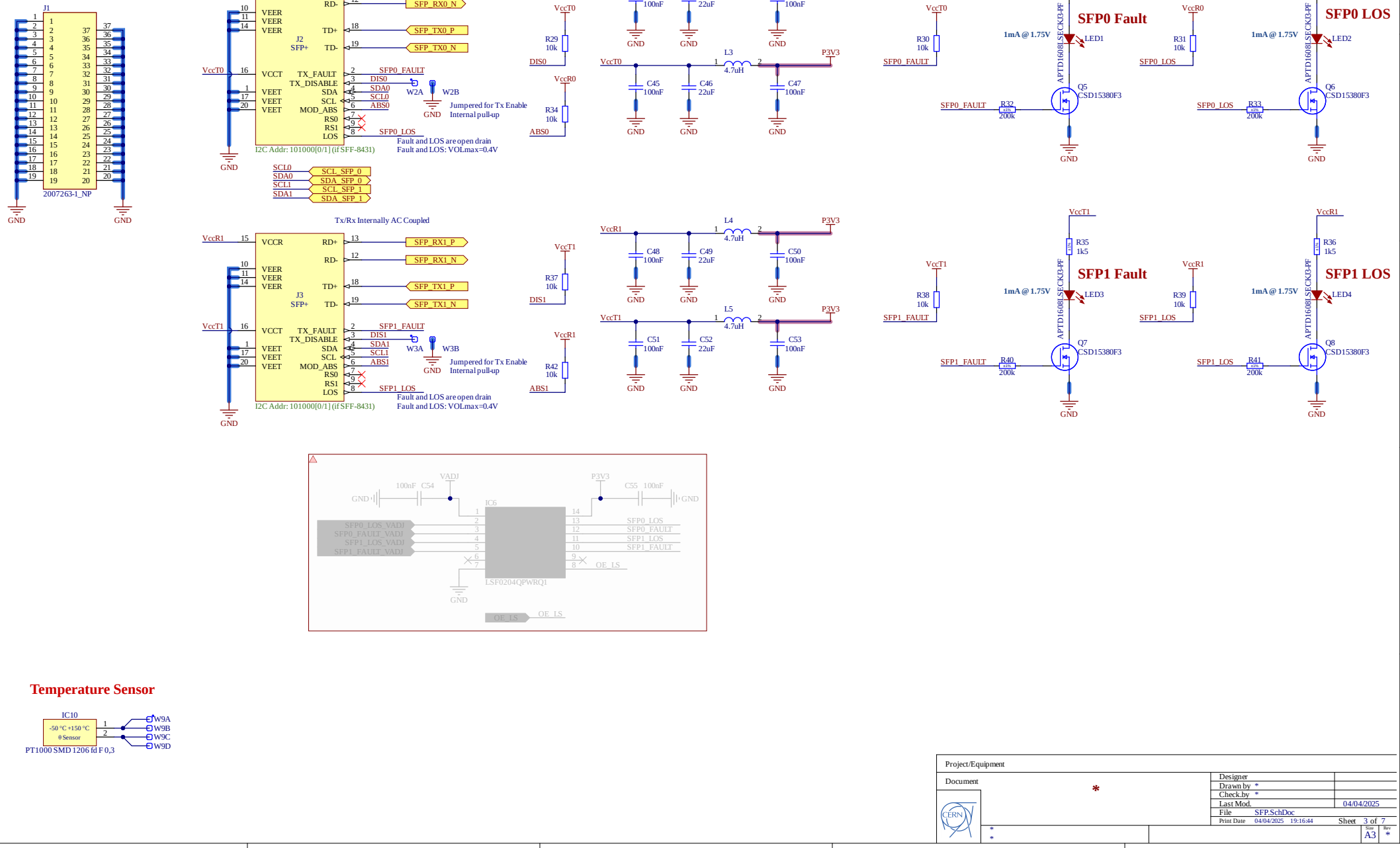

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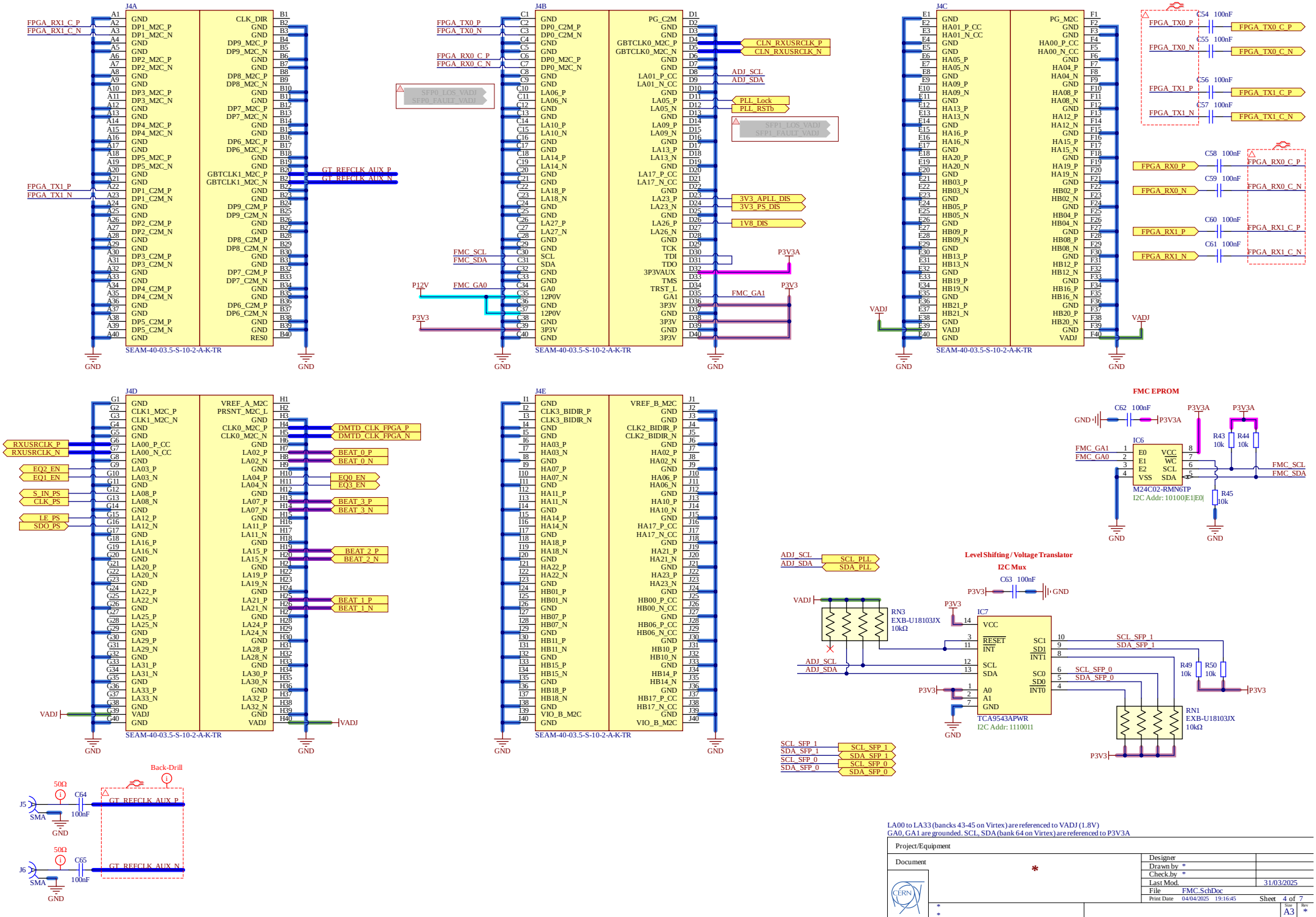
Rev	*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SEAM-40-03.5-S-10-2-A-K-TR
FPGA_RX1_C_P
FPGA_RX1_C_N
FPGA_TX1_P
FPGA_TX1_N
GT_REFCLK_AUX_P
GT_REFCLK_AUX_N
J4B
SEAM-40-03.5-S-10-2-A-K-TR
FPGA_TX0_P
FPGA_TX0_N
FPGA_RX0_C_P
FPGA_RX0_C_N
SFP0_LOS_VADJ
SFP0_FAULT_VADJ
CLN_RXUSRCLK_P
CLN_RXUSRCLK_N
ADJ_SCL
ADJ_SDA
PLL_Lock
PLL_RSTb
SFP1_LOS_VADJ
SFP1_FAULT_VADJ
3V3_APLL_DIS
3V3_PS_DIS
1V8_DIS
FMC_SCL
FMC_SDA
FMC_GA0
FMC_GA1
P12V
P3V3A
P3V3
J4C
SEAM-40-03.5-S-10-2-A-K-TR
VADJ
C54 100nF
C55 100nF
C56 100nF
C57 100nF
C58 100nF
C59 100nF
C60 100nF
C61 100nF
J4D
SEAM-40-03.5-S-10-2-A-K-TR
RXUSRCLK_P
RXUSRCLK_N
EQ2_EN
EQ1_EN
S_IN_PS
CLK_PS
LE_PS
SDO_PS
DMTD_CLK_FPGA_P
DMTD_CLK_FPGA_N
BEAT_0_P
BEAT_0_N
EQ0_EN
EQ3_EN
BEAT_3_P
BEAT_3_N
BEAT_2_P
BEAT_2_N
BEAT_1_P
BEAT_1_N
J4E
SEAM-40-03.5-S-10-2-A-K-TR
FMC EPROM
IC6
M24C02-RMN6TP
I2C Addr: 10100|E1|E0|
C62 100nF
R43 10k
R44 10k
R45 10k
Level Shifting / Voltage Translator
I2C Mux
IC7
TCA9543APWR
I2C Addr: 1110011
RN3
EXB-U18103JX
10kΩ
RN1
EXB-U18103JX
10kΩ
C63 100nF
R49 10k
R50 10k
SCL_PLL
SDA_PLL
SCL_SFP_1
SDA_SFP_1
SCL_SFP_0
SDA_SFP_0
Back-Drill
50Ω
C64
100nF
C65
100nF
J5
J6
SMA
GND
LA00 to LA33 (bancks 43-45 on Virtex) are referenced to VADJ (1.8V)
GA0, GA1 are grounded. SCL, SDA (bank 64 on Virtex) are referenced to P3V3A
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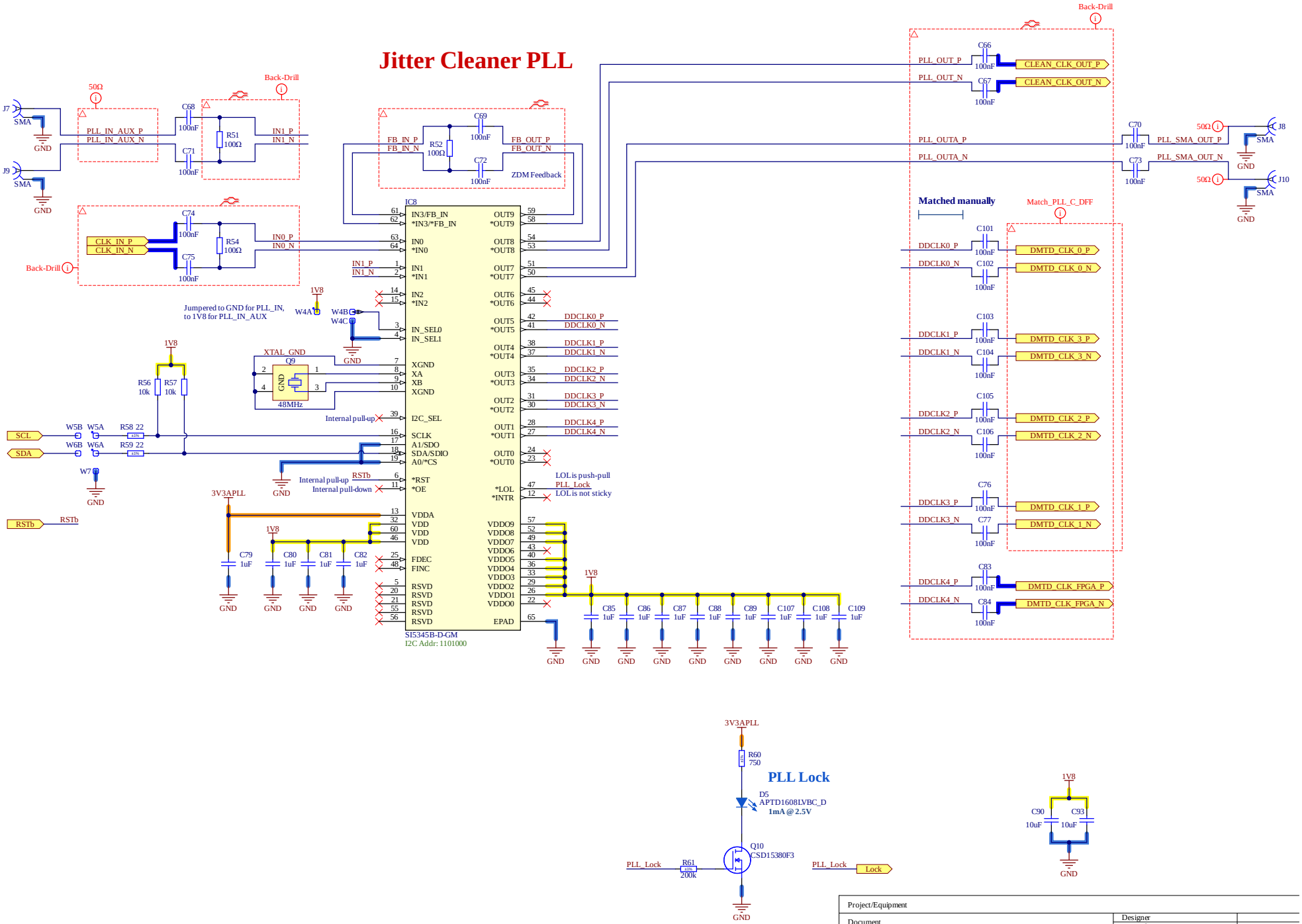
Rev *

Jitter Cleaner PLL



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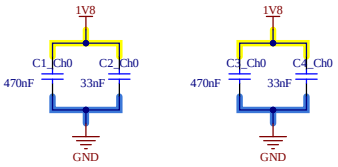
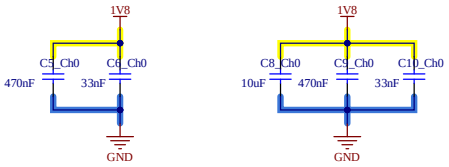
Rev	*

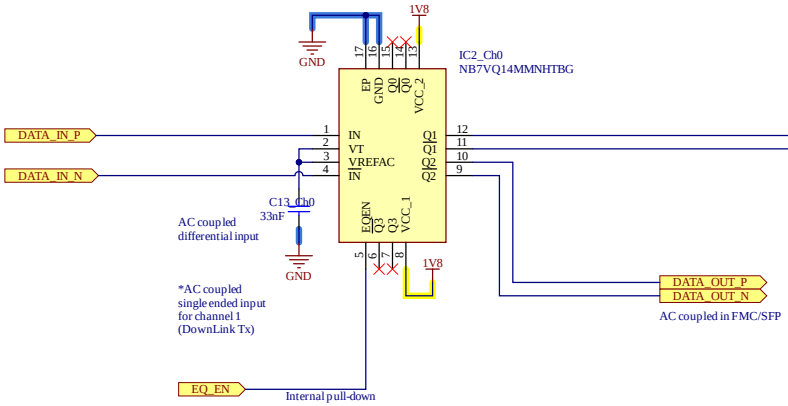
Bypass for Fanout power pins

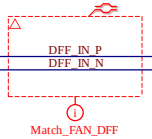


Bypass for D-FF power pins



Fanout Buffer





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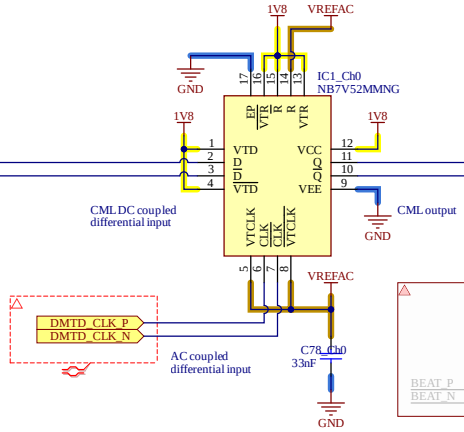

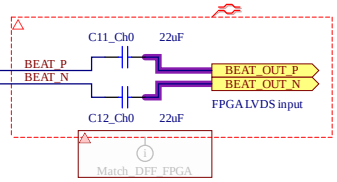

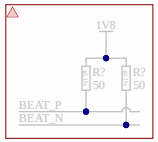

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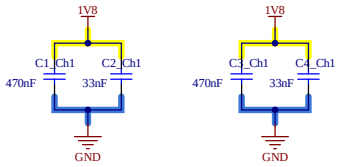
EP-ESE	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	Size	A3
		Rev	1.0

Bypass for Fanout power pins



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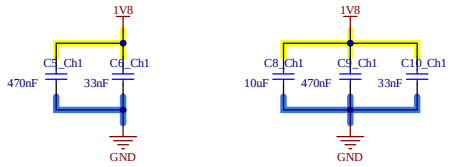

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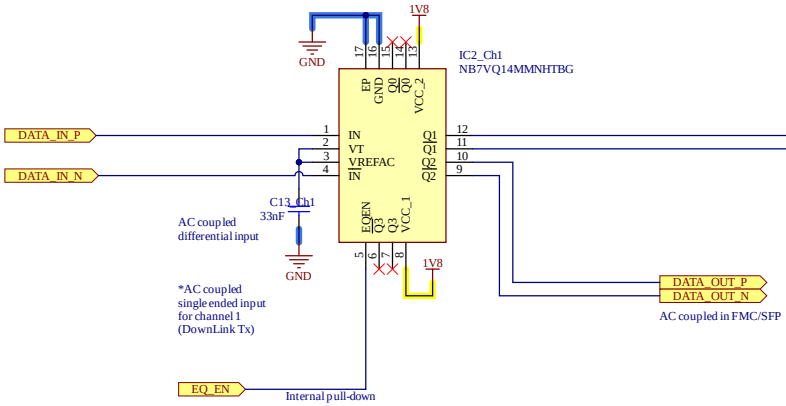

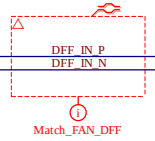

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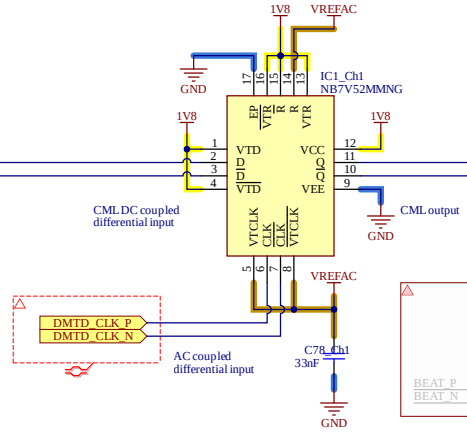

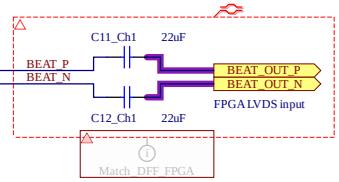

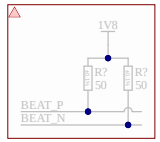

Project/Equipment	Phase Stable Link		
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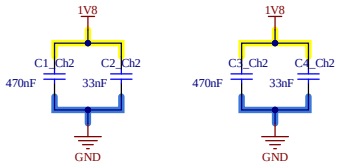
EP-ESE	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	Size	A3
		Rev	1.0

Bypass for Fanout power pins



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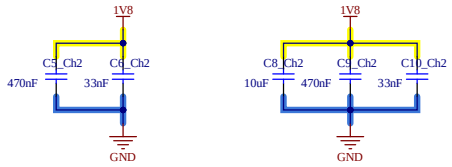

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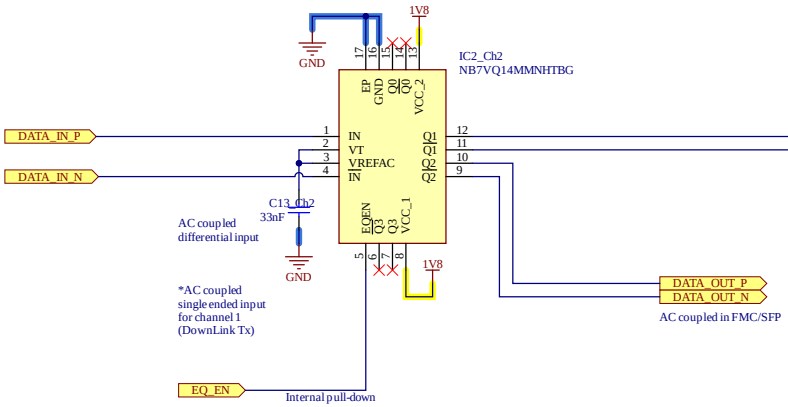

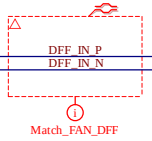

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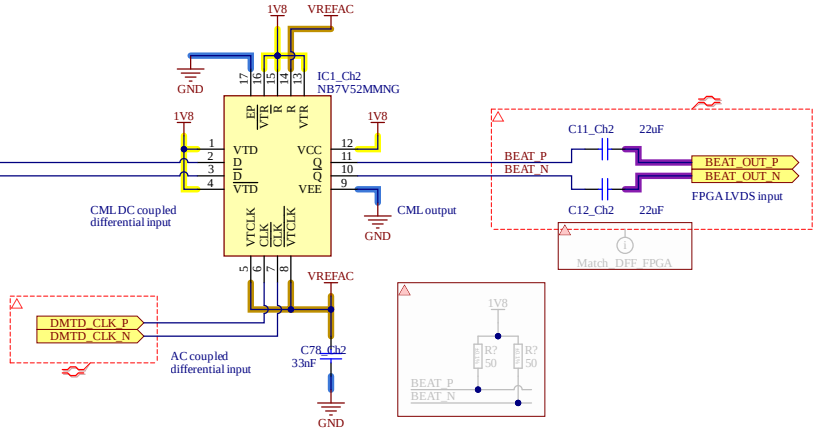

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		Check.by	E.Orzes F.Martina S.Baron
		Last Mod.	03/04/2025
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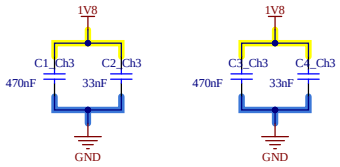
Bypass for Fanout power pins



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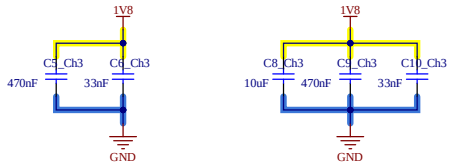

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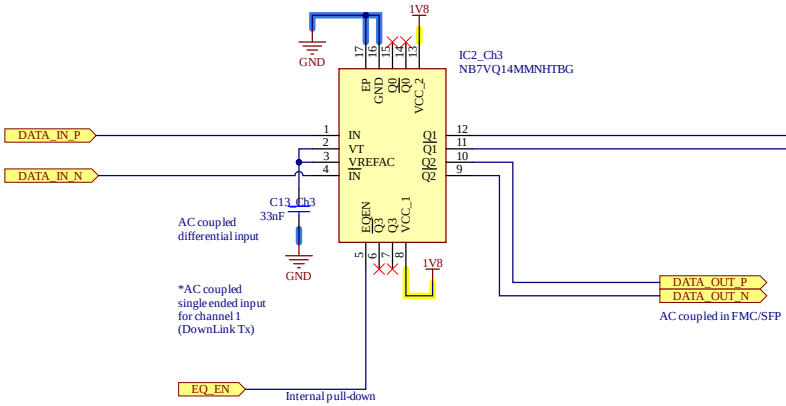

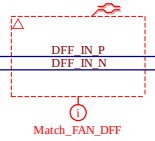

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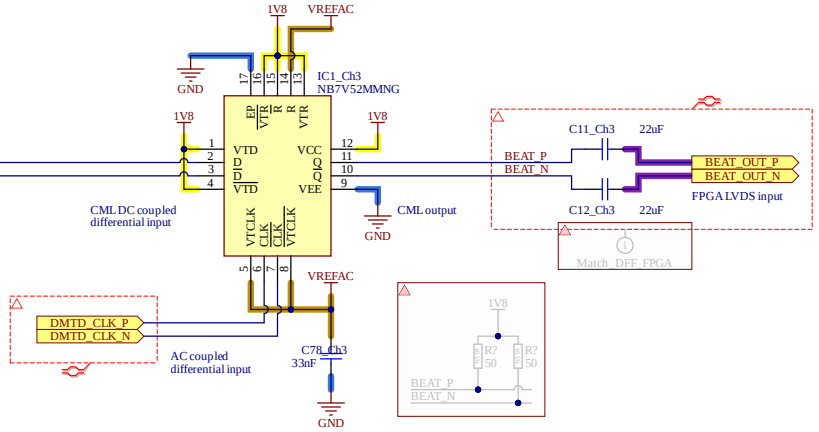

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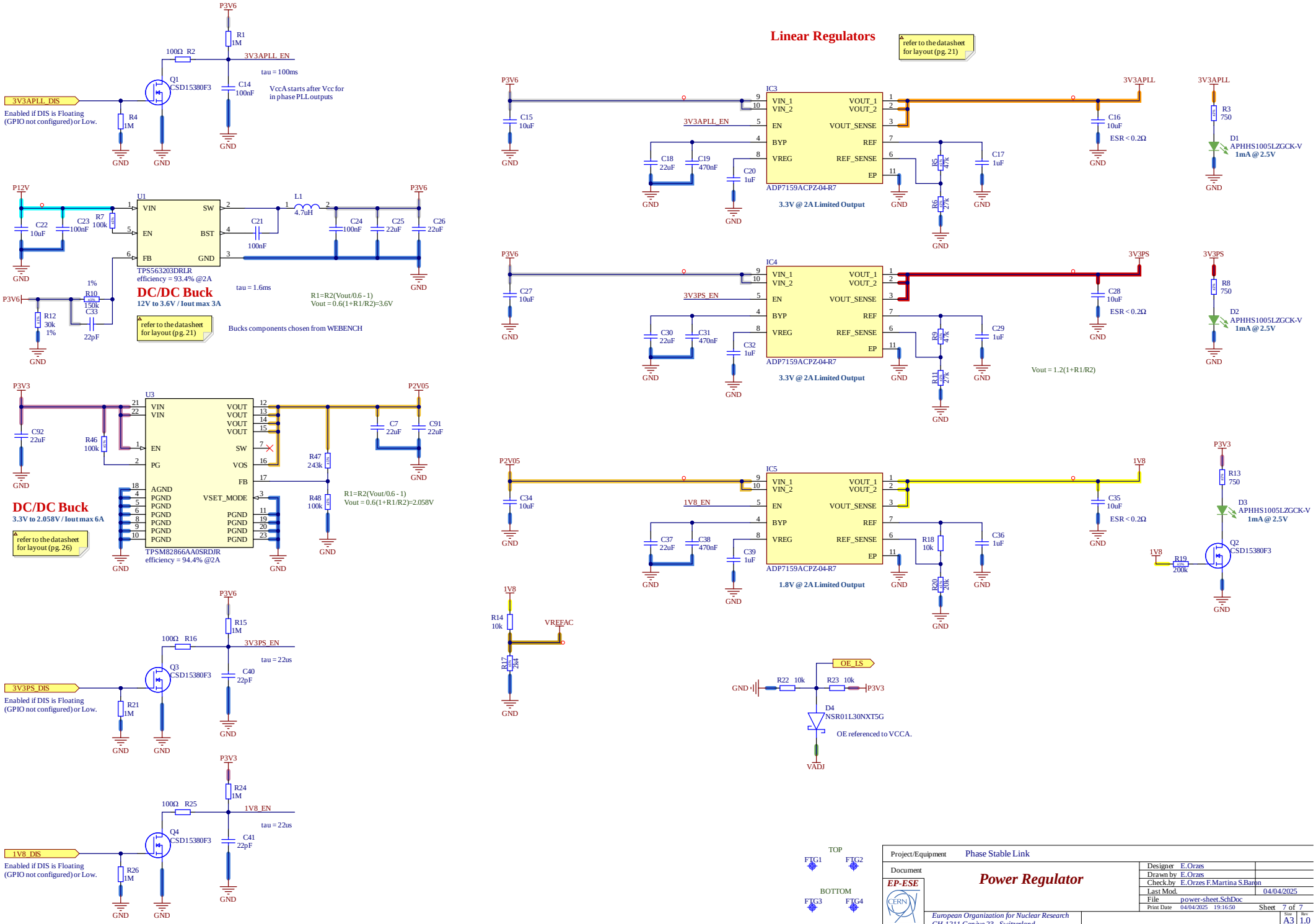
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland


Linear Regulators
refer to the datasheet for layout (pg. 21)
P3V6
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100Ω R2
3V3APLL_EN
tau = 100ms
Q1 CSD15380F3
C14 100nF
VccA starts after Vcc for in phase PLL outputs
3V3APLL_DIS
Enabled if DIS is Floating (GPIO not configured) or Low.
R4 1M
GND
P12V
U1
VIN
SW
EN
BST
FB
GND
L1 4.7uH
C22 10uF
C23 100nF
R7 100k
C21 100nF
C24 100nF
C25 22uF
C26 22uF
TPS563203DRLR
efficiency = 93.4% @2A
DC/DC Buck
12V to 3.6V / Iout max 3A
tau = 1.6ms
R1=R2(Vout/0.6 - 1)
Vout = 0.6(1+R1/R2)=3.6V
R10 150k 1%
R12 30k 1%
C33 22pF
refer to the datasheet for layout (pg. 21)
Bucks components chosen from WEBENCH
P3V3
U3
VIN
VOUT
EN
SW
PG
VOS
FB
AGND
PGND
VSET_MODE
C92 22uF
R46 100k
C7 22uF
C91 22uF
R47 243k
R48 100k
P2V05
TPSM82866AA0SRDJR
efficiency = 94.4% @2A
DC/DC Buck
3.3V to 2.058V / Iout max 6A
R1=R2(Vout/0.6 - 1)
Vout = 0.6(1+R1/R2)=2.058V
refer to the datasheet for layout (pg. 26)
IC3
VIN_1
VIN_2
VOUT_1
VOUT_2
EN
VOUT_SENSE
BYP
REF
VREG
REF_SENSE
EP
ADP7159ACPZ-04-R7
3.3V @ 2A Limited Output
C15 10uF
3V3APLL_EN
C18 22uF
C19 470nF
C20 1uF
R5 47k
R6 27k
C17 1uF
C16 10uF
ESR < 0.2Ω
3V3APLL
R3 750
D1 APHHS1005LZGCK-V
1mA @ 2.5V
IC4
C27 10uF
3V3PS_EN
C30 22uF
C31 470nF
C32 1uF
R8 47k
R11 27k
C29 1uF
C28 10uF
3V3PS
R8 750
D2 APHHS1005LZGCK-V
1mA @ 2.5V
Vout = 1.2(1+R1/R2)
IC5
C34 10uF
1V8_EN
C37 22uF
C38 470nF
C39 1uF
R18 10k
R20 20k
C36 1uF
C35 10uF
1V8
R13 750
D3 APHHS1005LZGCK-V
1mA @ 2.5V
Q2 CSD15380F3
R19 200k
1.8V @ 2A Limited Output
R14 10k
R17 2M4
VREFAC
OE_LS
R22 10k
R23 10k
D4 NSR01L30NXT5G
OE referenced to VCCA.
VADJ
R15 1M
100Ω R16
3V3PS_EN
tau = 22us
Q3 CSD15380F3
C40 22pF
3V3PS_DIS
Enabled if DIS is Floating (GPIO not configured) or Low.
R21 1M
R24 1M
100Ω R25
1V8_EN
tau = 22us
Q4 CSD15380F3
C41 22pF
1V8_DIS
Enabled if DIS is Floating (GPIO not configured) or Low.
R26 1M
TOP
FTG1
FTG2
BOTTOM
FTG3
FTG4
Project/Equipment Phase Stable Link
Document
Power Regulator
EP-ESE
CERN
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
Designer E.Orzes
Drawn by E.Orzes
Check by E.Orzes F.Martina S.Baron
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