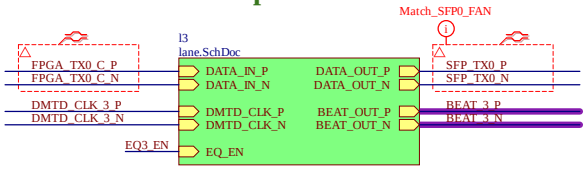
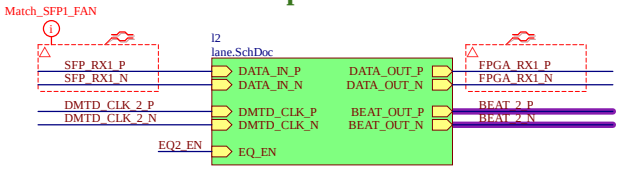
Dedicated to GT 0 (Channel 0) on Quad 0 and SFP 0

UpLink Tx



Dedicated to GT 1 (Channel 1) on Quad 0 and SFP 1

UpLink Rx



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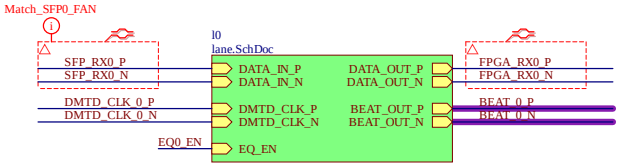

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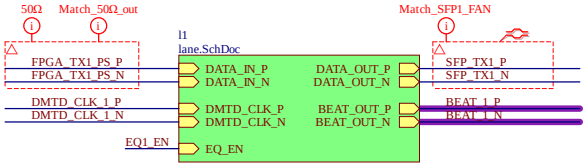

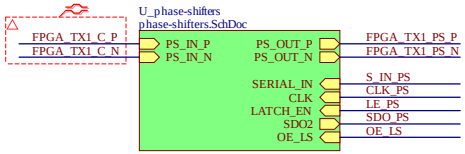

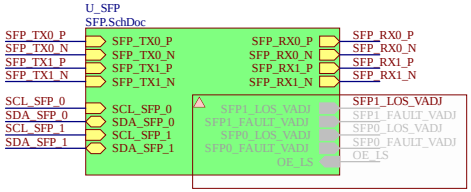

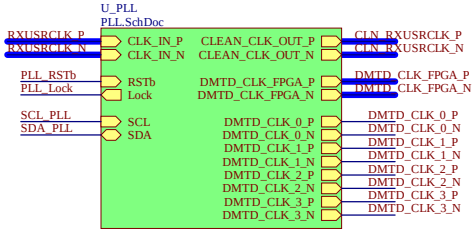

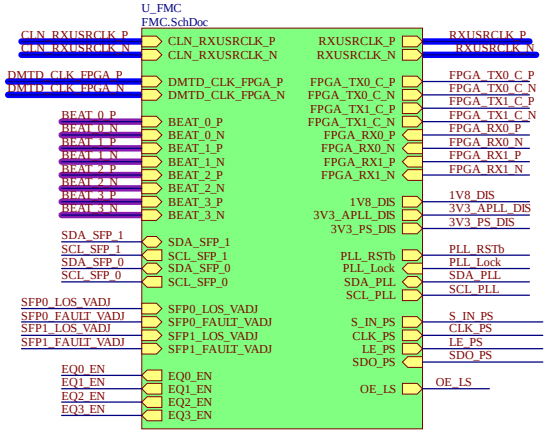

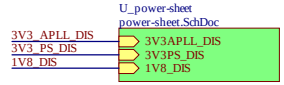

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2. Allow sheet entries to name nets (NO)
3. Append sheet number to local nets (NO)
4. Net identifier scope: Automatic (Hierarchical)
5. Automatic cross reference disabled

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	Check.by *	
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	File	top.SchDoc
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*		Size A3 / Rev *
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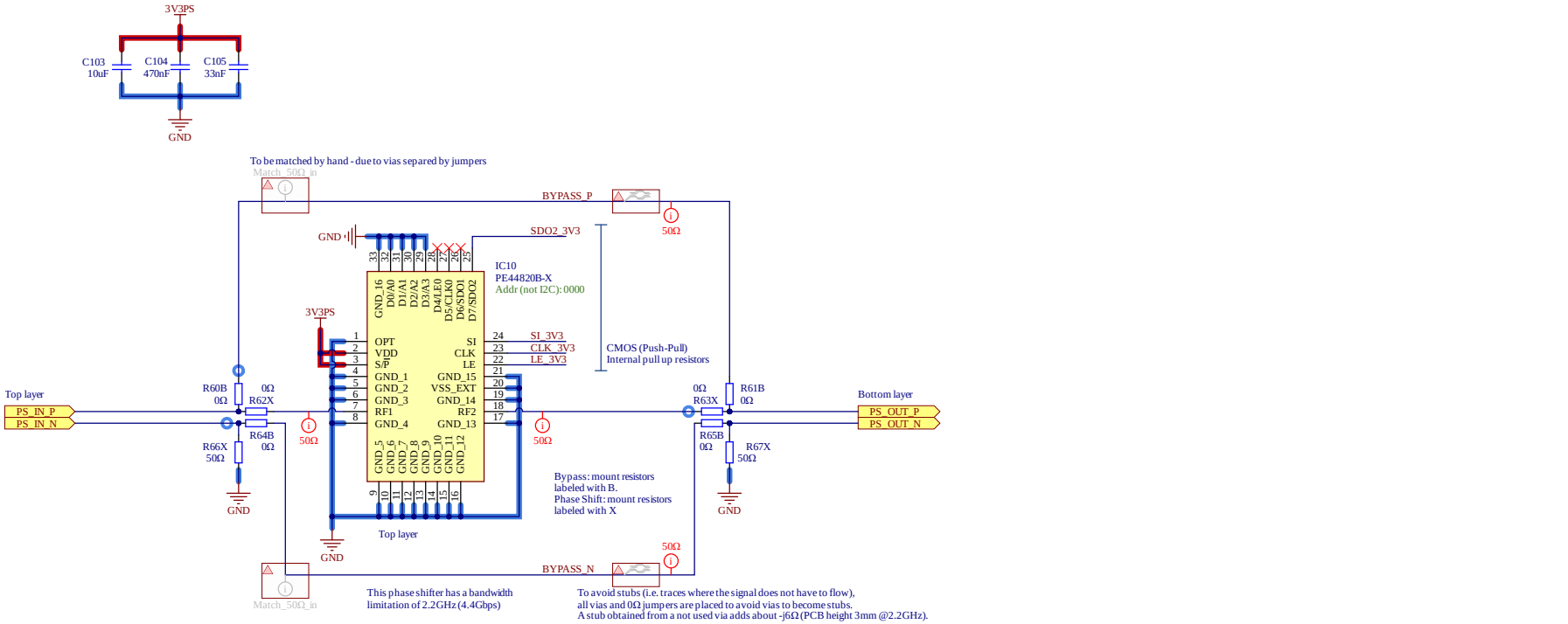

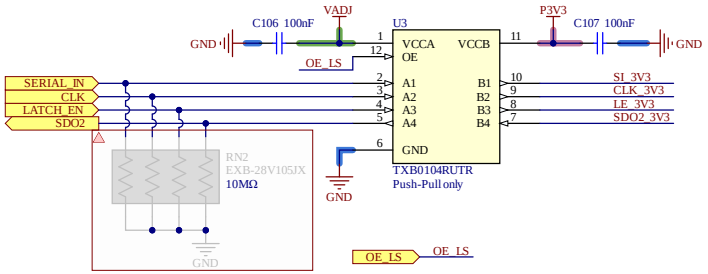

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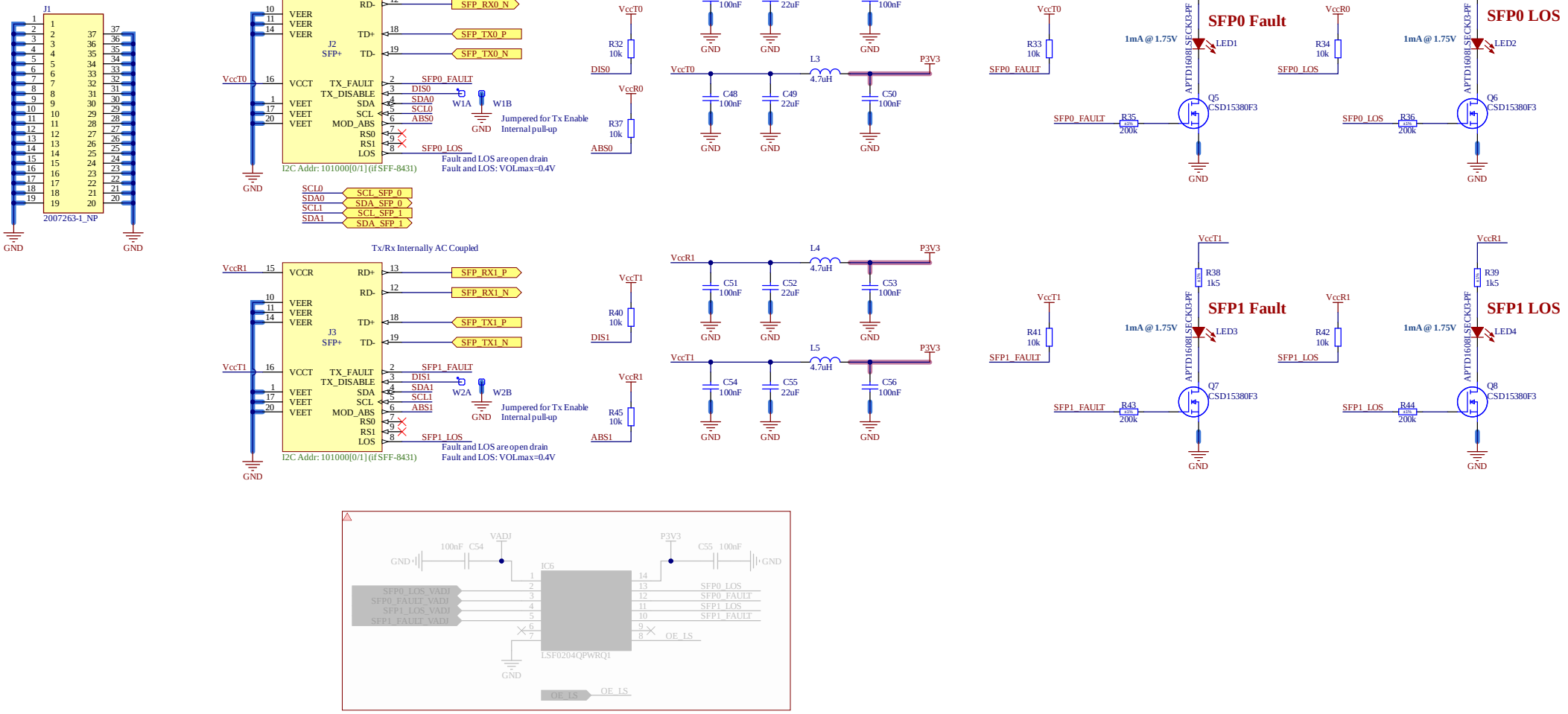
J1
2007263-1_NP
GND
Tx/Rx Internally AC Coupled
VccR0
VCCR
RD+
RD-
VEER
TD+
TD-
J2
SFP+
VccT0
VCCT
VEET
TX_FAULT
TX_DISABLE
SDA
SCL
MOD_ABS
RS0
RS1
LOS
SFP_RX0_P
SFP_RX0_N
SFP_TX0_P
SFP_TX0_N
SFP0_FAULT
DIS0
SDA0
SCL0
ABS0
SFP0_LOS
W1A
W1B
Jumpered for Tx Enable
Internal pull-up
Fault and LOS are open drain
Fault and LOS: VOLmax=0.4V
I2C Addr: 101000[0/1] (if SFF-8431)
SCL0
SDA0
SCL1
SDA1
SCL_SFP_0
SDA_SFP_0
SCL_SFP_1
SDA_SFP_1
R32 10k
R37 10k
Rs = 98mΩ < 1Ω
L2 4.7uH
L3 4.7uH
P3V3
C45 100nF
C46 22uF
C47 100nF
C48 100nF
C49 22uF
C50 100nF
SFP0 Fault
SFP0 LOS
R30 1k5
R31 1k5
R33 10k
R34 10k
1mA @ 1.75V
APTD1608LSECK3-PF
LED1
LED2
Q5 CSD15380F3
Q6 CSD15380F3
R35 200k
R36 200k
VccR1
VccT1
SFP_RX1_P
SFP_RX1_N
SFP_TX1_P
SFP_TX1_N
SFP1_FAULT
DIS1
SDA1
SCL1
ABS1
SFP1_LOS
W2A
W2B
R40 10k
R45 10k
L4 4.7uH
L5 4.7uH
C51 100nF
C52 22uF
C53 100nF
C54 100nF
C55 22uF
C56 100nF
SFP1 Fault
SFP1 LOS
R38 1k5
R39 1k5
R41 10k
R42 10k
LED3
LED4
Q7 CSD15380F3
Q8 CSD15380F3
R43 200k
R44 200k
IC6
VADJ
100nF C54
C55 100nF
SFP0_LOS_VADJ
SFP0_FAULT_VADJ
SFP1_LOS_VADJ
SFP1_FAULT_VADJ
SFP0_LOS
SFP0_FAULT
SFP1_LOS
SFP1_FAULT
OE_LS
LSF0204QPWRQ1
Temperature Sensor
RTD -50°C +130°C
32207590
W3A
W3B
W3C
W3D
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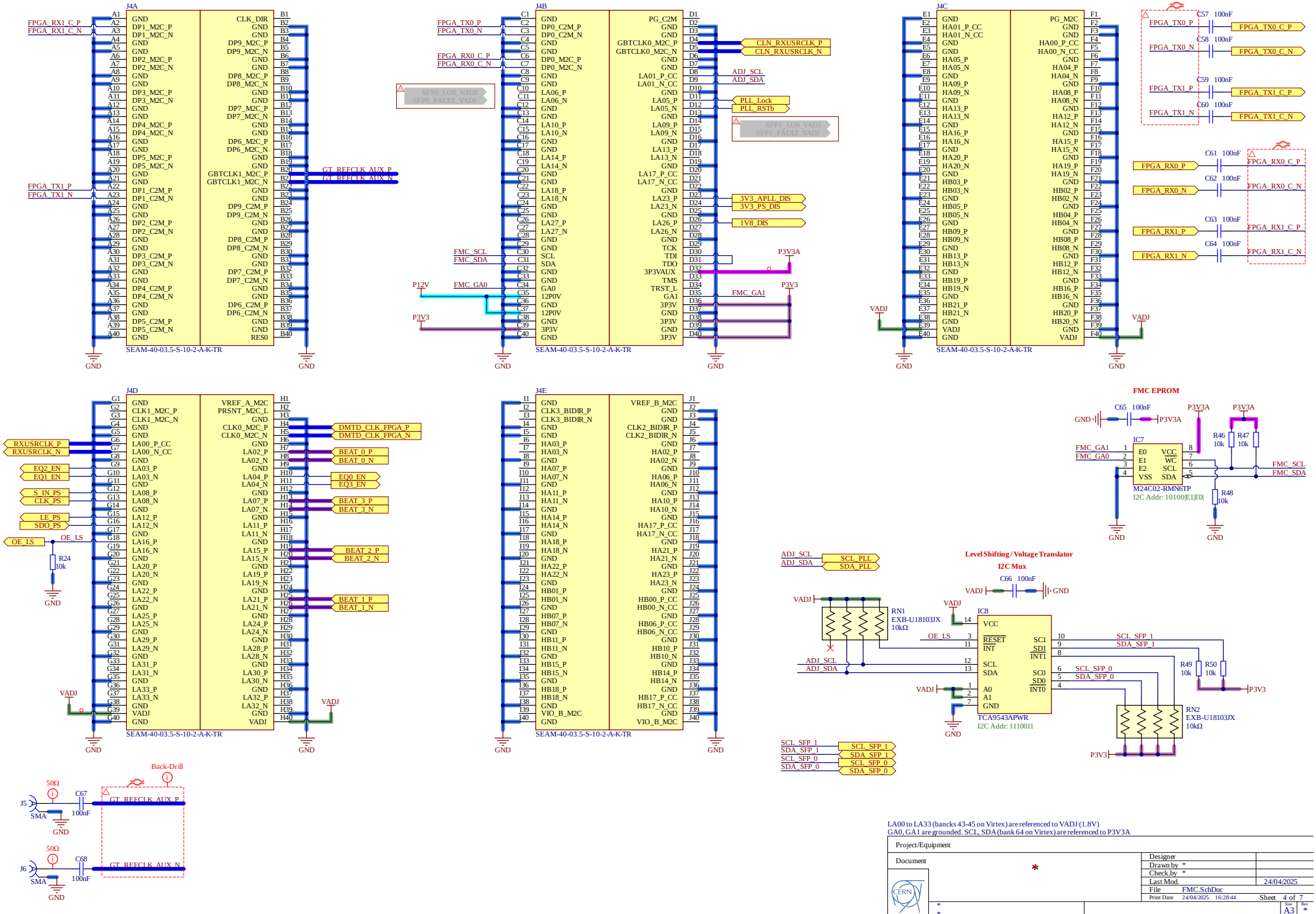
Rev *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FPGA_RX1_C_P
FPGA_RX1_C_N
FPGA_TX1_P
FPGA_TX1_N
GT_REFCLK_AUX_P
GT_REFCLK_AUX_N
SEAM-40-03.5-S-10-2-A-K-TR
J4B
FPGA_TX0_P
FPGA_TX0_N
FPGA_RX0_C_P
FPGA_RX0_C_N
SFP0_LOS_VADJ
SFP0_FAULT_VADJ
CLN_RXUSRCLK_P
CLN_RXUSRCLK_N
ADJ_SCL
ADJ_SDA
PLL_Lock
PLL_RSTb
SFP1_LOS_VADJ
SFP1_FAULT_VADJ
3V3_APLL_DIS
3V3_PS_DIS
1V8_DIS
FMC_SCL
FMC_SDA
FMC_GA0
FMC_GA1
P12V
P3V3A
P3V3
SEAM-40-03.5-S-10-2-A-K-TR
J4C
FPGA_TX0_P
FPGA_TX0_N
FPGA_TX1_P
FPGA_TX1_N
FPGA_RX0_P
FPGA_RX0_N
FPGA_RX1_P
FPGA_RX1_N
C57 100nF
C58 100nF
C59 100nF
C60 100nF
C61 100nF
C62 100nF
C63 100nF
C64 100nF
FPGA_TX0_C_P
FPGA_TX0_C_N
FPGA_TX1_C_P
FPGA_TX1_C_N
FPGA_RX0_C_P
FPGA_RX0_C_N
FPGA_RX1_C_P
FPGA_RX1_C_N
VADJ
SEAM-40-03.5-S-10-2-A-K-TR
J4D
RXUSRCLK_P
RXUSRCLK_N
EQ2_EN
EQ1_EN
S_IN_PS
CLK_PS
LE_PS
SDO_PS
OE_LS
R24
10k
DMTD_CLK_FPGA_P
DMTD_CLK_FPGA_N
BEAT_0_P
BEAT_0_N
EQ0_EN
EQ3_EN
BEAT_3_P
BEAT_3_N
BEAT_2_P
BEAT_2_N
BEAT_1_P
BEAT_1_N
VADJ
SEAM-40-03.5-S-10-2-A-K-TR
J4E
SEAM-40-03.5-S-10-2-A-K-TR
FMC EPROM
C65 100nF
IC7
M24C02-RMN6TP
I2C Addr: 10100|E1|E0|
R46 10k
R47 10k
R48 10k
FMC_SCL
FMC_SDA
Level Shifting / Voltage Translator
I2C Mux
C66 100nF
IC8
TCA9543APWR
I2C Addr: 1110011
RN1
EXB-U18103JX
10kΩ
RN2
EXB-U18103JX
10kΩ
R49 10k
R50 10k
SCL_PLL
SDA_PLL
SCL_SFP_1
SDA_SFP_1
SCL_SFP_0
SDA_SFP_0
Back-Drill
50Ω
J5
J6
SMA
C67 100nF
C68 100nF
GT_REFCLK_AUX_P
GT_REFCLK_AUX_N
GND
P3V3
P3V3A
LA00 to LA33 (bancks 43-45 on Virtex) are referenced to VADJ (1.8V)
GA0, GA1 are grounded. SCL, SDA (bank 64 on Virtex) are referenced to P3V3A
Project/Equipment
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Check.by *
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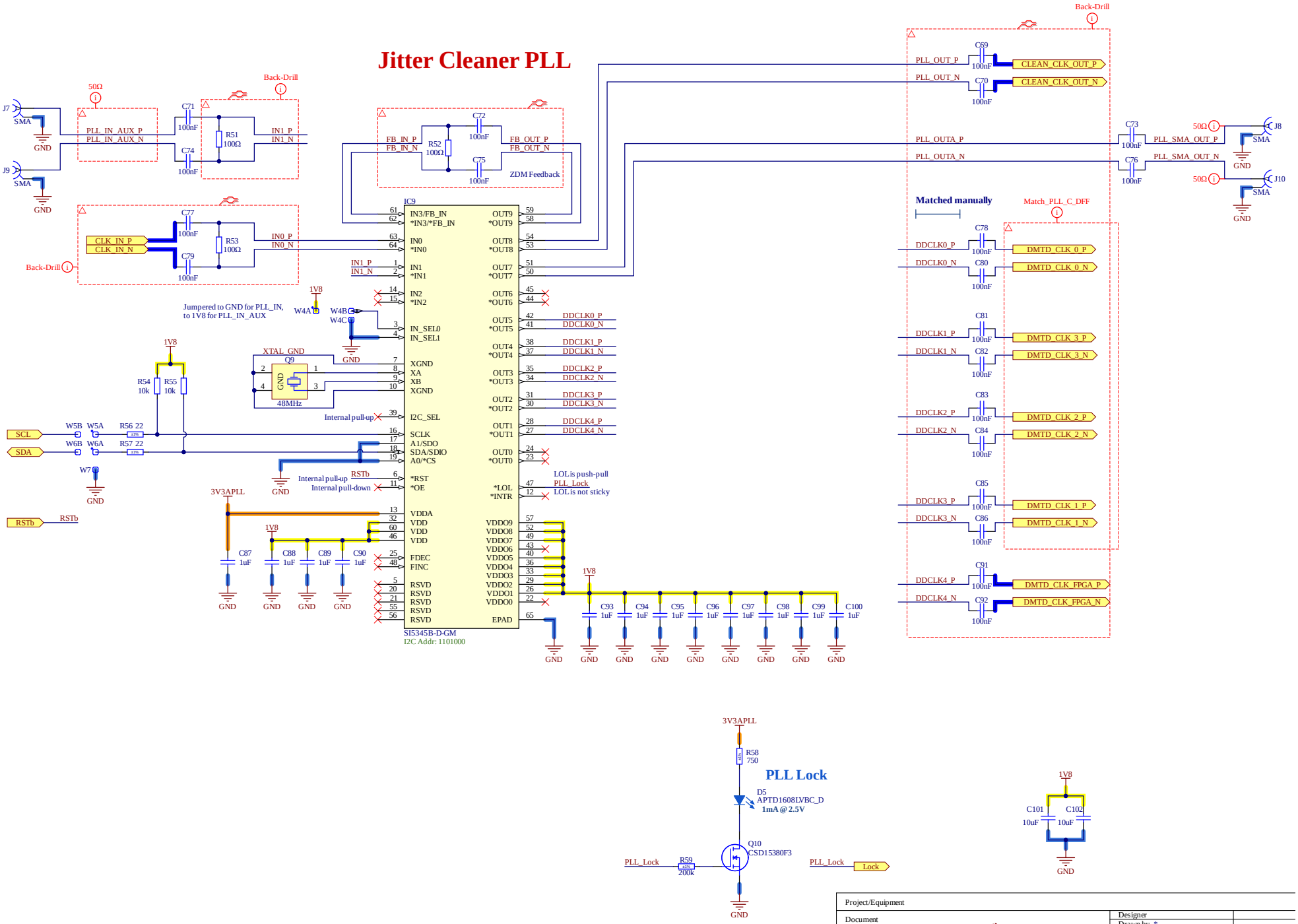
Rev *

Jitter Cleaner PLL



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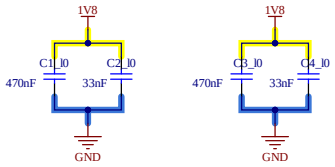
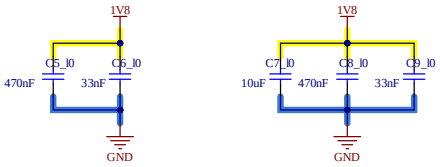
Rev	*

Bypass for Fanout power pins



Bypass for D-FF power pins



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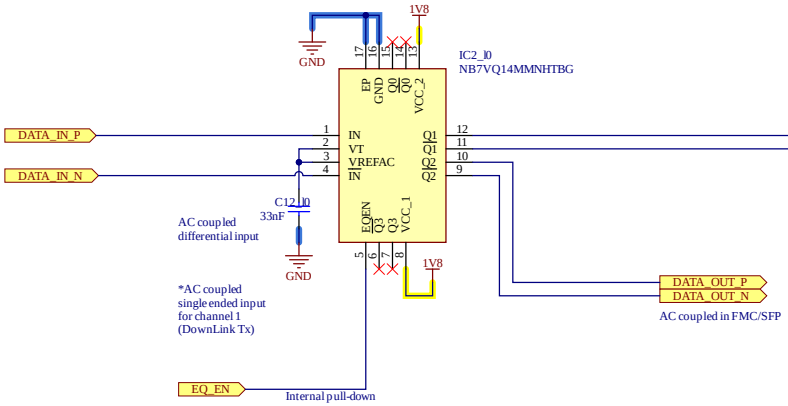

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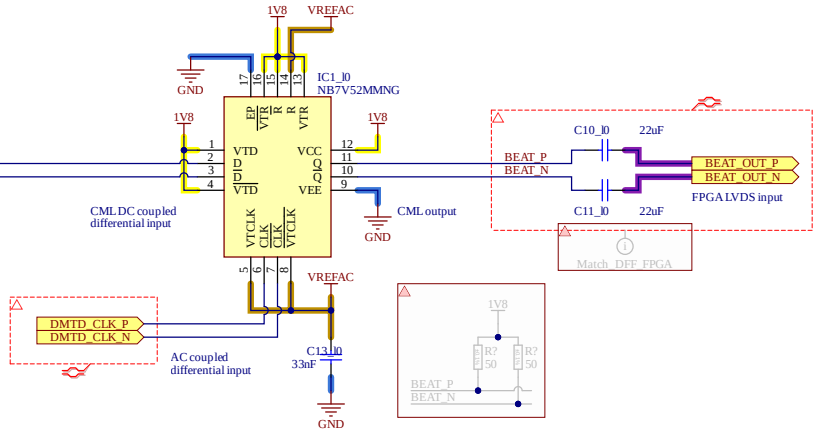

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		Drawn by	E.Orzes
		Check.by	E.Orzes F.Martina S.Baron
		Last Mod.	15/04/2025
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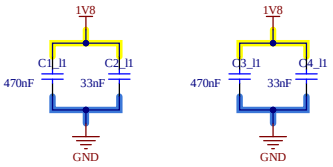
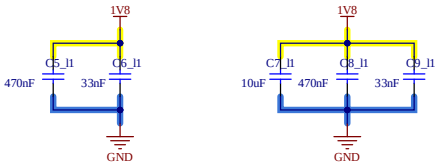
		Rev	1.0

Bypass for Fanout power pins



Bypass for D-FF power pins



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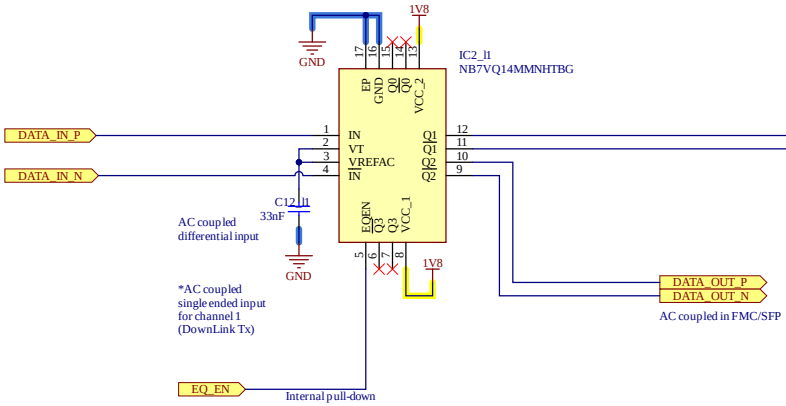

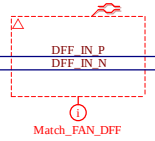

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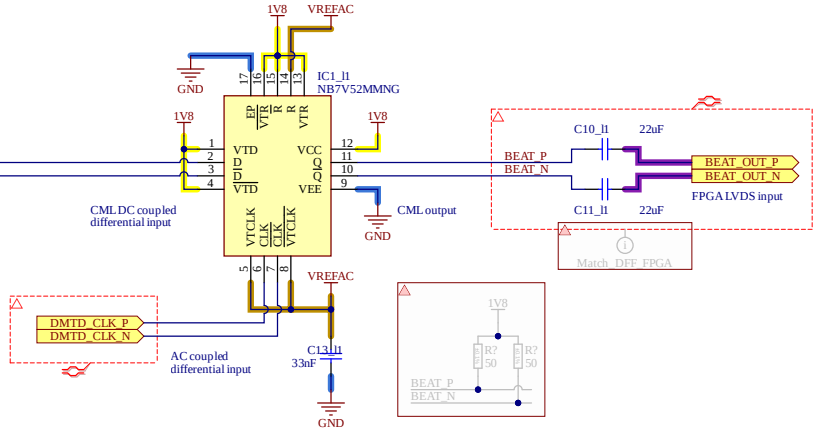

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		Check.by	E.Orzes F.Martina S.Baron
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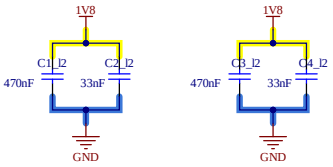
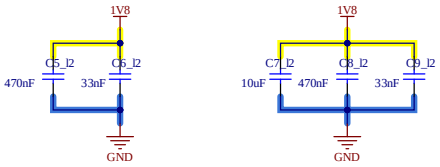
Bypass for Fanout power pins



Bypass for D-FF power pins



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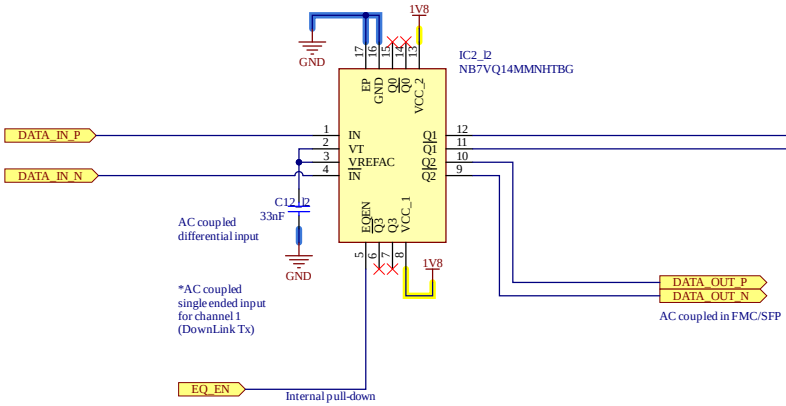

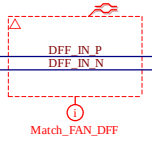

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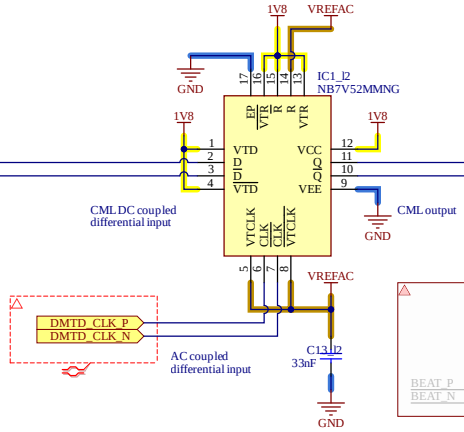

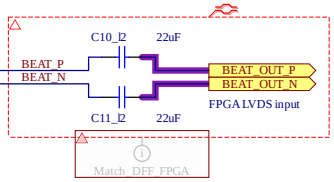

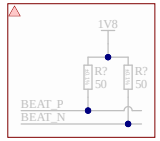

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		Rev	1.0

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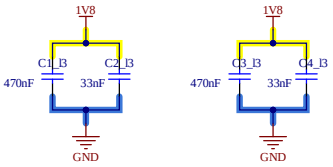
Bypass for Fanout power pins



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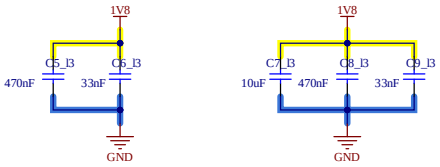

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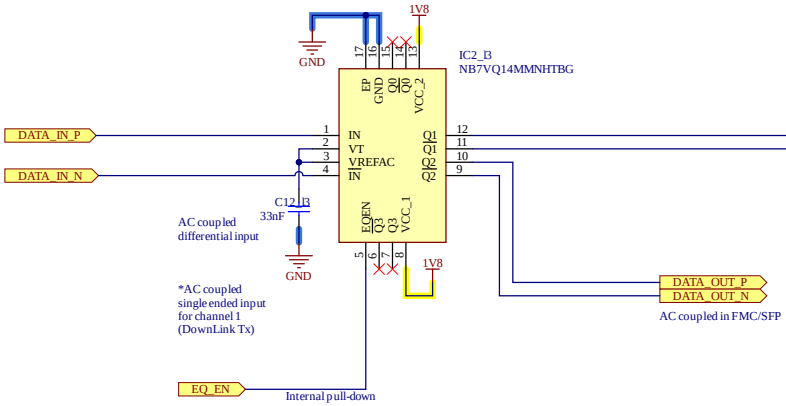
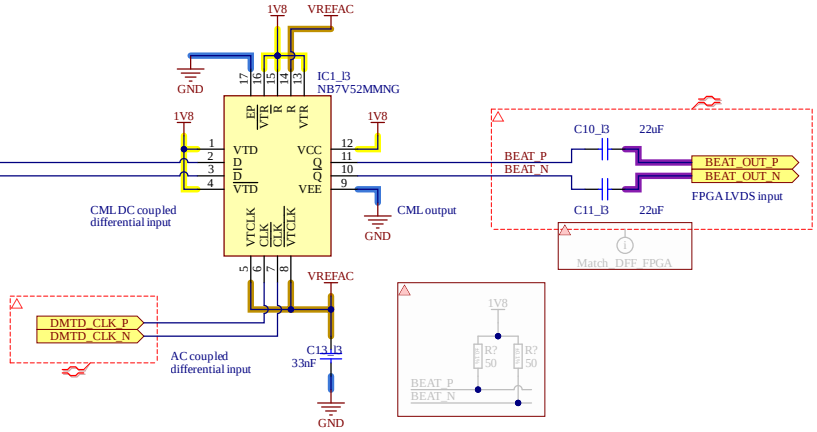
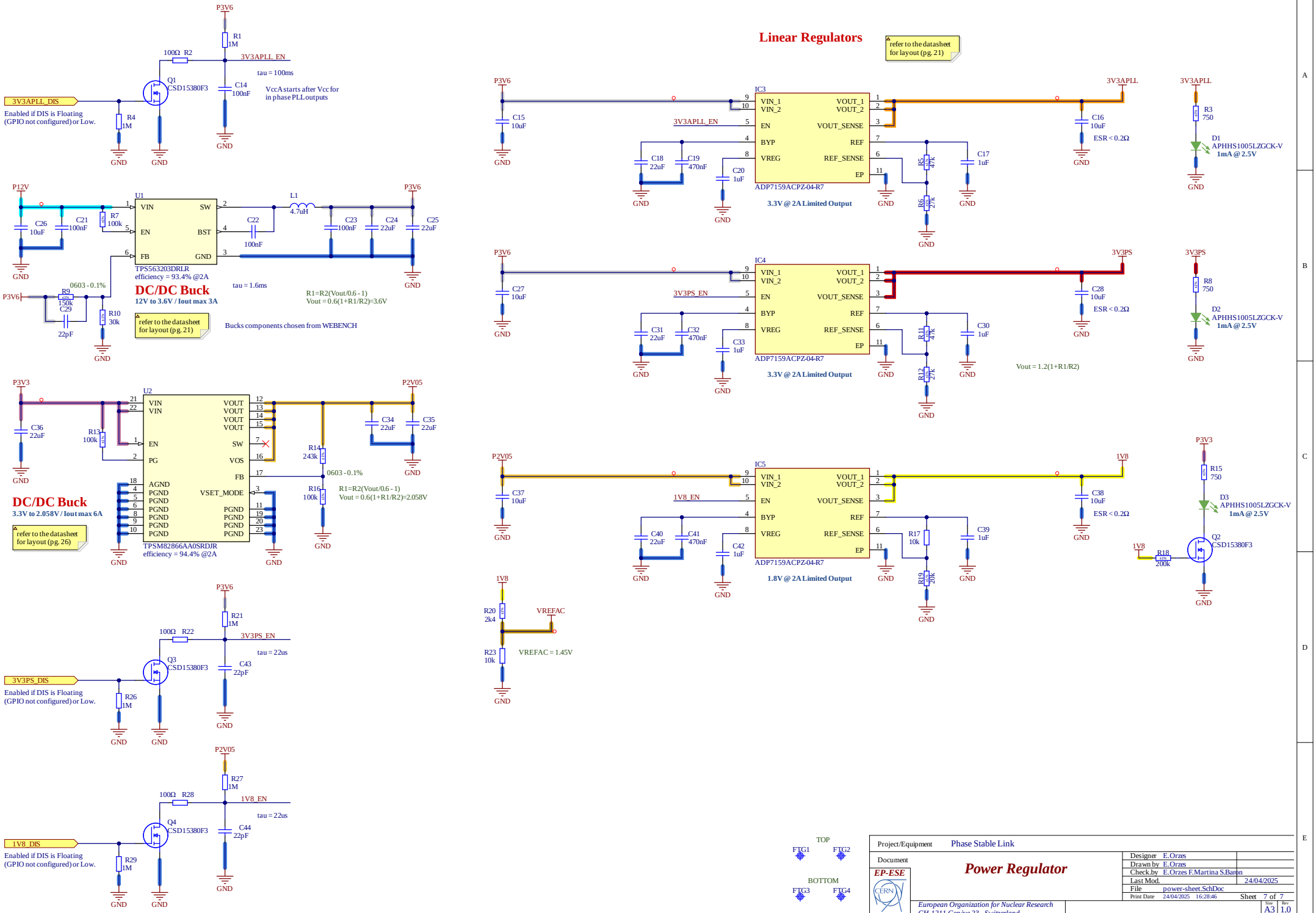


D-FF



Project/Equipment	Phase Stable Link		
Document	*CDR, Fanout, D-FF*	Designer	E.Orzes
		Drawn by	E.Orzes
		Check.by	E.Orzes F.Martina S.Baron
		Last Mod.	15/04/2025
		File	lane.SchDoc
		Print Date	24/04/2025 16:28:46
		Sheet	6 of 7
European Organization for Nuclear Research *CH-1211 Genève 23 - Switzerland*		Size	A3
		Rev	1.0


Linear Regulators
refer to the datasheet for layout (pg. 21)
P3V6
R1 1M
100Ω R2
3V3APLL_EN
tau = 100ms
Q1 CSD15380F3
C14 100nF
VccA starts after Vcc for in phase PLL outputs
3V3APLL_DIS
Enabled if DIS is Floating (GPIO not configured) or Low.
R4 1M
GND
P12V
U1
VIN
SW
EN
BST
FB
GND
L1 4.7uH
C26 10uF
C21 100nF
R7 100k
C22 100nF
C23 100nF
C24 22uF
C25 22uF
TPS563203DRLR
efficiency = 93.4% @2A
DC/DC Buck
12V to 3.6V / Iout max 3A
tau = 1.6ms
R1=R2(Vout/0.6 - 1)
Vout = 0.6(1+R1/R2)=3.6V
R9 150k
0603 - 0.1%
C29 22pF
R10 30k
refer to the datasheet for layout (pg. 21)
Bucks components chosen from WEBENCH
P3V3
U2
VIN
EN
PG
AGND
PGND
VOUT
SW
VOS
FB
VSET_MODE
C36 22uF
R13 100k
R14 243k
R16 100k
C34 22uF
C35 22uF
P2V05
TPSM82866AA0SRDJR
efficiency = 94.4% @2A
DC/DC Buck
3.3V to 2.058V / Iout max 6A
R1=R2(Vout/0.6 - 1)
Vout = 0.6(1+R1/R2)=2.058V
refer to the datasheet for layout (pg. 26)
3V3PS_DIS
Enabled if DIS is Floating (GPIO not configured) or Low.
R21 1M
100Ω R22
3V3PS_EN
tau = 22us
Q3 CSD15380F3
C43 22pF
R26 1M
1V8_DIS
Enabled if DIS is Floating (GPIO not configured) or Low.
R27 1M
100Ω R28
1V8_EN
tau = 22us
Q4 CSD15380F3
C44 22pF
R29 1M
IC3
IC4
IC5
VIN_1
VIN_2
VOUT_1
VOUT_2
EN
VOUT_SENSE
BYP
REF
VREG
REF_SENSE
EP
ADP7159ACPZ-04-R7
3.3V @ 2A Limited Output
1.8V @ 2A Limited Output
C15 10uF
C16 10uF
ESR < 0.2Ω
C17 1uF
C18 22uF
C19 470nF
C20 1uF
R5 47k
R6 27k
3V3APLL_EN
C27 10uF
C28 10uF
C30 1uF
C31 22uF
C32 470nF
C33 1uF
R11 47k
R12 27k
3V3PS_EN
Vout = 1.2(1+R1/R2)
C37 10uF
C38 10uF
C39 1uF
C40 22uF
C41 470nF
C42 1uF
R17 10k
R19 20k
1V8_EN
1V8
R20 2k4
R23 10k
VREFAC
VREFAC = 1.45V
3V3APLL
3V3PS
R3 750
R8 750
R15 750
D1 APHHS1005LZGCK-V
1mA @ 2.5V
D2 APHHS1005LZGCK-V
1mA @ 2.5V
D3 APHHS1005LZGCK-V
1mA @ 2.5V
Q2 CSD15380F3
R18 200k
TOP
FTG1
FTG2
BOTTOM
FTG3
FTG4
Project/Equipment Phase Stable Link
Document
Power Regulator
EP-ESE
CERN
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
Designer E.Orzes
Drawn by E.Orzes
Check.by E.Orzes F.Martina S.Baron
Last Mod. 24/04/2025
File power-sheet.SchDoc
Print Date 24/04/2025 16:28:46
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Size A3
Rev 1.0