KiCad schematic — zynq_sdr_dongle

+3.3V

Conn_01x13_Male
J10

Pin	Signal
1	
2	
3	PS-SRST#
4	UART_TX
5	UART_RX
6	PS_MIO11_SDA
7	PS_MIO10_SCL
8	PS_MIO19_SPI_MOSI
9	PS_MIO16_SPI_CLK
10	PS_MIO17_SPI_MISO
11	PS_MIO18_SPI_SS
12	PS_MIO20_SPI_SS1
13	PS_MIO21_SPI_SS2

GND

ZYNQ PS Part

PS-SRST#
UART_TX
UART_RX
PS_MIO11_SDA
PS_MIO10_SCL
PS_MIO19_SPI_MOSI
PS_MIO16_SPI_CLK
PS_MIO17_SPI_MISO
PS_MIO18_SPI_SS
PS_MIO20_SPI_SS1
PS_MIO21_SPI_SS2

TRANS_SPI_CLK
TRANS_SPI_MOSI
TRANS_SPI_MISO
TRANS_SPI_SS
TRANS_RST

Transceiver Powr

File: Transceiver_Power.kicad_sch

USB Connector

PS_MIO27_500_USB_RESETB
PS_MIO29_501_USB0_DIR
PS_MIO31_501_USB0_NXT
PS_MIO36_501_USB0_CLK
PS_MIO30_501_USB0_STP
PS_MIO_501_USB0_D[0..7]
PWR_STA

PS_MIO27_500_USB_RESETB
PS_MIO29_501_USB0_DIR
PS_MIO31_501_USB0_NXT
PS_MIO36_501_USB0_CLK
PS_MIO30_501_USB0_STP
PS_MIO_501_USB0_D[0..7]
LDO_EN
DCDC_PG_1V35

LDO_EN

File: ZYNQ_PS.kicad_sch

File: USB_Connector.kicad_sch

Transceiver RF

TRANS_RST
LDO_EN
TRANS_SPI_CLK
TRANS_SPI_MOSI
TRANS_SPI_MISO
TRANS_SPI_SS

+5V

D1 R43
FPGA_LED_DONE
240Ω
R44
D2 500Ω
R45
D3 500Ω

GND

亏路灯 (handwritten)

Power Manage

DCDC_PG_1V35
LDO_EN

File: Power_Manage.kicad_sch

ZYNQ PL Part

TRANS_SYNC
TRANS_ENAGC
TRANS_TXNRX
TRANS_ENABLE
TRANS_CMOS_TX_FRAME
TRANS_CMOS_TX_D[0..11]
TRANS_CMOS_FB_CLK
TRANS_CMOS_RX_D[0..11]
TRANS_MRCC_DATA_CLK
TRANS_CMOS_RX_FRAME
TRANS_CTRL_OUT[0..7]
TRANS_CTRL_IN[0..3]
TRANS_MRCC_CLKOUT
FPGA_LED_DONE

pluto SPI connect to PL? (handwritten)

TRANS_SYNC
TRANS_ENAGC
TRANS_TXNRX
TRANS_ENABLE
TRANS_CMOS_TX_FRAME
TRANS_CMOS_TX_D[0..11]
TRANS_CMOS_FB_CLK
TRANS_CMOS_RX_D[0..11]
TRANS_MRCC_DATA_CLK
TRANS_CMOS_RX_FRAME
TRANS_CTRL_OUT[0..7]
TRANS_CTRL_IN[0..3]
TRANS_MRCC_CLKOUT

ARD_ANALOG[0..7]

Pin	Signal
	ARD_ANALOG0
	ARD_ANALOG1
	ARD_ANALOG2
	ARD_ANALOG3
	ARD_ANALOG4
	ARD_ANALOG5
	ARD_ANALOG6
	ARD_ANALOG7

J11   Conn_01x16_Male

GND

Pin	Signal
1	ARD_ANALOG0
2	ARD_AREF
3	ARD_ANALOG1
4	ARD_ANALOG3
5	ARD_ANALOG4
6	ARD_ANALOG5
7	ARD_ANALOG6
8	ARD_ANALOG7
9	ARD_PWM7
10	ARD_PWM6
11	ARD_PWM5
12	ARD_PWM4
13	ARD_PWM3
14	ARD_PWM2

ARD_PWM[2..7]

ARD_PWM2
ARD_PWM3
ARD_PWM4
ARD_PWM5
ARD_PWM6
ARD_PWM7

R60 N/A TRANS_AUX_DAC2
R42 N/A TRANS_AUX_DAC1
R61 N/A TRANS_AUX_ADC

TRANS_AUX_DAC1
TRANS_AUX_DAC2
TRANS_AUX_ADC

TRANS_AUX_DAC1
TRANS_AUX_DAC2
TRANS_AUX_ADC
TRANS_GPO_[0..3]

File: Transceiver_RF.kicad_sch

Transceiver

FPGA_LED_DONE

ARD_ANALOG[0..7]
ARD_PWM[2..7]

cannot fanout
to ardruino IO

FPGA_AUXADC_N
FPGA_AUXADC_P
FPGA_SRCCN_YB
FPGA_VREF

FPGA_JTAG_TMS
FPGA_JTAG_TCK
FPGA_JTAG_TDO
FPGA_JTAG_TDI

ARD_AREF R63 N/A
R54 N/A FPGA_VREF

File: ZYNQ_PL.kicad_sch

ZYNQ

BTB Connector

FPGA_AUXADC_N FPGA_JTAG_TMS
FPGA_AUXADC_P FPGA_JTAG_TCK
FPGA_JTAG_TDO
FPGA_JTAG_TDI
FPGA_VREF
TRANS_GPO_[0..3]

File: BTB_Connector.kicad_sch

Sheet: /
File: zynq_sdr_dongle.kicad_sch

Title:

Size: A3   Date: Rev:
KiCad E.D.A. kicad (6.99.0-621-g810a49ef1b)   Id: 1/13

+5V

C43 4.7uF   C92 4.7uF

R25 10K

U10 TPS6208B
A2 VIN   SW B2
A1 EN   FB C1
B1 PG   GND C2

GND

DCDC_PG_1V0

L7 DFE18SANR47MG0

+1V0

R26 22K   C50 4.7uF   C51 4.7uF

R27 33K

GND

GND

DCDC_PG_1V35

DCDC_PG_1V35

LDO_END   LDO_EN

C89 4.7uF   C93 4.7uF

U9 TPS6208B
A2 VIN   SW B2
A1 EN   FB C1
B1 PG   GND C2

GND

DCDC_PG_1V8

DCDC_PG_1V35

Pullup by PS part

L6 DFE18SANR47MG0

VCC_DDR

R23 R   C48 4.7uF   C49 4.7uF   C128 4.7uF

R24 R

GND

GND

C90 4.7uF   C94 4.7uF

R19 10K

U8 TPS6208B
A2 VIN   SW B2
A1 EN   FB C1
B1 PG   GND C2

DCDC_PG_1V0

DCDC_PG_1V8

GND

L1 DFE18SANR47MG0

+1V8

R20 200K   C35 4.7uF   C37 4.7uF

R21 100K

GND

GND

C91 4.7uF   C95 4.7uF

R8 10K

U4 TPS6208B
A2 VIN   SW B2
A1 EN   FB C1
B1 PG   GND C2

DCDC_PG_1V8

GND

L8 DFE18SANR47MG0

+3.3V

R9 82K   C96 4.7uF   C97 4.7uF

R10 18K

GND

GND

+1V8   +1V8

C23 4.7uF   C30 4.7uF

GND

LDO_EN

U6
A1 IN   OUT C1
         BYP C5
A5 EN   FB B5
B1 GND
MAX38904C

GND

C120 0.1uF

R13 R

R14 R

GND

C39 4.7uF   C41 0.1uF   C121 10nF   C122 10nF   C123 4.7uF

GND

VCC_1V3_TRANS_0

+1V8   +1V8

C27 4.7uF   C32 4.7uF

GND

LDO_EN

U7
A1 IN   OUT C1
         BYP C5
A5 EN   FB B5
B1 GND
MAX38904C

GND

C124 0.1uF

R15 R

R16 R

GND

C40 4.7uF   C42 4.7uF   C125 0.1uF   C126 10nF   C127 10nF

GND

VCC_1V3_TRANS_1

R41 0R

+1V8   VCC_BANK34

+1V8
C131
0.1uF
+1V8
R49
R
GND1
X2
Tri-State OUT
LVCMOS
ECS-2520MV-xxx-xx
GND
+1V8
PS_CLK
+1V8
+1V8
C145
0.1uF
GND
R50
10K
R51
N/A
GND
R52
10K
GND
+1V8
GND
SW2
SW_DIP_x01
+1V8
R22
10K
GND
C38
0.1uF
GND

U2E   xc7z020clq400
E7 PS_CLK_500
E6 PS_MIO0_500
A7 PS_MIO1_500
B8 PS_MIO2_500
D6 PS_MIO3_500
B7 PS_MIO4_500
A6 PS_MIO5_500
A5 PS_MIO6_500
D8 PS_MIO7_500
D5 PS_MIO8_500
B5 PS_MIO9_500
E9 PS_MIO10_500
C6 PS_MIO11_500
D9 PS_MIO12_500
E8 PS_MIO13_500
C5 PS_MIO14_500
C8 PS_MIO15_500
C7 PS_POR_B_500
B6 VCCO_MIO0_500[2]

PS_MIO4_BOOT1
PS_MIO6_BOOT-MODE
PS_MIO010_SCL
PS_MIO011_SDA
UART_TX
UART_RX
DCDC_PG_1V35

MIO[2] set to GND
jtag in cascade mode

MIO[6] set to 0, Hardware waits for PLL to lock
user resistor pulldown, provide hard fix possibilities

MIO[7-8] set to 1.8V
bank0,1 IO voltage 1.8V -> set to high

LDO_EN
PS_MIO16_SPI_CLK
PS_MIO17_SPI_MISO
PS_MIO18_SPI_SS
PS_MIO19_SPI_MOSI
PS_MIO20_SPI_SS1
PS_MIO21_SPI_SS2

TRANS_SPI_MOSI
TRANS_SPI_MISO
TRANS_SPI_CLK
TRANS_SPI_SS
TRANS_RST
PS_MIO29_501_USB0_DIR
PS_MIO30_501_USB0_STP
PS_MIO31_501_USB0_NXT

PS_MIO_501_USB0_D[0..7]

PS_MIO_501_USB0_D0
PS_MIO_501_USB0_D1
PS_MIO_501_USB0_D2
PS_MIO_501_USB0_D3
PS_MIO_501_USB0_D4
PS_MIO_501_USB0_D5
PS_MIO_501_USB0_D6
PS_MIO_501_USB0_D7

PS_MIO36_501_USB0_CLK
PS_MIO27_500_USB_RESETB

PS_MIO010_SCL
PS_MIO011_SDA
UART_TX
UART_RX

DCDC_PG_1V35
PS-SRST#

+3.3V

J3   Micro_SD_Card
1 DAT2
2 DAT3/CD
3 CMD
4 VDD
5 CLK
6 VSS
7 DAT0
8 DAT1
9 SHIELD

GND   GND

PS_MIO44_501_SD_D2
PS_MIO45_501_SD_D3
PS_MIO41_501_SD_CMD
PS_MIO40_501_SD_CLK
PS_MIO42_501_SD_D0
PS_MIO43_501_SD_D1

U2F   xc7z020clq400
A19 PS_MIO16_501
E14 PS_MIO17_501
B18 PS_MIO18_501
D10 PS_MIO19_501
A17 PS_MIO20_501
F14 PS_MIO21_501
B17 PS_MIO22_501
D11 PS_MIO23_501
A16 PS_MIO24_501
F15 PS_MIO25_501
A15 PS_MIO26_501
D13 PS_MIO27_501
C16 PS_MIO28_501
C13 PS_MIO29_501
C15 PS_MIO30_501
E16 PS_MIO31_501
A14 PS_MIO32_501
D15 PS_MIO33_501
A12 PS_MIO34_501
F12 PS_MIO35_501
A11 PS_MIO36_501
A10 PS_MIO37_501
E13 PS_MIO38_501
C18 PS_MIO39_501
D14 PS_MIO40_501
C17 PS_MIO41_501
E12 PS_MIO42_501
A9   PS_MIO43_501
F13 PS_MIO44_501
B15 PS_MIO45_501
D16 PS_MIO46_501
B14 PS_MIO47_501
B12 PS_MIO48_501
C12 PS_MIO49_501
B13 PS_MIO50_501
B9   PS_MIO51_501
C10 PS_MIO52_501
C11 PS_MIO53_501
E11 PS_MIO_VREF_501
B10 PS_SRST_B_501
A13 VCCO_MIO1_501[4]

PS_MIO16_SPI_CLK
PS_MIO17_SPI_MISO
PS_MIO18_SPI_SS
PS_MIO19_SPI_MOSI
PS_MIO20_SPI_SS1
PS_MIO21_SPI_SS2
TRANS_SPI_MOSI
TRANS_SPI_MISO
TRANS_SPI_CLK
TRANS_SPI_SS
PS_MIO27_500_USB_RESETB
PS_MIO_501_USB0_D4
PS_MIO29_501_USB0_DIR
PS_MIO30_501_USB0_STP
PS_MIO31_501_USB0_NXT
PS_MIO_501_USB0_D0
PS_MIO_501_USB0_D1
PS_MIO_501_USB0_D2
PS_MIO_501_USB0_D3
PS_MIO36_501_USB0_CLK
PS_MIO_501_USB0_D5
PS_MIO_501_USB0_D6
PS_MIO_501_USB0_D7
PS_MIO40_501_SD_CLK
PS_MIO41_501_SD_CMD
PS_MIO42_501_SD_D0
PS_MIO43_501_SD_D1
PS_MIO44_501_SD_D2
PS_MIO45_501_SD_D3

TRANS_RST
+1V8
LDO_EN
R62
10K
PS-SRST#
+1V8
+1V8
C142
0.1uF
GND

DDR_CK− R1 80Ω DDR_CK+
GND R2 4.7K DDR_nRST

VCC_DDR

VREF_DDR1   VREF_DDR2
VREF_DDR3

C2   C4   C7   C10   C13   C15   C19   C22   C33   C34   C36   C25   L20
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF   0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

GND   GND   GND

VCC_DDR

C3   C5   C8   C11   C14   C16   C18   C21   C24   C26   C29   C31
0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF 0.1uF

GND

VCC_DDR   VREF_DDR3
          VREF_DDR2

DDR_A0	N3	A0	DDR3	DQ0	E3	DDR_DQ0
DDR_A1	P7	A1		DQ1	F7	DDR_DQ1
DDR_A2	P3	A2		DQ2	F2	DDR_DQ2
DDR_A3	N2	A3		DQ3	F8	DDR_DQ3
DDR_A4	P8	A4		DQ4	H3	DDR_DQ4
DDR_A5	P2	A5		DQ5	H8	DDR_DQ5
DDR_A6	R8	A6		DQ6	G2	DDR_DQ6
DDR_A7	R2	A7		DQ7	H7	DDR_DQ7
DDR_A8	T8	A8		DQ8	D7	DDR_DQ8
DDR_A9	R3	A9		DQ9	C3	DDR_DQ9
DDR_A10	L7	A10/AP		DQ10	C8	DDR_DQ10
DDR_A11	R7	A11		DQ11	C2	DDR_DQ11
DDR_A12	N7	A12/BC		DQ12	A7	DDR_DQ12
DDR_A13	T3	A13		DQ13	A2	DDR_DQ13
DDR_A14	T7	A14		DQ14	B8	DDR_DQ14
				DQ15	A3	DDR_DQ15
DDR_BA0	M2	BA0				
DDR_BA1	N8	BA1		LDM	E7	DDR_DQM0
DDR_BA2	M3	BA2		UDM	D3	DDR_DQM1
DDR_CK+	J7	CK		LDQS	F3	DDR_DQS0+
DDR_CK−	K7	CK		LDQS	G3	DDR_DQS0−
DDR_CKE	K9	CKE		UDQS	C7	DDR_DQS1+
				UDQS	B7	DDR_DQS1−
DDR_nRST	T2	RESET				
DDR_nCS	L2	CS		ZQ	L8	
DDR_nRAS	J3	RAS	DDR3			R3
DDR_nCAS	K3	CAS	U1			240Ω
DDR_nWE	L3	WE				GND
DDR_ODT	K1	ODT				

VDD B2
VDDQ A1
VREFDQ H1
VREFCA M8

VSS A9
VSSQ B1

GND

U2G
xc7z020clg400

DDR_A0	N2	PS_DDR_A0_502
DDR_A1	K2	PS_DDR_A1_502
DDR_A2	M3	PS_DDR_A2_502
DDR_A3	K3	PS_DDR_A3_502
DDR_A4	M4	PS_DDR_A4_502
DDR_A5	L1	PS_DDR_A5_502
DDR_A6	L4	PS_DDR_A6_502
DDR_A7	K4	PS_DDR_A7_502
DDR_A8	K1	PS_DDR_A8_502
DDR_A9	J4	PS_DDR_A9_502
DDR_A10	F5	PS_DDR_A10_502
DDR_A11	G4	PS_DDR_A11_502
DDR_A12	E4	PS_DDR_A12_502
DDR_A13	D4	PS_DDR_A13_502
DDR_A14	F4	PS_DDR_A14_502
DDR_BA0	L5	PS_DDR_BA0_502
DDR_BA1	R4	PS_DDR_BA1_502
DDR_BA2	J5	PS_DDR_BA2_502
DDR_nCAS	P5	PS_DDR_CAS_B_502
DDR_CKE	N3	PS_DDR_CKE_502
DDR_CK−	M2	PS_DDR_CKN_502
DDR_CK+	L2	PS_DDR_CKP_502
DDR_nCS	N1	PS_DDR_CS_B_502
DDR_DQM1	A1	PS_DDR_DM0_502
DDR_DQM0	F1	PS_DDR_DM1_502
	T1	PS_DDR_DM2_502
	Y1	PS_DDR_DM3_502
DDR_DQ8	C3	PS_DDR_DQ0_502
DDR_DQ9	B3	PS_DDR_DQ1_502
DDR_DQ15	A2	PS_DDR_DQ2_502
DDR_DQ13	A4	PS_DDR_DQ3_502
DDR_DQ14	D3	PS_DDR_DQ4_502
DDR_DQ12	D1	PS_DDR_DQ5_502
DDR_DQ11	C1	PS_DDR_DQ6_502
DDR_DQ10	E1	PS_DDR_DQ7_502
DDR_DQ0	E2	PS_DDR_DQ8_502
DDR_DQ1	F1	PS_DDR_DQ9_502
DDR_DQ3	G3	PS_DDR_DQ10_502
DDR_DQ7	H3	PS_DDR_DQ11_502
DDR_DQ5	J3	PS_DDR_DQ12_502
DDR_DQ2	H2	PS_DDR_DQ13_502
DDR_DQ6	H1	PS_DDR_DQ14_502
DDR_DQ4	J1	PS_DDR_DQ15_502
	P1	PS_DDR_DQ16_502
	P3	PS_DDR_DQ17_502
	R3	PS_DDR_DQ18_502
	R1	PS_DDR_DQ19_502
	T4	PS_DDR_DQ20_502
	U4	PS_DDR_DQ21_502
	U2	PS_DDR_DQ22_502
	U3	PS_DDR_DQ23_502
	V1	PS_DDR_DQ24_502
	Y3	PS_DDR_DQ25_502
	W1	PS_DDR_DQ26_502
	Y4	PS_DDR_DQ27_502
	Y2	PS_DDR_DQ28_502
	W3	PS_DDR_DQ29_502
	V2	PS_DDR_DQ30_502
	V3	PS_DDR_DQ31_502
DDR_DQS1−	B2	PS_DDR_DQS_N0_502
DDR_DQS0−	F2	PS_DDR_DQS_N1_502
	T2	PS_DDR_DQS_N2_502
	W4	PS_DDR_DQS_N3_502
DDR_DQS1+	C2	PS_DDR_DQS_P0_502
DDR_DQS0+	G2	PS_DDR_DQS_P1_502
	R2	PS_DDR_DQS_P2_502
	W5	PS_DDR_DQS_P3_502
DDR_nRST	B4	PS_DDR_DRST_B_502
DDR_ODT	N5	PS_DDR_ODT_502
DDR_nRAS	P4	PS_DDR_RAS_B_502
	H6	PS_DDR_VREF0_502
VREF_DDR1	P6	PS_DDR_VREF1_502
VCC_DDR	G5	PS_DDR_VRN_502
	H5	PS_DDR_VRP_502
DDR_nWE	M5	PS_DDR_WE_B_502
VCC_DDR	A3	VCCO_DDR_502[10]

R4 80Ω DDR_VRN
R5 80Ω DDR_VRP
GND

VCC_DDR   VCC_DDR   VCC_DDR

R31 1K   R33 1K   R35 1K
VREF_DDR1 VREF_DDR2 VREF_DDR3
R32 1K   R34 1K   R36 1K

GND   GND   GND

Sheet: /ZYNQ PS Part/PS DDR/
File: PS_DDR.kicad_sch
Title:
Size: A3   Date: Rev:
KiCad E.D.A. kicad (6.99.0−621−g810a49ef1b)   Id: 4/13

U2D   xc7z020clg400

Left side signal labels:

TRANS_CTRL_IN[0..3] TRANS_CTRL_IN[0..3]
- TRANS_CTRL_IN0
- TRANS_CTRL_IN1
- TRANS_CTRL_IN2
- TRANS_CTRL_IN3

TRANS_CTRL_OUT[0..7] TRANS_CTRL_OUT[0..7]
- TRANS_CTRL_OUT0
- TRANS_CTRL_OUT1
- TRANS_CTRL_OUT2
- TRANS_CTRL_OUT3
- TRANS_CTRL_OUT4
- TRANS_CTRL_OUT5
- TRANS_CTRL_OUT6
- TRANS_CTRL_OUT7

TRANS_CMOS_RX_D[0..11] TRANS_CMOS_RX_D[0..11]
- TRANS_CMOS_RX_D0
- TRANS_CMOS_RX_D1
- TRANS_CMOS_RX_D2
- TRANS_CMOS_RX_D3
- TRANS_CMOS_RX_D4
- TRANS_CMOS_RX_D5
- TRANS_CMOS_RX_D6
- TRANS_CMOS_RX_D7
- TRANS_CMOS_RX_D8
- TRANS_CMOS_RX_D9
- TRANS_CMOS_RX_D10
- TRANS_CMOS_RX_D11

TRANS_CMOS_RX_FRAME
TRANS_MRCC_DATA_CLK

TRANS_CMOS_TX_D[0..11] TRANS_CMOS_TX_D[0..11]
- TRANS_CMOS_TX_D0
- TRANS_CMOS_TX_D1
- TRANS_CMOS_TX_D2
- TRANS_CMOS_TX_D3
- TRANS_CMOS_TX_D4
- TRANS_CMOS_TX_D5
- TRANS_CMOS_TX_D6
- TRANS_CMOS_TX_D7
- TRANS_CMOS_TX_D8
- TRANS_CMOS_TX_D9
- TRANS_CMOS_TX_D10
- TRANS_CMOS_TX_D11

TRANS_CMOS_TX_FRAME
TRANS_CMOS_FB_CLK
TRANS_MRCC_CLKOUT
TRANS_SYNC
TRANS_ENAGC
TRANS_ENABLE
TRANS_TXNRX

Pin table (signal — pin — IO name):

Signal	Pin	IO name
TRANS_CTRL_IN2	G14	IO_0_35
TRANS_CTRL_OUT0	J15	IO_25_35
TRANS_CTRL_OUT3	B20	IO_L1N_T0_AD0N_35
TRANS_CTRL_OUT1	C20	IO_L1P_T0_AD0P_35
	A20	IO_L2N_T0_AD8N_35
TRANS_ENABLE	B19	IO_L2P_T0_AD8P_35
TRANS_CMOS_RX_D0	D18	IO_L3N_T0_DQS_AD1N_35
TRANS_TXNRX	E17	IO_L3P_T0_DQS_AD1P_35
TRANS_CTRL_OUT7	D20	IO_L4N_T0_35
TRANS_CMOS_RX_D10	D19	IO_L4P_T0_35
TRANS_CMOS_RX_D8	E19	IO_L5N_T0_AD9N_35
TRANS_CMOS_RX_D3	E18	IO_L5P_T0_AD9P_35
TRANS_CMOS_RX_D1	F17	IO_L6N_T0_VREF_35
FPGA_M20	F16	IO_L6P_T0_35
TRANS_CMOS_TX_D2	M20	IO_L7N_T1_AD2N_35
TRANS_CMOS_TX_D0	M19	IO_L7P_T1_AD2P_35
TRANS_CMOS_TX_D5	M18	IO_L8N_T1_AD10N_35
TRANS_CTRL_OUT6	M17	IO_L8P_T1_AD10P_35
FPGA_L19	L20	IO_L9N_T1_DQS_AD3N_35
TRANS_CMOS_TX_FRAME	L19	IO_L9P_T1_DQS_AD3P_35
TRANS_CMOS_TX_D11	J19	IO_L10N_T1_AD11N_35
TRANS_CMOS_TX_D1	K19	IO_L10P_T1_AD11P_35
TRANS_CMOS_TX_D8	L17	IO_L11N_T1_SRCC_35
TRANS_CMOS_FB_CLK	L16	IO_L11P_T1_SRCC_35
TRANS_MRCC_DATA_CLK	K18	IO_L12N_T1_MRCC_35
TRANS_CMOS_RX_FRAME	K17	IO_L12P_T1_MRCC_35
TRANS_MRCC_CLKOUT	H17	IO_L13N_T2_MRCC_35
TRANS_CMOS_RX_D11	H16	IO_L13P_T2_MRCC_35
TRANS_ENAGC	H18	IO_L14N_T2_AD4N_SRCC_35
TRANS_CMOS_RX_D4	J18	IO_L14P_T2_AD4P_SRCC_35
	F20	IO_L15N_T2_DQS_AD12N_35
TRANS_CMOS_RX_D9	F19	IO_L15P_T2_DQS_AD12P_35
TRANS_CMOS_RX_D7	G18	IO_L16N_T2_35
TRANS_SYNC	G17	IO_L16P_T2_35
TRANS_CMOS_RX_D2	H20	IO_L17N_T2_AD5N_35
TRANS_CTRL_OUT4	J20	IO_L17P_T2_AD5P_35
TRANS_CMOS_RX_D6	G20	IO_L18N_T2_AD13N_35
TRANS_CMOS_RX_D5	G19	IO_L18P_T2_AD13P_35
TRANS_CMOS_TX_D10	G15	IO_L19N_T3_VREF_35
TRANS_CTRL_OUT2	H15	IO_L19P_T3_35
TRANS_CTRL_IN3	J14	IO_L20N_T3_AD6N_35
TRANS_CMOS_TX_D7	K14	IO_L20P_T3_AD6P_35
TRANS_CTRL_OUT5	N16	IO_L21N_T3_DQS_AD14N_35
TRANS_CTRL_IN1	N15	IO_L21P_T3_DQS_AD14P_35
TRANS_CTRL_IN0	L15	IO_L22N_T3_AD7N_35
TRANS_CMOS_TX_D3	L14	IO_L22P_T3_AD7P_35
TRANS_CMOS_TX_D9	M15	IO_L23N_T3_35
TRANS_CMOS_TX_D6	M14	IO_L23P_T3_35
TRANS_CMOS_TX_D4	J16	IO_L24N_T3_AD15N_35
	K16	IO_L24P_T3_AD15P_35
+1V8	C19	VCCO_35[6]

14 FPGA_M20
14 FPGA_L19

Decoupling:
+1V8
C139 0.1uF GND
C140 0.1uF GND
C141 0.1uF GND
+1V8 +1V8 +1V8

(handwritten red note: 余ったPin — "余ったPin")

FPGA_JTAG_TCK
FPGA_JTAG_TDI
FPGA_JTAG_TDO
FPGA_JTAG_TMS

FPGA_AUXADC_N
FPGA_AUXADC_P

FPGA_VREF

FPGA_LED_DONE

- BANK0=1.8V CFGBVS Set to GND
- Configure Done Indicator

- Temperature-sensing Not Use
  Tie to GND
- Indicates initialization of Configuration Memory.
  Not use
- Asynchronous reset to configuration logic.
  Active low. Not use
- RSVDGND Leave floating

+1V8

R28
0R

R59 4.7K   FPGA_LED_DONE

R48 4.7K
R47 4.7K

+1V8

C138
0.1uF

GND

FPGA_JTAG_TCK
FPGA_JTAG_TDI
FPGA_JTAG_TDO
FPGA_JTAG_TMS

FPGA_AUXADC_N
FPGA_AUXADC_P

FPGA_VREF

不用外部参考的时候怎么处理？

R53
0R
GND

U2A	xc7z020clg400
M6	CFGBVS_0
R11	DONE_0
M10	DXN_0
M9	DXP_0
J10	GNDADC_0
R10	INIT_B_0
L6	PROGRAM_B_0
F10	RSVDGND
T6	RSVDVCC1
R6	RSVDVCC2
N6	RSVDVCC3
F9	TCK_0
G6	TDI_0
F6	TDO_0
J6	TMS_0
J9	VCCADC_0
F11	VCCBATT_0
K6	VCCO_0
L10	VN_0
K9	VP_0
K10	VREFN_0
L9	VREFP_0

加滤头，重新检查

+1V0

C64	C65	C52	C53	C54	C55	C56	C57	C58	C59	C60	C61	C62	C63
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

GND

+1V8

C146	C117	C66	C67	C68	C69	C70	C71	C72	C73	C74	C75	C76	C77	C78	C79
0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF	0.1uF

GND

U2H	xc7z020clg400
A8	GND[59]
J11	VCCAUX[6]
G11	VCCBRAM[2]
G13	VCCINT[9]
G9	VCCPAUX[5]
G7	VCCPINT[6]
G8	VCCPLL

GND
+1V8
+1V0
+1V0
+1V0

测试切换稳定性

测试正负行为

检查 P/N

搞明白 ID 方向

4 pin 6 pin

TRANS_CTRL_IN[0..3] TRANS_CTRL_IN[0..3]
TRANS_CTRL_IN0
TRANS_CTRL_IN1
TRANS_CTRL_IN2
TRANS_CTRL_IN3

TRANS_CTRL_OUT[0..7] TRANS_CTRL_OUT[0..7]
TRANS_CTRL_OUT0
TRANS_CTRL_OUT1
TRANS_CTRL_OUT2
TRANS_CTRL_OUT3
TRANS_CTRL_OUT4
TRANS_CTRL_OUT5
TRANS_CTRL_OUT6
TRANS_CTRL_OUT7

TRANS_CMOS_RX_D[0..11] TRANS_CMOS_RX_D[0..11]
TRANS_CMOS_RX_D0
TRANS_CMOS_RX_D1
TRANS_CMOS_RX_D2
TRANS_CMOS_RX_D3
TRANS_CMOS_RX_D4
TRANS_CMOS_RX_D5
TRANS_CMOS_RX_D6
TRANS_CMOS_RX_D7
TRANS_CMOS_RX_D8
TRANS_CMOS_RX_D9
TRANS_CMOS_RX_D10
TRANS_CMOS_RX_D11
TRANS_CMOS_RX_FRAME TRANS_CMOS_RX_FRAME
TRANS_MRCC_DATA_CLK TRANS_MRCC_DATA_CLK

TRANS_CMOS_TX_D[0..11] TRANS_CMOS_TX_D[0..11]
TRANS_CMOS_TX_D0
TRANS_CMOS_TX_D1
TRANS_CMOS_TX_D2
TRANS_CMOS_TX_D3
TRANS_CMOS_TX_D4
TRANS_CMOS_TX_D5
TRANS_CMOS_TX_D6
TRANS_CMOS_TX_D7
TRANS_CMOS_TX_D8
TRANS_CMOS_TX_D9
TRANS_CMOS_TX_D10
TRANS_CMOS_TX_D11
TRANS_CMOS_TX_FRAMED TRANS_CMOS_TX_FRAME
TRANS_CMOS_FB_CLKD TRANS_CMOS_FB_CLK

TRANS_MRCC_CLKOUT TRANS_MRCC_CLKOUT

TRANS_SYNCD TRANS_SYNC
TRANS_ENAGCD TRANS_ENAGC
LDO_END LDO_EN
TRANS_ENABLED TRANS_ENABLE
TRANS_TXNRXD TRANS_TXNRX

TRANS_RSTD TRANS_RST

TRANS_SPI_SSD TRANS_SPI_SS
TRANS_SPI_CLKD TRANS_SPI_CLK
TRANS_SPI_MOSID TRANS_SPI_MOSI
TRANS_SPI_MISOD TRANS_SPI_MISO

TRANS_AUX_ADCD TRANS_AUX_ADC
TRANS_AUX_DAC1D TRANS_AUX_DAC1
TRANS_AUX_DAC2D TRANS_AUX_DAC2

TRANS_GPO_[0..3] TRANS_GPO_[0..3]
TRANS_GPO_0
TRANS_GPO_1
TRANS_GPO_2
TRANS_GPO_3

LDO_END LDO_EN

FB1
VCC_1V3_TRANS
C84 C85 C86
0.1uF 0.1uF 0.1uF
GND GND GND

FB9
C87 C88 C83
0.1uF 0.1uF 0.1uF

VCC_1V3_TRANS_1

L2 L3 L4 L5
L   L   L L
0.1uF

GND

U3A
AD9361

J5
Conn_Coaxial
FL1
0850BM14E0016
1 UBP RF_P 4   TRANS_TXRF0_P
          RF_N 3   TRANS_TXRF0_N
     GND RX/TX 2
2
GND
0.1uF

J6
Conn_Coaxial
FL2
0850BM14E0016
1 UBP RF_P 4   TRANS_TXRF1_P
          RF_N 3   TRANS_TXRF1_N
     GND RX/TX 2
2
GND
0.1uF
?

M7   TX1A+
M8   TX1A−
M9   TX1B+
M10 TX1B−
A8   TX2A+
A7   TX2A−
A10 TX2B+
A9   TX2B−
M5   TXMON1
A5   TXMON2

A12 TX_EXT_LO_IN

J9
Conn_Coaxial
C17 0.1uF
GND

FL3
0850BM14E0016
1 UBP RF_P 4   TRANS_RXRF0_P
          RF_N 3   TRANS_RXRF0_N
     GND RX/TX 2
2
GND
0.1uF

M1   RX1A+
M2   RX1A−
H1   RX1B+
J1   RX1B−
K1   RX1C+
L1   RX1C−

J8
Conn_Coaxial
FL4
0850BM14E0016
1 UBP RF_P 4   TRANS_RXRF1_P
          RF_N 3   TRANS_RXRF1_N
     GND RX/TX 2
2
GND
0.1uF

A2   RX2A+
A1   RX2A−
E1   RX2B+
F1   RX2B−
D1   RX2C+
C1   RX2C−

J12
Conn_Coaxial
C20 0.1uF
GND

G1   RX_EXT_LO_IN

P0_D0/TX_D0− E12 TRANS_CMOS_TX_D0
P0_D1/TX_D0+ D11 TRANS_CMOS_TX_D1
P0_D2/TX_D1− E11 TRANS_CMOS_TX_D2
P0_D3/TX_D1+ D10 TRANS_CMOS_TX_D3
P0_D4/TX_D2− E10 TRANS_CMOS_TX_D4
P0_D5/TX_D2+ D9   TRANS_CMOS_TX_D5
P0_D6/TX_D3− E9   TRANS_CMOS_TX_D6
P0_D7/TX_D3+ D8   TRANS_CMOS_TX_D7
P0_D8/TX_D4− E8   TRANS_CMOS_TX_D8
P0_D9/TX_D4+ D7   TRANS_CMOS_TX_D9
P0_D10/TX_D5− F8   TRANS_CMOS_TX_D10
P0_D11/TX_D5+ E7   TRANS_CMOS_TX_D11
TX_FRAME−   H9   TRANS_CMOS_TX_FRAME
TX_FRAME+   G9

P1_D0/RX_D0− K11 TRANS_CMOS_RX_D0
P1_D1/RX_D0+ J12 TRANS_CMOS_RX_D1
P1_D2/RX_D1− K10 TRANS_CMOS_RX_D2
P1_D3/RX_D1+ J11 TRANS_CMOS_RX_D3
P1_D4/RX_D2− K9   TRANS_CMOS_RX_D4
P1_D5/RX_D2+ J10 TRANS_CMOS_RX_D5
P1_D6/RX_D3− K8   TRANS_CMOS_RX_D6
P1_D7/RX_D3+ J9   TRANS_CMOS_RX_D7
P1_D8/RX_D4− K7   TRANS_CMOS_RX_D8
P1_D9/RX_D4+ J8   TRANS_CMOS_RX_D9
P1_D10/RX_D5− J7   TRANS_CMOS_RX_D10
P1_D11/RX_D5+ H8   TRANS_CMOS_RX_D11
RX_FRAME−   G7
RX_FRAME+   H7   TRANS_CMOS_RX_FRAME

DATA_CLK−   H11 TRANS_MRCC_DATA_CLK
DATA_CLK+   G11
FB_CLK+   F10 TRANS_CMOS_FB_CLK
FB_CLK−   G10

RESET   K5   TRANS_RST
ENABLE   G6   TRANS_ENABLE
TEST/ENABLE   C4
SYNC_IN   H5   TRANS_SYNC
CLK_OUT   J6   TRANS_MRCC_CLKOUT
TXRX   H4   TRANS_TXNRX
EN_AGC   G5   TRANS_ENAGC

SPI_EN   K6   TRANS_SPI_SS
SPI_CLK   J5   TRANS_SPI_CLK
SPI_MOSI   J4   TRANS_SPI_MOSI
SPI_MISO   L6   TRANS_SPI_MISO

CTRL_IN0   C5   TRANS_CTRL_IN0
CTRL_IN1   C6   TRANS_CTRL_IN1
CTRL_IN2   D6   TRANS_CTRL_IN2
CTRL_IN3   D5   TRANS_CTRL_IN3
CTRL_OUT0   D4   TRANS_CTRL_OUT0
CTRL_OUT1   E4   TRANS_CTRL_OUT1
CTRL_OUT2   E5   TRANS_CTRL_OUT2
CTRL_OUT3   E6   TRANS_CTRL_OUT3
CTRL_OUT4   F6   TRANS_CTRL_OUT4
CTRL_OUT5   F5   TRANS_CTRL_OUT5
CTRL_OUT6   F4   TRANS_CTRL_OUT6
CTRL_OUT7   G4   TRANS_CTRL_OUT7

TRANS_AUX_ADC   L5   AUXADC
TRANS_AUX_DAC1 B3   AUXDAC1
TRANS_AUX_DAC2 C3   AUXDAC2

TRANS_GPO_0   B7   GPO_0
TRANS_GPO_1   B6   GPO_1
TRANS_GPO_2   B5   GPO_2
TRANS_GPO_3   B4   GPO_3

Receive Data Clock Output. These pins transmit the DATA_CLK signal that is used
by the BBP to clock RX data. In CMOS mode, use DATA_CLK_P as the output and
leave DATA_CLK_N unconnected.

Feedback Clock. These pins receive the FB_CLK signal that clocks in TX data.
In CMOS mode, use FB_CLK_P as the input and tie FB_CLK_N to ground.

+1V8
C135
0.1uF
GND
LDO_EN

U12 Si513A_2.5x3.2mm
+1V8
VDD 6
1 OE   CLK− 5
2 FS   CLK+ 4
   GND 3
GND

40M ?

TRANS_OSC_P C80 0.1uF
TRANS_OSC_N C81 0.1uF

M11 XTALP
M12 XTALN
TRANS_RBIAS
RBIAS
R18
R
GND
GND

干啥的? (handwritten)
加不加电阻 (handwritten)

Sheet: /Transceiver RF/
File: Transceiver_RF.kicad_sch
Title:
Size: A3   Date: Rev:
KiCad E.D.A. kicad (6.99.0−621−g810a49ef1b)   Id: 8/13

U3B
AD9361

Pin	Signal		Signal	Pin
D3	VddA1P3_RX_TX		NC	A3
			NC	M3
	VDDA_RX_TX		VssA	A4
B9	VddA1P3_TX_LO		VssA	A6
B10	VddA1P3_TX_VCO_LDO		VssA	B1
E3	VddA1P3_TX_LO_BUFFER		VssA	B2
K3	VddA1P3_TX_SYNTH		VssA	B12
D2	VddA1P3_RX_RF		VssA	C2
E2	VddA1P3_RX_LO		VssA	C7
F2	VddA1P3_RX_VCO_LDO		VssA	C8
J3	VddA1P3_RX_SYNTH		VssA	C9
K4	VddA1P3_BB		VssA	C10
			VssA	C11
			VssA	C12
G2	RX_VCO_LDO_OUT		VssA	F3
G3	VddA1P1_RX_VCO		VssA	H2
B11	TX_VCO_LDO_OUT		VssA	H3
A11	VddA1P1_TX_VCO		VssA	H6
H12	Vdd_INTERFACE		VssA	J2
B8	Vdd_GPO		VssA	K2
F12	VddD1P3_DIG		VssA	L2

VCC_1V3_TRANS_1

FB2 C104 VCC_1V3_TRANS_1 FB5 C112
C98   C109
0.1uF   0.1uF
GND   GND   GND

VCC_1V3_TRANS_0

FB3 C105 FB6 C113
C99   C110
0.1uF   0.1uF
GND   GND   GND

FB4 C82
C100   C111 C114
0.1uF   0.1uF
GND   GND   GND

VCC_1V3_TRANS_0 FB7

VDDA_RX_TX
VDDA_TX_LO
VDDA_TX_SYNTH
VDDA_RX_LO
VDDA_RX_SYNTH
VDDA_BB

RX_VCO
TX_VCO

+1V8
C134 C133 C132
0.1uF 0.1uF 0.1uF
GND

R11   R12
C6   C12
18pF   18pF
C1   C9
14.3K 18pF 14.3K 18pF
GND GND   GND GND

+1V8

1.8V

FB8
VCC_1V3_TRANS VDDA_DIGI_1V3
C136 C137
0.1uF 0.1uF
GND

GND

PS Config

TRANS_RST — TRANS_RST — TRANS_RST
TRANS_SPI_SS — TRANS_SPI_SS — TRANS_SPI_SS
TRANS_SPI_MOSI — TRANS_SPI_MOSI — TRANS_SPI_MOSI
TRANS_SPI_CLK — TRANS_SPI_CLK — TRANS_SPI_CLK
TRANS_SPI_MISO — TRANS_SPI_MISO — TRANS_SPI_MISO

PS_MIO19_SPI_MOSI — PS_MIO19_SPI_MOSI — PS_MIO19_SPI_MOSI
PS_MIO17_SPI_MISO — PS_MIO17_SPI_MISO — PS_MIO17_SPI_MISO
PS_MIO16_SPI_CLK — PS_MIO16_SPI_CLK — PS_MIO16_SPI_CLK
PS_MIO18_SPI_SS — PS_MIO18_SPI_SS — PS_MIO18_SPI_SS
PS_MIO20_SPI_SS1 — PS_MIO20_SPI_SS1 — PS_MIO20_SPI_SS1
PS_MIO21_SPI_SS2 — PS_MIO21_SPI_SS2 — PS_MIO21_SPI_SS2

UART_TX — UART_TX — UART_TX
UART_RX — UART_RX — UART_RX

PS_MIO11_SDA — PS_MIO11_SDA — PS_MIO11_SDA
PS_MIO10_SCL — PS_MIO10_SCL — PS_MIO10_SCL

File: PS_Config.kicad_sch

PS_MIO27_500_USB_RESETB — PS_MIO27_500_USB_RESETB — PS_MIO27_500_USB_RESETB
PS_MIO36_501_USB0_CLK — PS_MIO36_501_USB0_CLK — PS_MIO36_501_USB0_CLK
PS_MIO29_501_USB0_DIR — PS_MIO29_501_USB0_DIR — PS_MIO29_501_USB0_DIR
PS_MIO30_501_USB0_STP — PS_MIO30_501_USB0_STP — PS_MIO30_501_USB0_STP
PS_MIO31_501_USB0_NXT — PS_MIO31_501_USB0_NXT — PS_MIO31_501_USB0_NXT

PS_MIO_501_USB0_D[0..7] — PS_MIO_501_USB0_D[0..7] — PS_MIO_501_USB0_D[0..7]

LDO_EN — LDO_EN — LDO_EN

PS—SRST# — PS—SRST# — PS—SRST#

DCDC_PG_1V35 — DCDC_PG_1V35 — DCDC_PG_1V35

PS DDR

File: PS_DDR.kicad_sch

PL Transceiver

TRANS_CTRL_IN[0..3] — TRANS_CTRL_IN[0..3] — TRANS_CTRL_IN[0..3]
TRANS_CTRL_OUT[0..7] — TRANS_CTRL_OUT[0..7] — TRANS_CTRL_OUT[0..7]

TRANS_CMOS_RX_D[0..11] — TRANS_CMOS_RX_D[0..11] — TRANS_CMOS_RX_D[0..11]
TRANS_CMOS_RX_FRAME — TRANS_CMOS_RX_FRAME — TRANS_CMOS_RX_FRAME
TRANS_MRCC_DATA_CLK — TRANS_MRCC_DATA_CLK — TRANS_MRCC_DATA_CLK

TRANS_CMOS_TX_D[0..11] — TRANS_CMOS_TX_D[0..11] — TRANS_CMOS_TX_D[0..11]
TRANS_CMOS_TX_FRAME — TRANS_CMOS_TX_FRAME — TRANS_CMOS_TX_FRAME
TRANS_CMOS_FB_CLK — TRANS_CMOS_FB_CLK — TRANS_CMOS_FB_CLK

TRANS_MRCC_CLKOUT — TRANS_MRCC_CLKOUT — TRANS_MRCC_CLKOUT

TRANS_SYNC — TRANS_SYNC — TRANS_SYNC
TRANS_ENAGC — TRANS_ENAGC — TRANS_ENAGC

TRANS_ENABLE — TRANS_ENABLE — TRANS_ENABLE
TRANS_TXNRX — TRANS_TXNRX — TRANS_TXNRX

File: PL_Transceiver.kicad_sch

PL Connector

FPGA_SRCCN_Y8 — FPGA_SRCCN_Y8 — FPGA_SRCCN_Y8

ARD_PWM[2..7] — ARD_PWM[2..7]
ARD_PWM2 — FPGA_Y19
ARD_PWM3 — FPGA_Y18
ARD_PWM4 — FPGA_Y17
ARD_PWM5 — FPGA_Y16
ARD_PWM6 — FPGA_Y14
ARD_PWM7 — FPGA_Y13

ARD_ANALOG[0..7] — ARD_ANALOG[0..7]
ARD_ANALOG0 — FPGA_MRCCP_Y7
ARD_ANALOG1 — FPGA_MRCCN_Y6
ARD_ANALOG2 — FPGA_W6
ARD_ANALOG3 — FPGA_SRCCP_Y9
ARD_ANALOG4 — FPGA_Y11
ARD_ANALOG5 — FPGA_Y12
ARD_ANALOG6
ARD_ANALOG7

File: PL_Connector.kicad_sch

PL Config

FPGA_LED_DONE — FPGA_LED_DONE — FPGA_LED_DONE

FPGA_AUXADC_N — FPGA_AUXADC_N — FPGA_AUXADC_N
FPGA_AUXADC_P — FPGA_AUXADC_P — FPGA_AUXADC_P

FPGA_JTAG_TMS — FPGA_JTAG_TMS — FPGA_JTAG_TMS
FPGA_JTAG_TDO — FPGA_JTAG_TDO — FPGA_JTAG_TDO
FPGA_JTAG_TDI — FPGA_JTAG_TDI — FPGA_JTAG_TDI
FPGA_JTAG_TCK — FPGA_JTAG_TCK — FPGA_JTAG_TCK

FPGA_VREF — FPGA_VREF — FPGA_VREF

File: PL_Config.kicad_sch

FPGA_MRCCP_Y7
FPGA_MRCCN_Y6
FPGA_W6
FPGA_SRCCP_Y9
FPGA_Y11
FPGA_Y12

FPGA_SRCCN_Y8

FPGA_Y19
FPGA_Y18
FPGA_Y17
FPGA_Y16
FPGA_Y14
FPGA_Y13

U2B   xc7z020clq400

Net	Pin	Function
FPGA_V5	V5	IO_L6N_T0_VREF_13
FPGA_U7	U7	IO_L11P_T1_SRCC_13
	V7	IO_L11N_T1_SRCC_13
	T9	IO_L12P_T1_MRCC_13
FPGA_U10	U10	IO_L12N_T1_MRCC_13
FPGA_MRCCP_Y7	Y7	IO_L13P_T2_MRCC_13
FPGA_MRCCN_Y6	Y6	IO_L13N_T2_MRCC_13
FPGA_SRCCP_Y9	Y9	IO_L14P_T2_SRCC_13
FPGA_SRCCN_Y8	Y8	IO_L14N_T2_SRCC_13
	V8	IO_L15P_T2_DQS_13
FPGA_W8	W8	IO_L15N_T2_DQS_13
FPGA_W10	W10	IO_L16P_T2_13
FPGA_W9	W9	IO_L16N_T2_13
	U9	IO_L17P_T2_13
	U8	IO_L17N_T2_13
FPGA_W11	W11	IO_L18P_T2_13
FPGA_Y11	Y11	IO_L18N_T2_13
	T5	IO_L19P_T3_13
	U5	IO_L19N_T3_VREF_13
FPGA_Y12	Y12	IO_L20P_T3_13
FPGA_Y13	Y13	IO_L20N_T3_13
FPGA_V11	V11	IO_L21P_T3_DQS_13
FPGA_V10	V10	IO_L21N_T3_DQS_13
	V6	IO_L22P_T3_13
FPGA_W6	W6	IO_L22N_T3_13
VCC_BANK34	T8	VCCO_13[4]

U2C   xc7z020clq400

FPGA_U13   R40   1K   GND

Net	Pin	Function
FPGA_R19	R19	IO_0_34
FPGA_T19	T19	IO_25_34
FPGA_T10	T10	IO_L1N_T0_34
FPGA_T11	T11	IO_L1P_T0_34
FPGA_U12	U12	IO_L2N_T0_34
FPGA_T12	T12	IO_L2P_T0_34
FPGA_V13	V13	IO_L3N_T0_DQS_34
FPGA_U13	U13	IO_L3P_T0_DQS_PUDC_B_34
FPGA_W13	W13	IO_L4N_T0_34
FPGA_V12	V12	IO_L4P_T0_34
FPGA_T15	T15	IO_L5N_T0_34
FPGA_T14	T14	IO_L5P_T0_34
FPGA_R14	R14	IO_L6N_T0_VREF_34
FPGA_P14	P14	IO_L6P_T0_34
FPGA_Y17	Y17	IO_L7N_T1_34
FPGA_Y16	Y16	IO_L7P_T1_34
FPGA_Y14	Y14	IO_L8N_T1_34
FPGA_W14	W14	IO_L8P_T1_34
FPGA_U17	U17	IO_L9N_T1_DQS_34
FPGA_T16	T16	IO_L9P_T1_DQS_34
FPGA_W15	W15	IO_L10N_T1_34
FPGA_V15	V15	IO_L10P_T1_34
FPGA_U15	U15	IO_L11N_T1_SRCC_34
FPGA_U14	U14	IO_L11P_T1_SRCC_34
FPGA_U19	U19	IO_L12N_T1_MRCC_34
FPGA_U18	U18	IO_L12P_T1_MRCC_34
FPGA_P19	P19	IO_L13N_T2_MRCC_34
	N18	IO_L13P_T2_MRCC_34
FPGA_P20	P20	IO_L14N_T2_SRCC_34
FPGA_N20	N20	IO_L14P_T2_SRCC_34
FPGA_U20	U20	IO_L15N_T2_DQS_34
FPGA_T20	T20	IO_L15P_T2_DQS_34
FPGA_W20	W20	IO_L16N_T2_34
FPGA_V20	V20	IO_L16P_T2_34
FPGA_Y19	Y19	IO_L17N_T2_34
FPGA_Y18	Y18	IO_L17P_T2_34
FPGA_W16	W16	IO_L18N_T2_34
FPGA_V16	V16	IO_L18P_T2_34
	R17	IO_L19N_T3_VREF_34
	R16	IO_L19P_T3_34
	R18	IO_L20N_T3_34
FPGA_T17	T17	IO_L20P_T3_34
FPGA_V18	V18	IO_L21N_T3_DQS_34
FPGA_V17	V17	IO_L21P_T3_DQS_34
FPGA_W19	W19	IO_L22N_T3_34
FPGA_W18	W18	IO_L22P_T3_34
	P18	IO_L23N_T3_34
	N17	IO_L23P_T3_34
	P16	IO_L24N_T3_34
FPGA_P15	P15	IO_L24P_T3_34
VCC_BANK34	N19	VCCO_34[6]

Connector J4 — BTB Connector schematic

Left signal	Pin	Pin	Right signal
FPGA_L19	1	2	TRANS_GPO_1
FPGA_M20	3	4	TRANS_GPO_2
FPGA_N20	5	6	TRANS_GPO_3
FPGA_P20	7	8	TRANS_GPO_0
FPGA_P19	9	10	FPGA_P14
FPGA_R19	11	12	FPGA_P15
FPGA_U20	13	14	FPGA_W20
FPGA_T20	15	16	FPGA_V20
FPGA_U19	17	18	FPGA_W19
FPGA_T19	19	20	
FPGA_U18	21	22	FPGA_W18
	23	24	FPGA_V18
FPGA_U17	25	26	VCC_BANK34
FPGA_T17	27	28	FPGA_V17
	29	30	FPGA_W16
FPGA_T16	31	32	FPGA_V16
FPGA_U15	33	34	FPGA_W15
FPGA_T15	35	36	FPGA_V15
FPGA_U14	37	38	FPGA_W14
FPGA_T14	39	40	
FPGA_U13	41	42	FPGA_W13
FPGA_R14	43	44	FPGA_V13
FPGA_U12	45	46	
FPGA_T12	47	48	FPGA_V12
	49	50	FPGA_W11
FPGA_T11	51	52	FPGA_V11
FPGA_U10	53	54	FPGA_W10
FPGA_T10	55	56	FPGA_V10
	57	58	
FPGA_AUXADC_N	59	60	FPGA_W9
FPGA_AUXADC_P	61	62	FPGA_W8
	63	64	ARD_AREF
FPGA_U7	65	66	
	67	68	FPGA_VREF
	69	70	
FPGA_JTAG_TCK	71	72	
FPGA_JTAG_TDI	73	74	
FPGA_JTAG_TMS	75	76	FPGA_V5
FPGA_JTAG_TDO	77	78	
	79	80	

TRANS_GPO_[0..3]

VCC_BANK34

+1V8

+1V0

5024268012

GND   GND