Eric Thornton

Contact

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Education

Rochester Institute of Technology (BS/MS Electrical Engineering)- Anticipated graduation: Winter 2023.

GPA: 3.67.

Dean's List: 2020 - 2022.

Certifications & Skills

Autodesk Inventor Pro - Certified User, 2017.

Autodesk Fusion 360 - Certified User, 2018.

Programming -

C, C++, shell/bash, Python, LabVIEW, MATLAB, VHDL, Verilog.

Other -

Linux/Unix operating systems, PCB Design (ki-CAD, Cadence, Altium), Soldering, Bench-top Test Equipment.

About

Highly motivated electrical engineering student with extensive experience and interest in embedded systems, digital communication protocols, high and low-level software development, digital circuits, and phtonics. Experienced with top-down design and skilled in understanding problems holistically. Experience working in both the public and private sector, from startups to large firms Personable team member comfortable with constructive debate.

Experience

RIT Materials Science Department - Engineer (August 2022 - December 2022)

- Supported team researching light activated self healing ploymers in engineering custom solutions to imporve process consistancy.
- Worked closely with lab technictions to understand current process shortcommings and devoloped a custom dual wavelength LED exposure rig with persice intensity and exposure time control.

Z-Axis, Inc - Electrical Engineering Intern. (August 2021 - August 2022)

- Top down, complete design (CAD, machining, electrical and software) of the "LED Poker", an electromagnetic actuator designed to automatically dislodge SMT LEDs from the vacuum pickup of a 3-axis LED sorting robot.
- The LED poker increased the output of the machine from 50 LEDs/day at a maximum to a consistent 300 LEDs/day. This increase in speed and reliability allowed the company to bid on higher volume, higher value orders with confidence of on-time delivery.
- Developed the Universal Test Fixture, a complex and application agnostic system designed to apply a user defined test sequence to an arbitrary power supply, thus eliminating the need for bespoke test fixtures for each power supply. Involved the development of a high-level user oriented GUI (written in python), and a low level communication protocol (parsed in C++).

SRC, Inc - Electrical Engineering Intern. (May 2021 - August 2021)

- Developed IPMI Parse and Control (IPAC) for the Agile Condor high performance edge computing system.
- IPAC extended the standard Intelligent Platform Management Interface (IPMI) to allow access to high level OS functions (e.g. IP addresses). This allowed richer diagnostics of networked client "slice" CPUs/GPUs from the host computer if the network interface was malfunctioning.

Horizon 31, LLC – Systems Integration Specialist. (May 2020 – August 2020)

- Worked with a team to successfully diagnose and repair several issues with an in-house designed power management PCB under the pressure of a demo deadline with the project sponsor.
- Developed low level software running on embedded Linux hardware to interface a variety of sensors to a digital radio network; integrated and verified this software along with that developed by others on the team.

Oak Ridge National Laboratory, Unmanned Vehicles Development Group – Intern. (May 2019 – August 2019)

- Developed a novel packet protocol (BRNR-S.Bus) capable of transmitting low latency and fault tolerant telemetry data to unmanned vehicles over secure digital radio networks. The latency improves over 100ms vs existing solutions.
- Designed the hardware and firmware needed to implement this protocol and worked closely with other team members to integrate this hardware