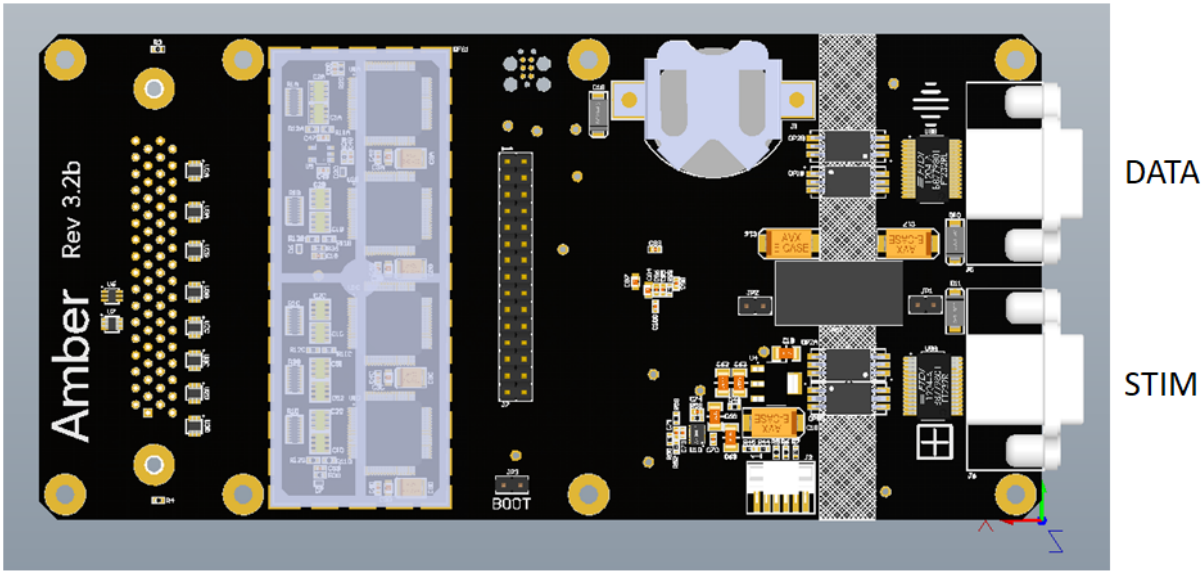
M20 EE Design Document

M20 bioamplifier is a 32 channel EEG project developed by Philo. It is designed to be connected to a PC USB port for data communication.



1. Hardware Design

1.1. DAQ

The heart of the design is the ADS1299 8 channel bioamplifier from Texas Instruments. This single IC provides the front-end amplification and 24 bit conversion. It is particularly suitable for EEG measurements as it provides a ground bias generator and built-in lead-off detection.

4 of the ADS1299s are connected together in a parallel data configuration. All 4 together provide 32 EEG channels. U1A is the master ADS1299 and provides the conversion clock to the other 3 converters to keep things synchronized. U1A is also the master bias generator.

Although the ADS1299 can provide differential or single-ended inputs, the configuration of the board allows for only single-ended inputs on channels 1-24, and the option of single-ended or differential inputs on channels 25-32.

The sample rate is 250 samples per second.

Communication with the MCU is over 4 wire SPI running at a clock speed of 4 MHz. The ADS1299 provides a signal (#DRDY) that goes low when a conversion is ready to be read out of the chip. Only the master has this signal connected to the MCU and as all timing is referenced to it. Individual chip selects are asserted to read the data from each of the ADS1299s in turn. An alternate option would be to ready the data in a daisy-chain configuration, but the parallel configuration was chosen for its speed and flexibility.

1.2. MCU

The MCU is a Kinetis (NXP/Freescale) KL27Z256 in a 64 pin QFP package. This is an Arm Cortex M0 processor running at 48 MHz with 256K of flash memory. The reasons for choosing this processor include the speed, cost, availability, and ease of development with the Kinetis tool chain.

Debugging is done through a dedicated JTAG port implemented with a special TAG connect cable. Production programming is done through the DATA USB port utilizing the built-in ROM bootloader and a special Python tool.

The MCU handles the data conversion from the ADS1299s and communication with the host PC. It is also responsible for monitoring the on-board power supplies.

4 input pins allow for identifying the hardware revision through pull-down resistors. 4 pins are also reserved for future expansion.

Although the MCU has low-power modes, in this design it is always running at full power.

1.3. Power Supplies

Power to the board comes from either one of the 2 USB connectors. USB voltage is diode-ORed and powers an isolated DC/DC converter (PS1). This provides the 4kv isolation and patient leakage current protection. Jumpers JP1 and JP2 must be installed for normal operation. These were implement to provide power flexibility in the event a battery would need to be used.

The 5V output of the DC/DC converter is linear regulated down to 3.3V. A linear regulated was chosen to provide a lower noise floor than another DC/DC. The 3.3V primary powers the MCU and digital logic.

A charge pump based converter also runs off the 3.3V rail and provides the +/-2.5V rails to the ADS1299s. Normally charge pumps are rather noisy, but this particular IC (LM27762) has built-in linear regulators following the charge pumps and is tailored to these sorts of applications.

A separate 2.5V reference is also generated to power the MCU analog section and to provide a precise reference for power supply measurements.

1.4. USB Ports

Two USB ports connect the PCB to a PC. The DATA port is used to transfer the streaming EEG data. The STIM port allows control of the board and is used to set marks in the EEG data stream.

Each port uses an FTDI232 USB to serial IC on the PC side. The MCU side implements optical isolators for patient protection. These are rated at 4kv with a maximum data rate of 10Mbps.

1.5. Real Time Clock

A real time clock is implemented. It communicates over I2C with the MCU and has battery backup.

1.6. Micro SD

A micro SD slot is provided for future expansion. It is connected to a second SPI port on the MCU.

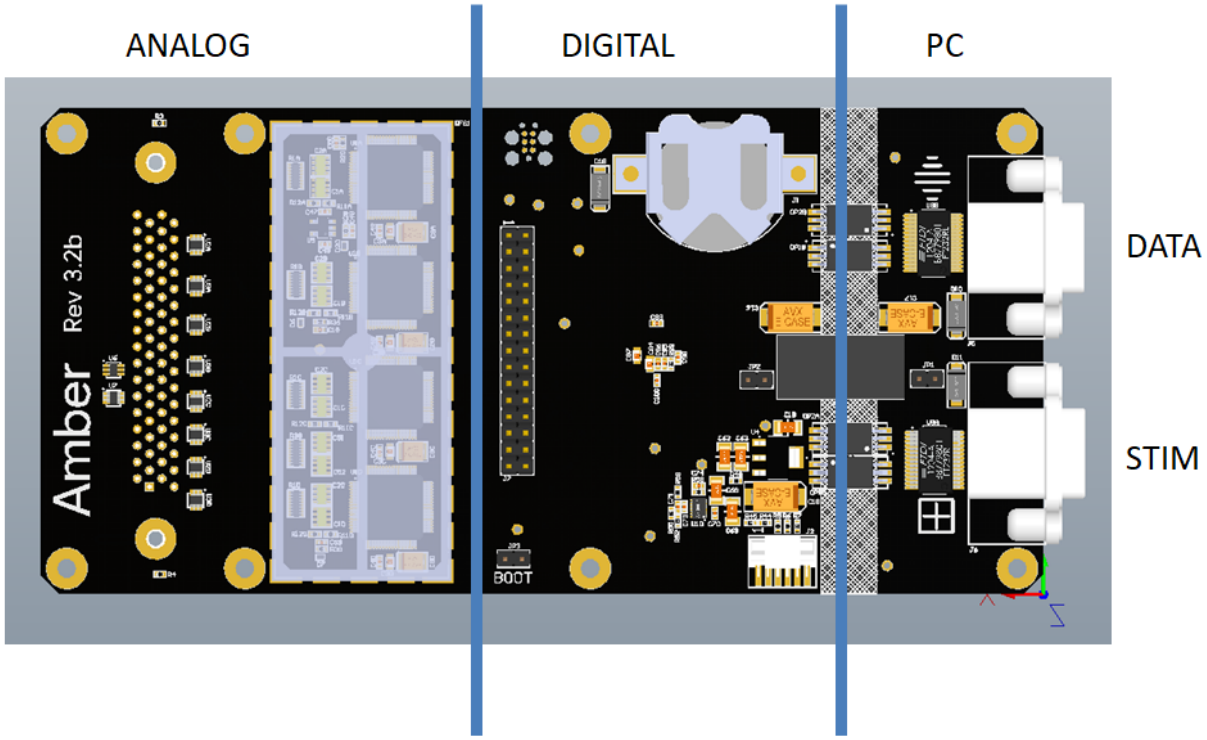
1.7. Expansion/Debug Header

Board test and expansion signals are brought to this header. They are labeled in the layout and provide an easy means of testing or debugging the board.

2. Layout

The PCB is designed as a 6 layer board. The layer stack is signal, ground plane, signal, signal, power connections, signal. Minimum line/space is 6/6 and minimum via size is 6/16. Board material is plain FR4 and finish is ENIG. This is standard for today's fabrication processes and allows the board to be manufactured at any number of board houses.

The board is separated into 3 distinct sections: PC non-isolated, digital, and analog.



2.1. PC

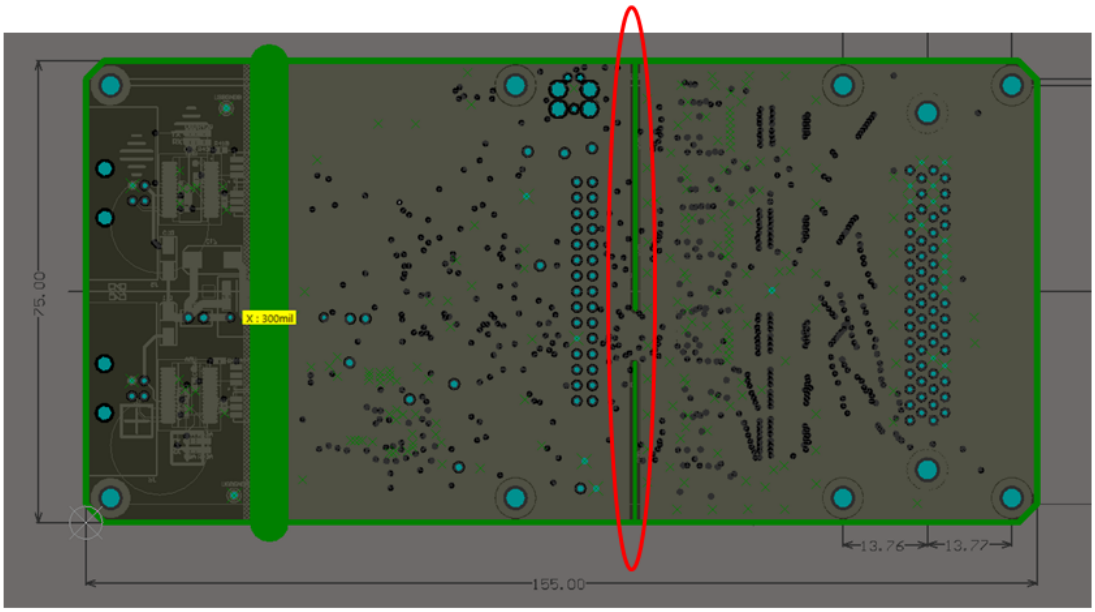
The PC side has the USB ports and half the optical isolators and DC/DC converter. Creepage and clearance is maintained at 8mm.

2.2. Digital

The digital section incorporates the power supplies and MCU. The expansion header is also included here.

2.3. Analog

The analog section protects the microvolt level EEG signals from the noisy digital sections. An RF shield is included that encapsulates the ADS1299 converters. A split ground plane separates the sensitive ground returns from the noisy digital grounds:



2.4. Test Points

Various individual test points are provided as well as the debug header for future automated testing.

3. Firmware

The firmware was developed in C using the Kinetis Design Studio. Some functions were developed with the help of Kinetis's Processor Expert which simplifies MCU configuration parameters. Some low-level drivers were hand written for the high performance and low latency needed processing the EEG data.

A main loop handles gathering EEG data, doing serial communication, and blinking LEDs. Some tasks are event driven such as EEG data ready and serial communication. These typically either buffer the data or raise flags for processing in the main loop.

A text based command line interpreter (CLI) is implemented for easy control and communication. Any terminal program can be used for sending commands. Although the CLI will respond to commands from either port, only characters on the STIM port are echoed. CLI responses on the DATA port are multiplexed with the streaming EEG data by prefixing 'CLI:' to the response line. Commands to the CLI are terminated by a carriage return.

EEG data is continuously streamed on the DATA port in ASCII format. Each channel is comma separated and the EEG value is encoded as a signed 24 bit value. A frame of EEG data has the following format:

SEQUENCE NUMBER	CH 1	CH 2	…	CH32	MARK	CR/LF

The frame is prefixed by ‘DATA:’. The sequence number is an auto incrementing unsigned 32 bit value. The mark is a user-selected data value appended to the EEG stream. Each line is terminated by a carriage return/line feed.