



# 16-Bit, Ultra-Low Glitch, Voltage Output Digital-to-Analog Converter with 2.5V, 2ppm/°C Internal Reference

Check for Samples: [DAC8560](#)

## FEATURES

- **Relative Accuracy: 4LSB**
- **Glitch Energy: 0.15nV-s**
- **MicroPower Operation: 510μA at 2.7V**
- **Internal Reference:**
  - **2.5V Reference Voltage (enabled by default)**
  - **0.02% Initial Accuracy**
  - **2ppm/°C Temperature Drift (typ)**
  - **5ppm/°C Temperature Drift (max)**
  - **20mA Sink/Source Capability**
- **Power-On Reset to Zero**
- **Power Supply: +2.7V to +5.5V**
- **16-Bit Monotonic Over Temperature Range**
- **Settling Time: 10μs to ±0.003% FSR**
- **Low-Power Serial Interface with Schmitt-Triggered Inputs**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Power-Down Capability**
- **Drop-In Compatible With [DAC8531 /01](#) and [DAC8550 /51](#)**
- **Temperature Range: –40°C to +105°C**
- **Available in a Tiny MSOP-8 Package**

## APPLICATIONS

- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo-Control**
- **PC Peripherals**
- **Portable Instrumentation**

## DESCRIPTION

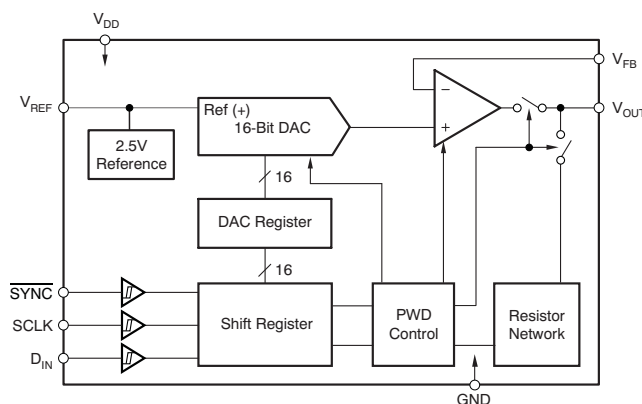
The DAC8560 is a low-power, voltage output, 16-bit digital-to-analog converter (DAC). The DAC8560 includes a 2.5V, 2ppm/°C internal reference (enabled by default), giving a full-scale output voltage range of 2.5V. The internal reference has an initial accuracy of 0.02% and can source up to 20mA at the  $V_{REF}$  pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch). The DAC8560 uses a versatile 3-wire serial interface that operates at clock rates up to 30MHz. It is compatible with standard SPI™, QSPI™, Microwire™, and digital signal processor (DSP) interfaces.

The DAC8560 incorporates a power-on-reset circuit that ensures the DAC output powers up at zero-scale and remains there until a valid code is written to the device. The DAC8560 contains a power-down feature, accessed over the serial interface, that reduces the current consumption of the device to 1.2μA at 5V.

The low-power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment. The power consumption is 2.6mW at 5V, reducing to 6μW in power-down mode.

The DAC8560 is available in an MSOP-8 package.

## FUNCTIONAL BLOCK DIAGRAM



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGING/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC8560A	±12	±1	25	MSOP-8	DGK	–40°C TO +105°C	D860
DAC8560B	±8	±1	25				
DAC8560C	±12	±1	5				
DAC8560D	±8	±1	5				

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		UNIT
$V_{DD}$ to GND		–0.3V to 6V
Digital input voltage to GND		–0.3V to $V_{DD} + 0.3V$
$V_{OUT}$ to GND		–0.3V to $V_{DD} + 0.3V$
Operating temperature range		–40°C to +105°C
Storage temperature range		–65°C to +150°C
Junction temperature range ( $T_J$ max)		+150°C
Power dissipation (DGK)		$(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal impedance, $\theta_{JA}$		206°C/W
Thermal impedance, $\theta_{JC}$		44°C/W
ESD rating	Human body model (HBM)	4000V
	Charged device model (CDM)	1500V

- (1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

 $V_{DD} = 2.7V$  to  $5.5V$ ,  $-40^{\circ}C$  to  $+105^{\circ}C$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE <sup>(1)</sup>							
Resolution				16			Bits
Relative accuracy		Measured by line passing through codes 485 and 64714	DAC8560A, DAC8560C		±4	±12	LSB
			DAC8560B, DAC8560D		±4	±8	LSB
Differential nonlinearity		16-bit Monotonic		±0.5		±1	LSB
Zero-code error		Measured by line passing through codes 485 and 64714.		±5		±12	mV
Full-scale error				±0.2		±0.5	% of FSR
Gain error				±0.05		±0.2	% of FSR
Zero-code error drift				±4			μV/°C
Gain temperature coefficient		V <sub>DD</sub> = 5V		±1			ppm of FSR/°C
		V <sub>DD</sub> = 2.7V		±3			
PSRR	Power supply rejection ratio	Output unloaded		1			mV/V
OUTPUT CHARACTERISTICS <sup>(2)</sup>							
Output voltage range				0		V <sub>REF</sub>	V
Output voltage settling time		To ±0.003% FSR, 0200h to FD00h, R <sub>L</sub> = 2kΩ, 0pF < C <sub>L</sub> < 200pF R <sub>L</sub> = 2kΩ, C <sub>L</sub> = 500pF		8		10	μs
				12			
Slew rate				1.8			V/μs
Capacitive load stability		R <sub>L</sub> = ∞		470			pF
		R <sub>L</sub> = 2kΩ		1000			
Code change glitch impulse		1LSB change around major carry		0.15			nV-s
Digital feedthrough		SCLK toggling, $\overline{\text{SYNC}}$ high		0.15			nV-s
DC output impedance		At mid-code input		1			Ω
Short-circuit current		V <sub>DD</sub> = 5V		50			mA
		V <sub>DD</sub> = 3V		20			
Power-up time		Coming out of power-down mode V <sub>DD</sub> = 5V		2.5			μs
		Coming out of power-down mode V <sub>DD</sub> = 3V		5			
AC PERFORMANCE <sup>(2)</sup>							
SNR		T <sub>A</sub> = +25°C, BW = 20kHz, V <sub>DD</sub> = 5V, f <sub>OUT</sub> = 1kHz, 1st 19 harmonics removed for SNR calculation		88			dB
THD				-77			dB
SFDR				79			dB
SINAD				77			dB
DAC output noise density		T <sub>A</sub> = +25°C, at mid-code input, f <sub>OUT</sub> = 1kHz		170			nV/√Hz
DAC output noise		T <sub>A</sub> = +25°C, at mid-code input, 0.1Hz to 10Hz		50			μV <sub>PP</sub>

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.

(2) Ensured by design and characterization, not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 2.7V$  to  $5.5V$ ,  $-40^{\circ}C$  to  $+105^{\circ}C$  range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE OUTPUT						
Output voltage		T <sub>A</sub> = +25°C	2.4975	2.5	2.5025	V
Initial accuracy		T <sub>A</sub> = +25°C	−0.1	±0.004	0.1	%
Output voltage temperature drift		DAC8560A, DAC8560B <sup>(3)</sup>		5	25	ppm/°C
		DAC8560C, DAC8560D <sup>(4)</sup>		2	5	
Output voltage noise		f = 0.1Hz to 10Hz		16		μV <sub>PP</sub>
Output voltage noise density (high-frequency noise)		T <sub>A</sub> = +25°C, f = 1MHz, C <sub>L</sub> = 0μF		125		nV/√Hz
		T <sub>A</sub> = +25°C, f = 1MHz, C <sub>L</sub> = 1μF		20		
		T <sub>A</sub> = +25°C, f = 1MHz, C <sub>L</sub> = 4μF		2		
Load regulation, sourcing <sup>(5)</sup>		T <sub>A</sub> = +25°C		30		μV/mA
Load regulation, sinking <sup>(5)</sup>		T <sub>A</sub> = +25°C		15		μV/mA
Output current load capability <sup>(6)</sup>				±20		mA
Line regulation		T <sub>A</sub> = +25°C		10		μV/V
Long-term stability/drift (aging) <sup>(5)</sup>		T <sub>A</sub> = +25°C, time = 0 to 1900 hours		50		ppm
Thermal hysteresis <sup>(5)</sup>		First cycle		100		ppm
		Additional cycles		25		
REFERENCE						
Internal reference current consumption		V <sub>DD</sub> = 5.5V		360		μA
		V <sub>DD</sub> = 3.6V		348		
External reference current		External V <sub>REF</sub> = 2.5V, if internal reference is disabled		20		μA
Reference input range			0		V <sub>DD</sub>	V
Reference input impedance				125		kΩ
LOGIC INPUTS <sup>(6)</sup>						
Input current				±1		μA
V <sub>INL</sub>	Logic input LOW voltage	V <sub>DD</sub> = 5V			0.8	V
		V <sub>DD</sub> = 3V			0.6	
V <sub>INH</sub>	Logic input HIGH voltage	V <sub>DD</sub> = 5V	2.4			V
		V <sub>DD</sub> = 3V	2.1			
Pin capacitance					3	pF
POWER REQUIREMENTS						
V <sub>DD</sub>			2.7		5.5	V
I <sub>DD</sub> <sup>(7)</sup>	Normal mode	V <sub>DD</sub> = 3.6V to 5.5V, V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND		0.530	0.850	mA
		V <sub>DD</sub> = 2.7V to 3.6V, V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND		0.510	0.840	
	All power-down modes	V <sub>DD</sub> = 3.6V to 5.5V, V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND		1.2	2.5	μA
		V <sub>DD</sub> = 2.7V to 3.6V, V <sub>IH</sub> = V <sub>DD</sub> and V <sub>IL</sub> = GND		0.7	2.2	
Power dissipation <sup>(7)</sup>	Normal mode	V <sub>DD</sub> = 3.6V to 5.5V		2.6	4.7	mW
		V <sub>DD</sub> = 2.7V to 3.6V		1.5	3.0	
	All power-down modes	V <sub>DD</sub> = 3.6V to 5.5V		6	14	μW
		V <sub>DD</sub> = 2.7V to 3.6V		2	8	
TEMPERATURE RANGE						
Specified performance			−40		+105	°C

(3) Reference is trimmed and tested at room temperature, and is characterized from  $-40^{\circ}C$  to  $+120^{\circ}C$ .

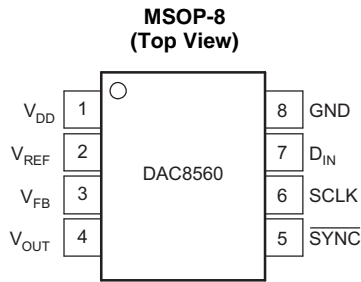
(4) Reference is trimmed and tested at two temperatures ( $+25^{\circ}C$  and  $+105^{\circ}C$ ), and is characterized from  $-40^{\circ}C$  to  $+120^{\circ}C$ .

(5) Explained in more detail in the [Application Information](#) section of this data sheet.

(6) Ensured by design and characterization, not production tested.

(7) Input code = 32768, reference current included, no load.

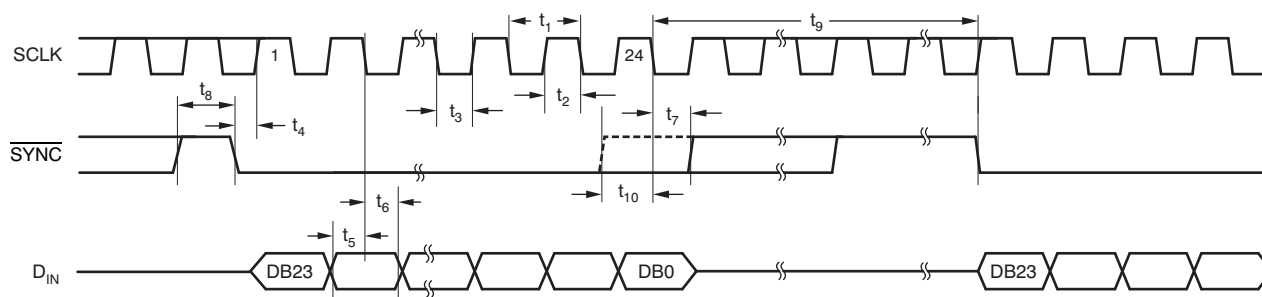
## PIN CONFIGURATION



## PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V <sub>DD</sub>	Power supply input, 2.7V to 5.5V.
2	V <sub>REF</sub>	Reference voltage input/output.
3	V <sub>FB</sub>	Feedback connection for the output amplifier. For voltage output operation, tie to V <sub>OUT</sub> externally.
4	V <sub>OUT</sub>	Analog output voltage from DAC. The output amplifier has rail-to-rail operation.
5	$\overline{\text{SYNC}}$	Level-triggered control input (active LOW). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes LOW, it enables the input shift register, and data is sampled on subsequent falling clock edges. The DAC output updates following the 24th clock. If $\overline{\text{SYNC}}$ is taken HIGH before the 24th clock edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC8560. Schmitt-Trigger logic Input.
6	SCLK	Serial clock input. Schmitt-Trigger logic input.
7	D <sub>IN</sub>	Serial data input. Data is clocked into the 24-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic Input.
8	GND	Ground reference point for all circuitry on the part.

## SERIAL WRITE OPERATION



## TIMING REQUIREMENTS<sup>(1) (2)</sup>

$V_{DD} = 2.7V$  to  $5.5V$ , all specifications  $-40^{\circ}C$  to  $+105^{\circ}C$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_1^{(3)}$ SCLK cycle time	$V_{DD} = 2.7V$ to $3.6V$	50			ns
	$V_{DD} = 3.6V$ to $5.5V$	33			
$t_2$ SCLK HIGH time	$V_{DD} = 2.7V$ to $3.6V$	13			ns
	$V_{DD} = 3.6V$ to $5.5V$	13			
$t_3$ SCLK LOW time	$V_{DD} = 2.7V$ to $3.6V$	22.5			ns
	$V_{DD} = 3.6V$ to $5.5V$	13			
$t_4$ $\overline{SYNC}$ to SCLK rising edge setup time	$V_{DD} = 2.7V$ to $3.6V$	0			ns
	$V_{DD} = 3.6V$ to $5.5V$	0			
$t_5$ Data setup time	$V_{DD} = 2.7V$ to $3.6V$	5			ns
	$V_{DD} = 3.6V$ to $5.5V$	5			
$t_6$ Data hold time	$V_{DD} = 2.7V$ to $3.6V$	4.5			ns
	$V_{DD} = 3.6V$ to $5.5V$	4.5			
$t_7$ SCLK falling edge to $\overline{SYNC}$ rising edge	$V_{DD} = 2.7V$ to $3.6V$	0			ns
	$V_{DD} = 3.6V$ to $5.5V$	0			
$t_8$ Minimum $\overline{SYNC}$ HIGH time	$V_{DD} = 2.7V$ to $3.6V$	50			ns
	$V_{DD} = 3.6V$ to $5.5V$	33			
$t_9$ 24th SCLK falling edge to $\overline{SYNC}$ falling edge	$V_{DD} = 2.7V$ to $3.6V$	100			ns
	$V_{DD} = 3.6V$ to $5.5V$	100			
$t_{10}$ $\overline{SYNC}$ rising edge to 24th SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	$V_{DD} = 2.7V$ to $3.6V$	15			ns
	$V_{DD} = 3.6V$ to $5.5V$	15			

(1) All input signals are specified with  $t_R = t_F = 3ns$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

(2) See Serial Write Operation timing diagram.

(3) Maximum SCLK frequency is 30MHz at  $V_{DD} = 3.6V$  to  $5.5V$  and 20MHz at  $V_{DD} = 2.7V$  to  $3.6V$ .

## TYPICAL CHARACTERISTICS: Internal Reference

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

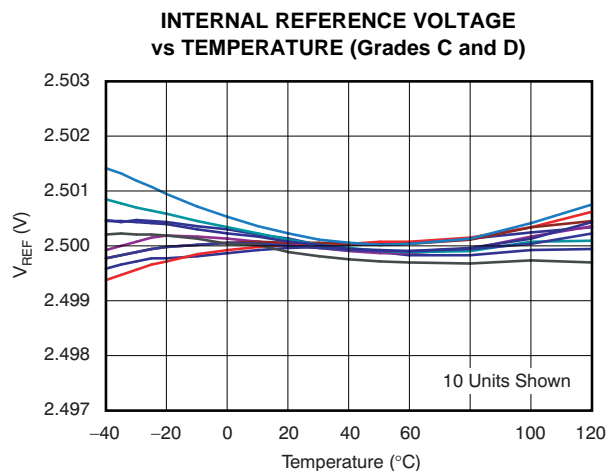


Figure 1.

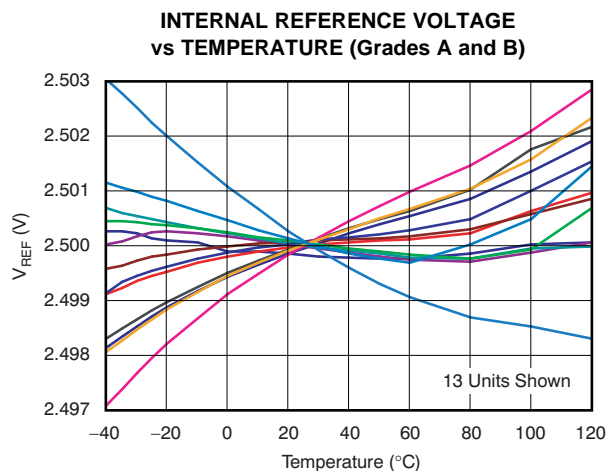


Figure 2.

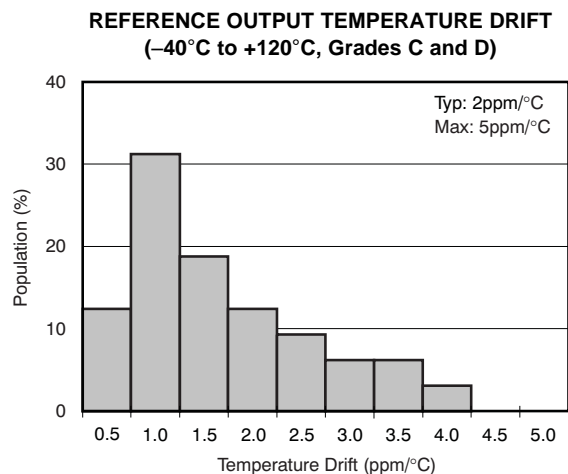


Figure 3.

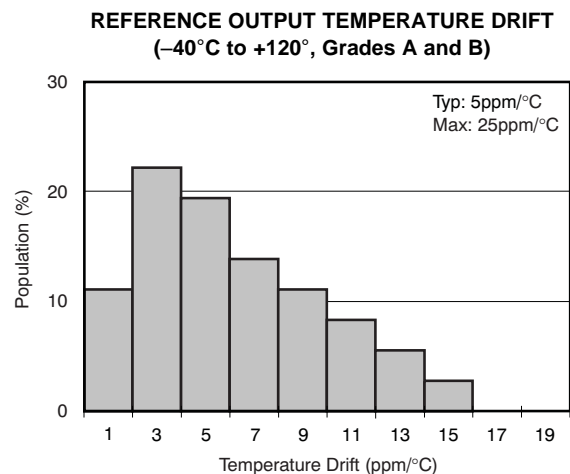


Figure 4.

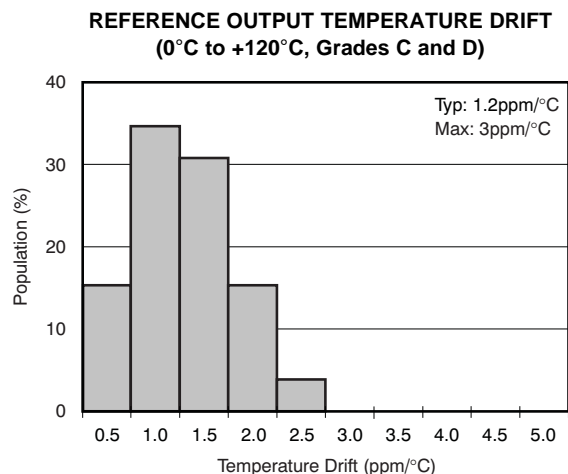


Figure 5.

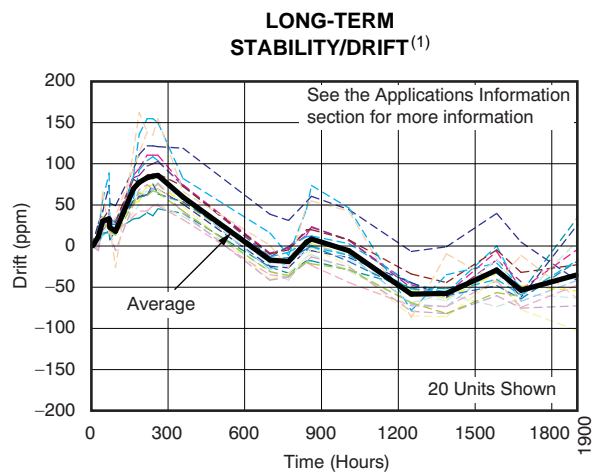


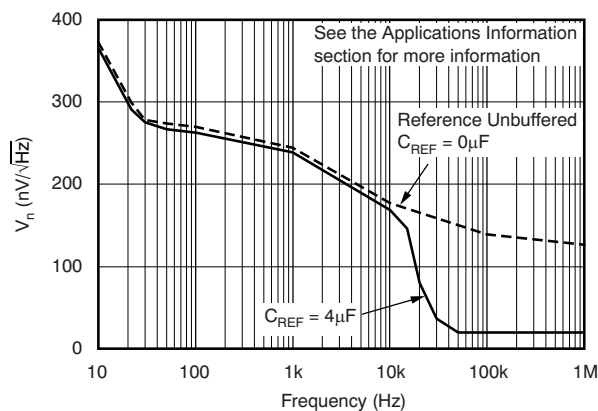
Figure 6.

(1) Explained in more detail in the [Application Information](#) section of this data sheet.

## TYPICAL CHARACTERISTICS: Internal Reference (continued)

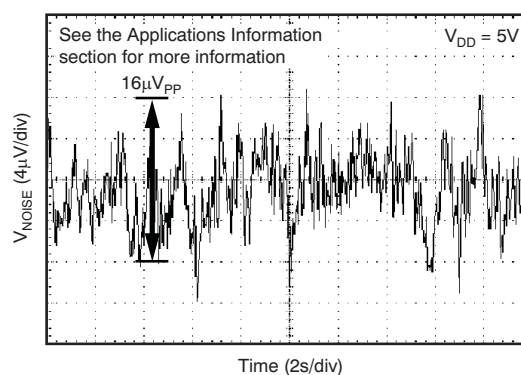
At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

**INTERNAL REFERENCE NOISE DENSITY  
vs FREQUENCY<sup>(2)</sup>**



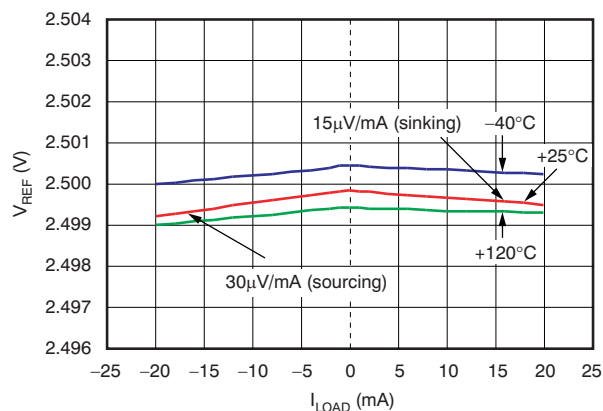
**Figure 7.**

**INTERNAL REFERENCE NOISE  
0.1Hz TO 10Hz<sup>(2)</sup>**



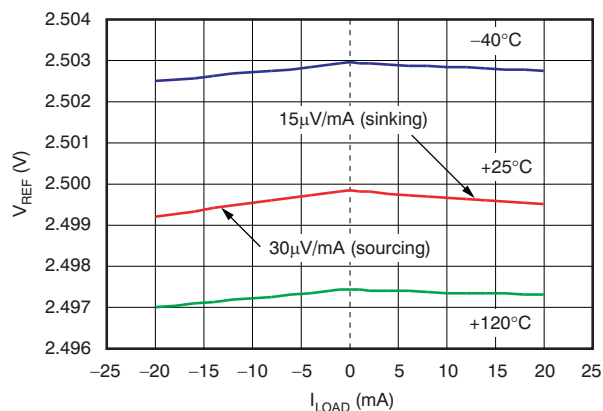
**Figure 8.**

**INTERNAL REFERENCE VOLTAGE  
vs LOAD CURRENT (Grades C and D)**



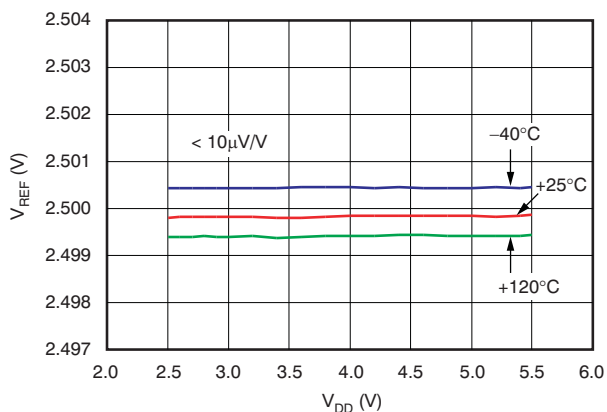
**Figure 9.**

**INTERNAL REFERENCE VOLTAGE  
vs LOAD CURRENT (Grades A and B)**



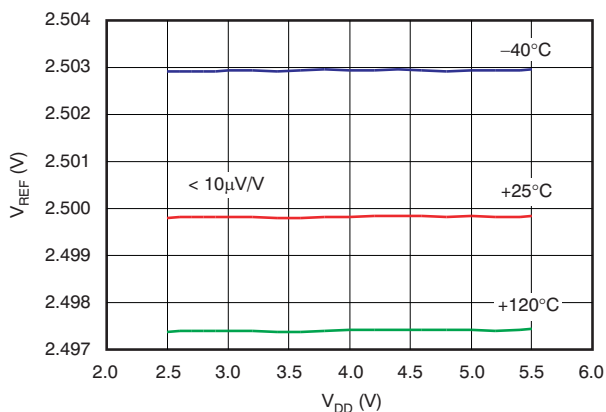
**Figure 10.**

**INTERNAL REFERENCE VOLTAGE  
vs SUPPLY VOLTAGE (Grades C and D)**



**Figure 11.**

**INTERNAL REFERENCE VOLTAGE  
vs SUPPLY VOLTAGE (Grades A and B)**



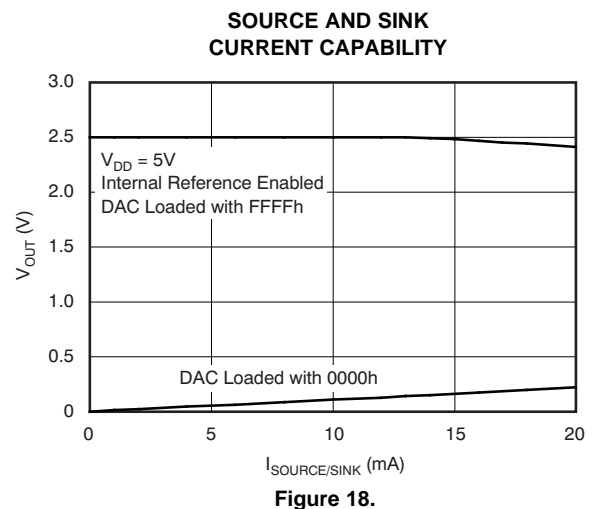
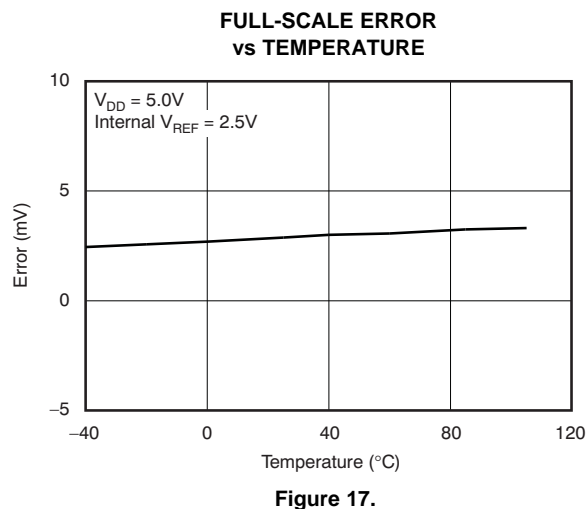
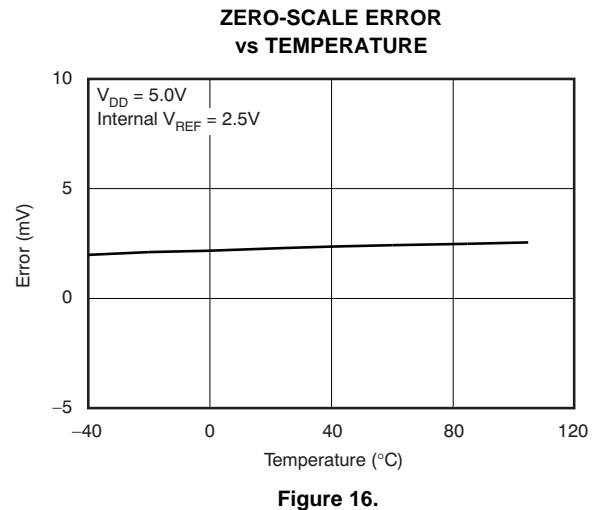
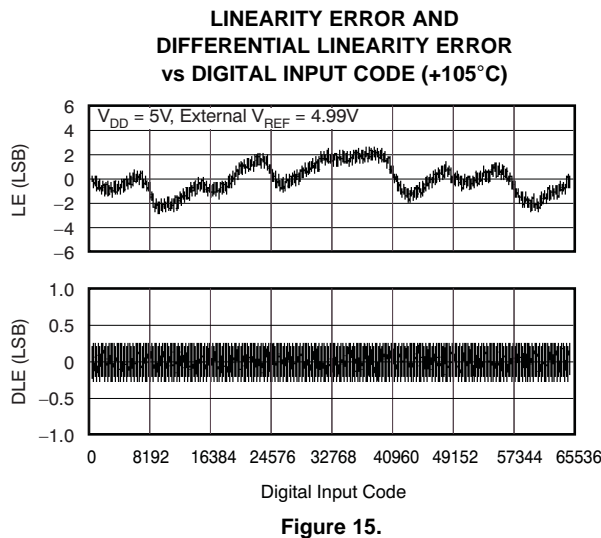
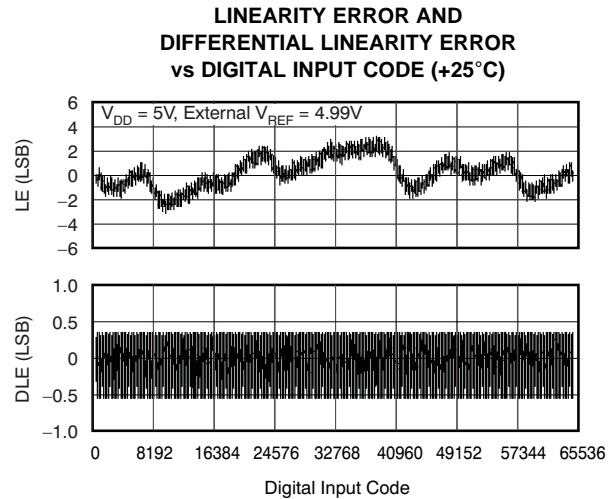
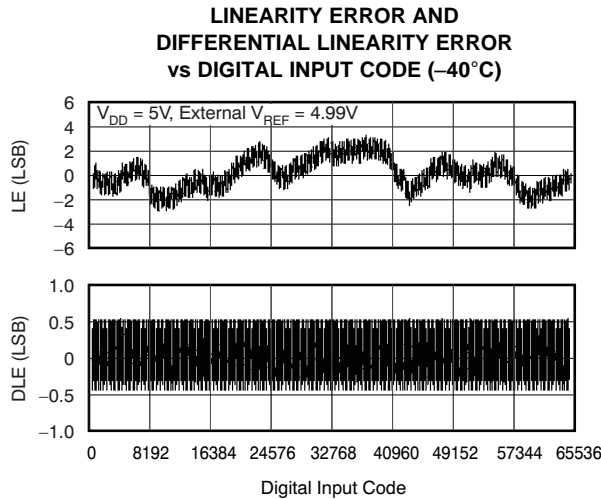
**Figure 12.**

(2) Explained in more detail in the [Application Information](#) section of this data sheet.



## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 5V$

At  $T_A = +25^\circ\text{C}$ , external reference used, and DAC output not loaded, unless otherwise noted.



## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 5V$ (continued)

At  $T_A = +25^\circ\text{C}$ , external reference used, and DAC output not loaded, unless otherwise noted.

**SOURCE AND SINK  
CURRENT CAPABILITY**

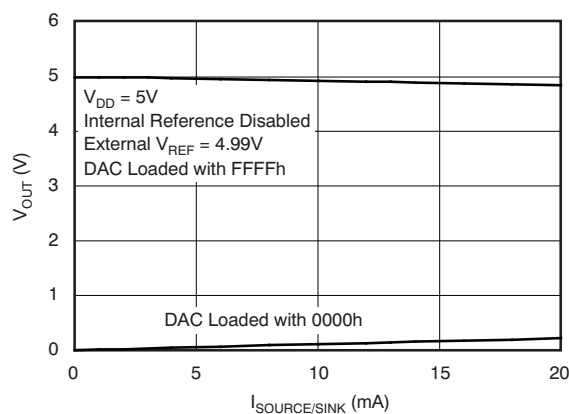


Figure 19.

**POWER-SUPPLY CURRENT  
vs DIGITAL INPUT CODE**

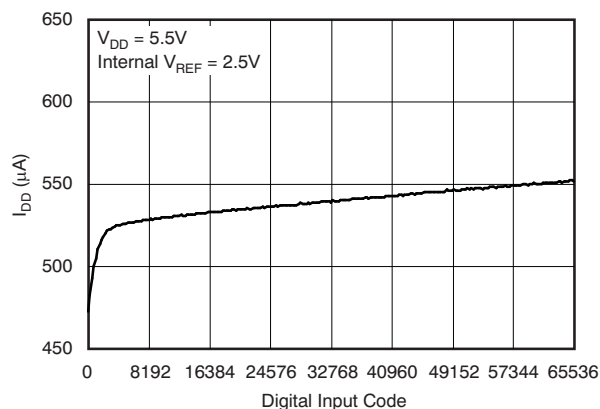


Figure 20.

**POWER-SUPPLY CURRENT  
vs TEMPERATURE**

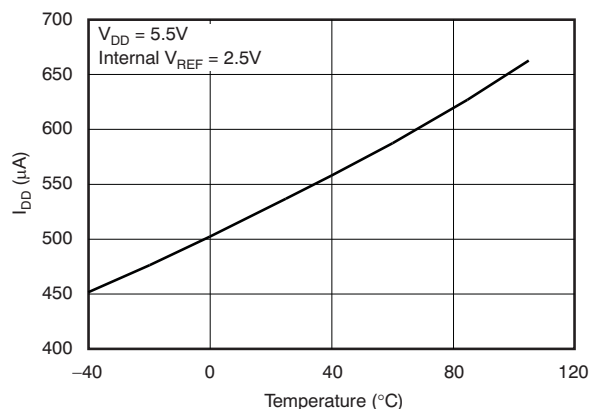


Figure 21.

**POWER-SUPPLY CURRENT  
vs POWER-SUPPLY VOLTAGE**

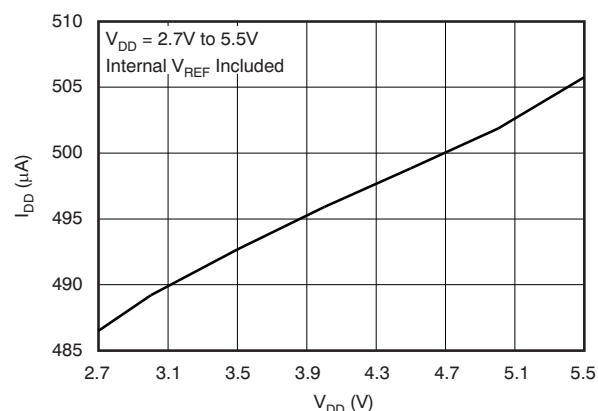


Figure 22.

**POWER-DOWN CURRENT  
vs POWER-SUPPLY VOLTAGE**

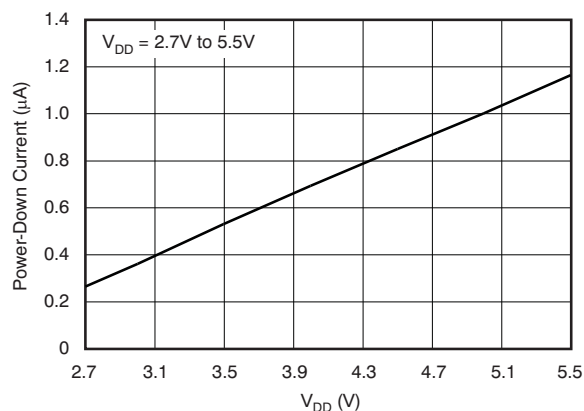


Figure 23.

**POWER-SUPPLY CURRENT  
vs LOGIC INPUT VOLTAGE**

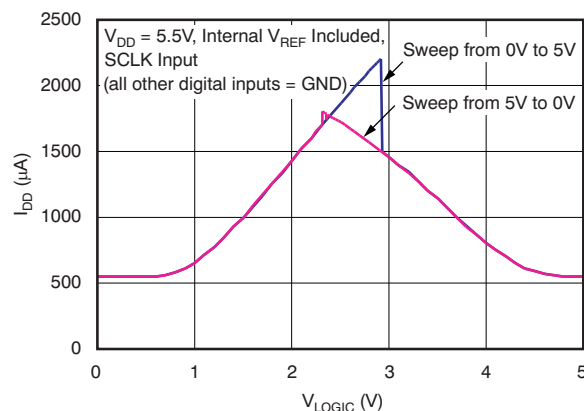


Figure 24.

## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 5V$ (continued)

At  $T_A = +25^\circ\text{C}$ , external reference used, and DAC output not loaded, unless otherwise noted.

**POWER-SUPPLY CURRENT  
HISTOGRAM**

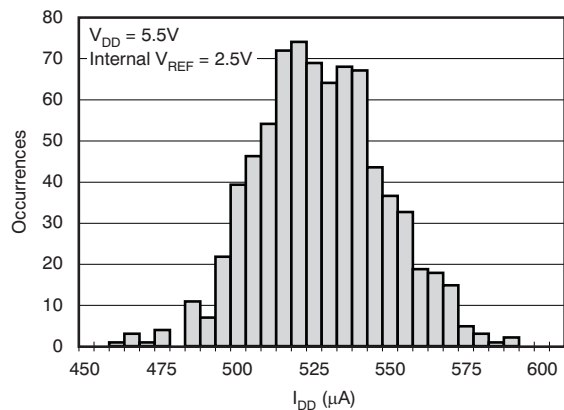


Figure 25.

**TOTAL HARMONIC DISTORTION  
vs OUTPUT FREQUENCY**

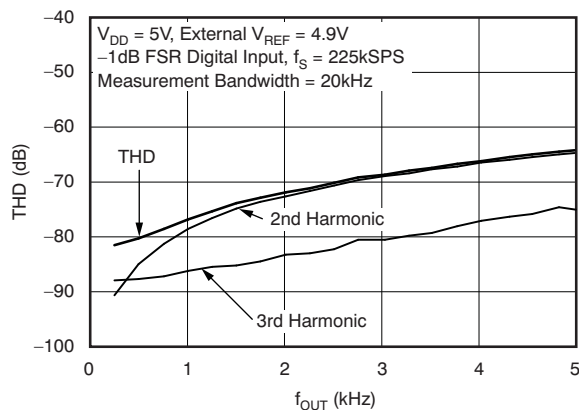
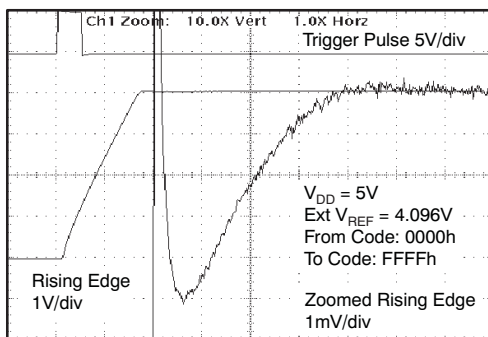


Figure 26.

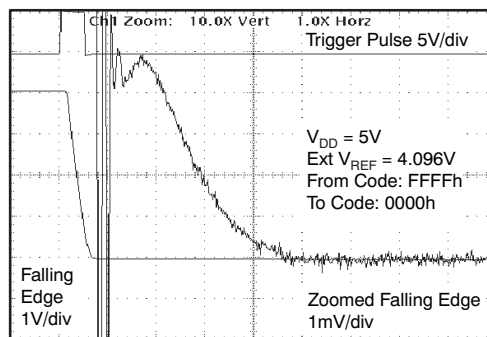
**FULL-SCALE SETTLING TIME:  
5V RISING EDGE**



Time (2µs/div)

Figure 27.

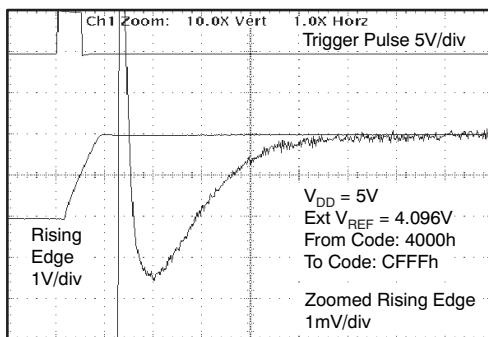
**FULL-SCALE SETTLING TIME:  
5V FALLING EDGE**



Time (2µs/div)

Figure 28.

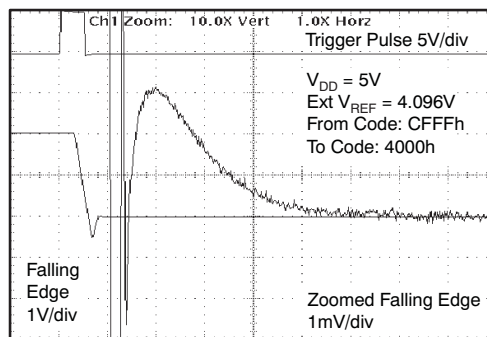
**HALF-SCALE SETTLING TIME:  
5V RISING EDGE**



Time (2µs/div)

Figure 29.

**HALF-SCALE SETTLING TIME:  
5V FALLING EDGE**



Time (2µs/div)

Figure 30.

## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 5V$ (continued)

At  $T_A = +25^\circ\text{C}$ , external reference used, and DAC output not loaded, unless otherwise noted.

**GLITCH ENERGY:  
5V, 1LSB STEP, RISING EDGE**

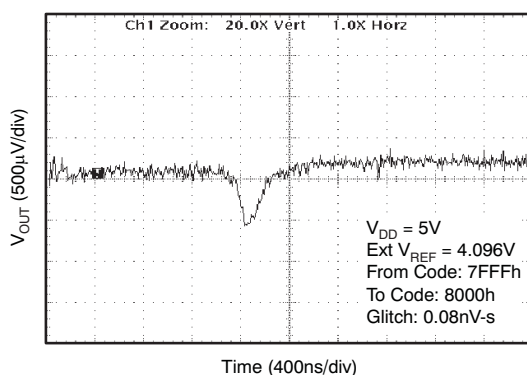


Figure 31.

**GLITCH ENERGY:  
5V, 1LSB STEP, FALLING EDGE**

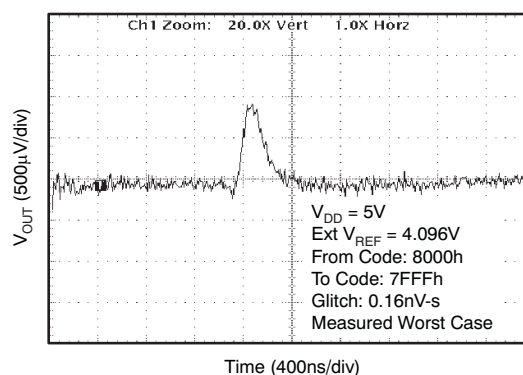


Figure 32.

**GLITCH ENERGY:  
5V, 16LSB STEP, RISING EDGE**

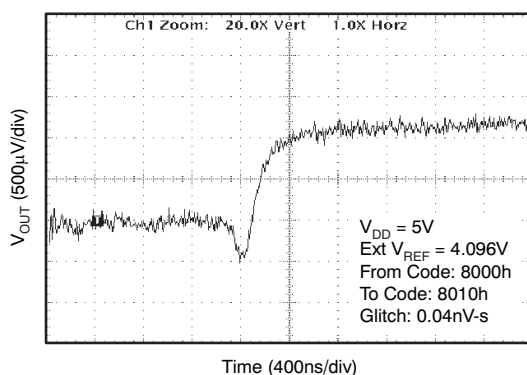


Figure 33.

**GLITCH ENERGY:  
5V, 16LSB STEP, FALLING EDGE**

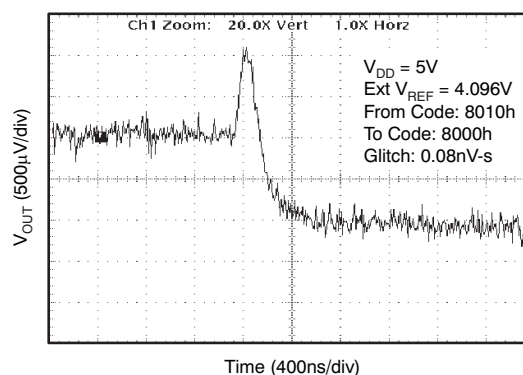


Figure 34.

**GLITCH ENERGY:  
5V, 256LSB STEP, RISING EDGE**

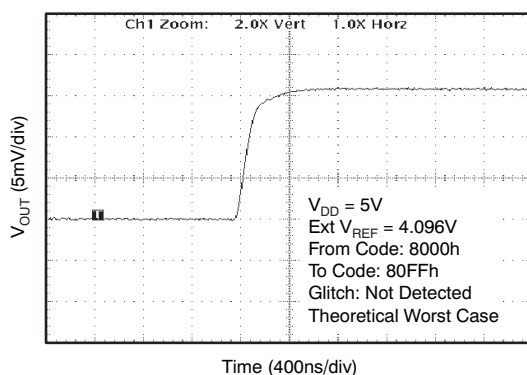


Figure 35.

**GLITCH ENERGY:  
5V, 256LSB STEP, FALLING EDGE**

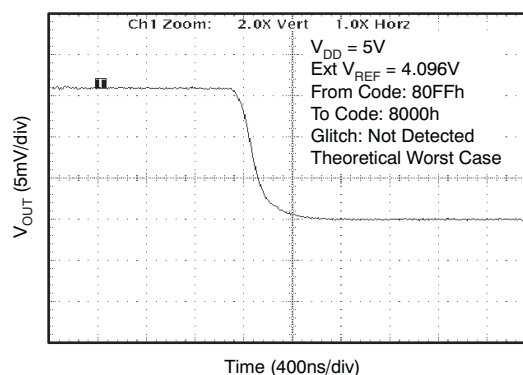


Figure 36.

## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 5V$ (continued)

At  $T_A = +25^\circ\text{C}$ , external reference used, and DAC output not loaded, unless otherwise noted.

### SIGNAL-TO-NOISE RATIO vs OUTPUT FREQUENCY

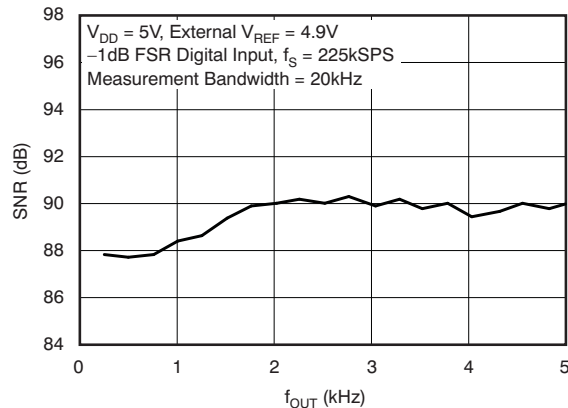


Figure 37.

### POWER SPECTRAL DENSITY

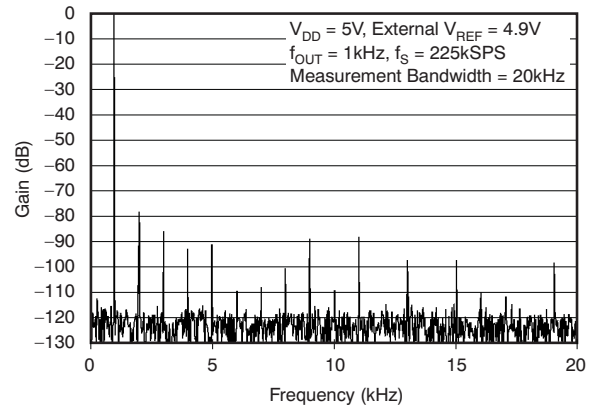


Figure 38.

### DAC OUTPUT NOISE DENSITY vs FREQUENCY<sup>(1)</sup>

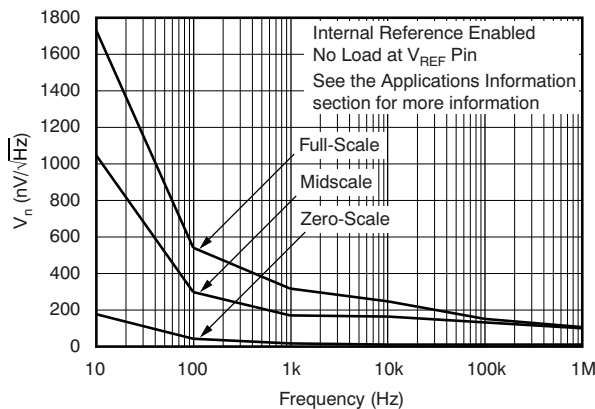


Figure 39.

### DAC OUTPUT NOISE DENSITY vs FREQUENCY<sup>(1)</sup>

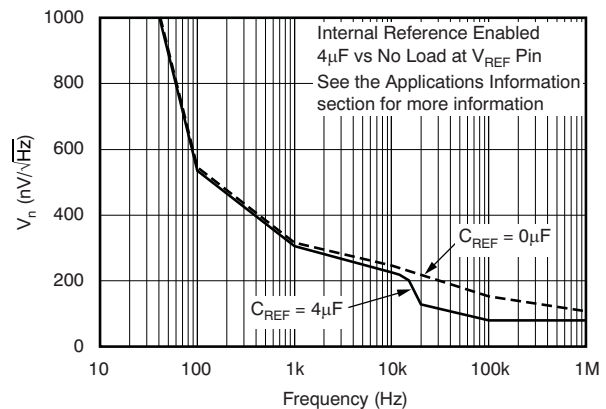


Figure 40.

### DAC OUTPUT NOISE 0.1Hz TO 10Hz

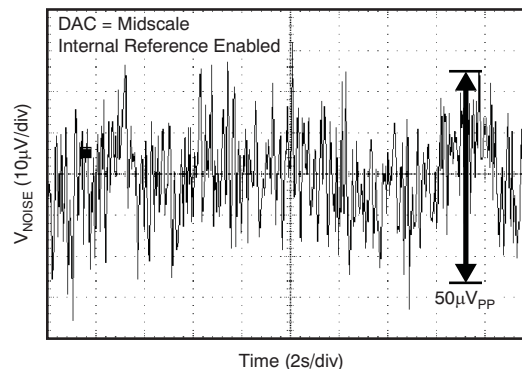


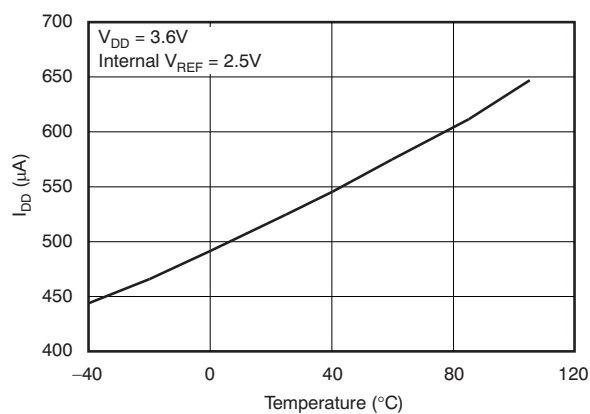
Figure 41.

(1) Explained in more detail in the [Application Information](#) section of this data sheet.

### TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 3.6V$

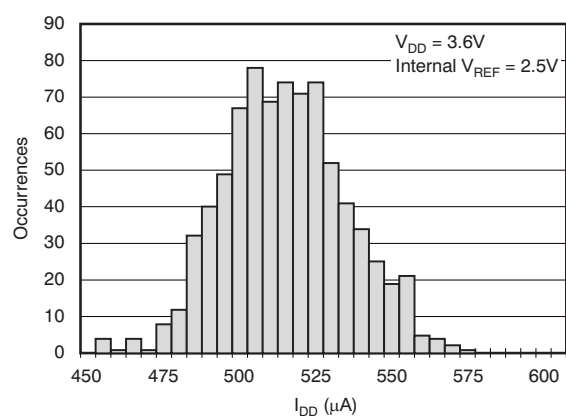
At  $T_A = +25^\circ\text{C}$ , internal reference used, and DAC output not loaded, unless otherwise noted

**POWER-SUPPLY CURRENT  
vs TEMPERATURE**



**Figure 42.**

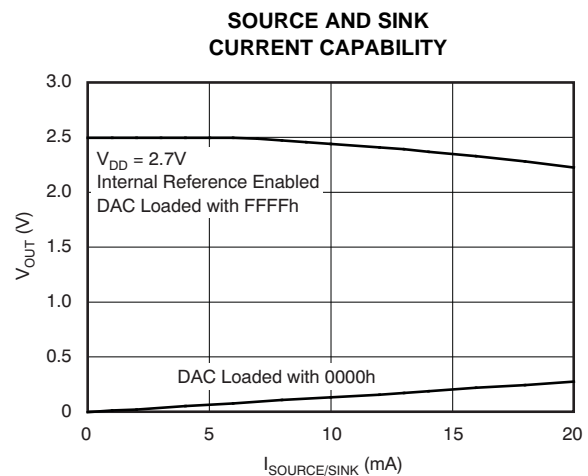
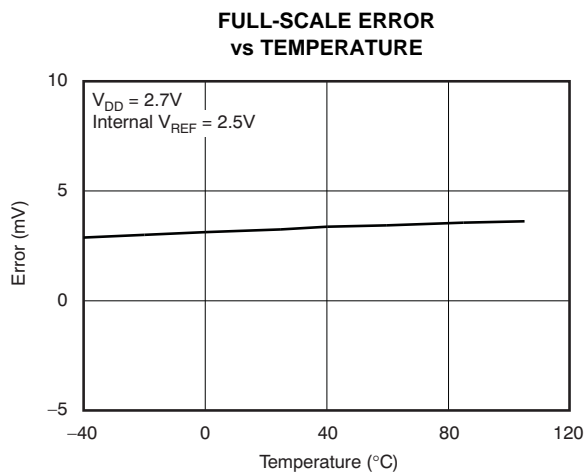
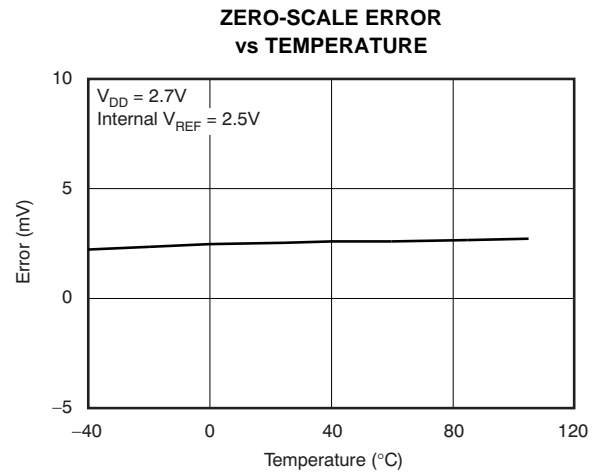
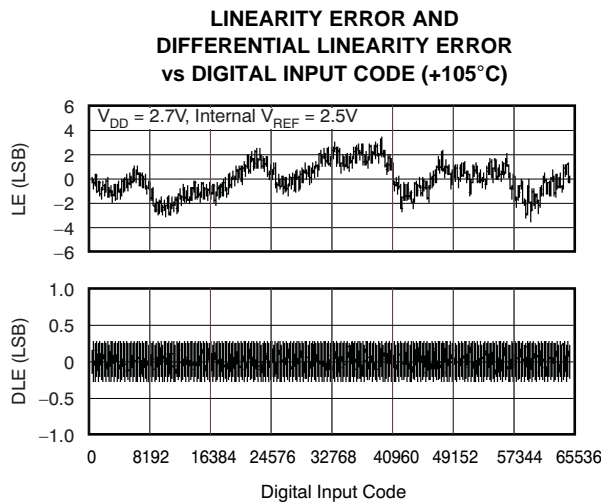
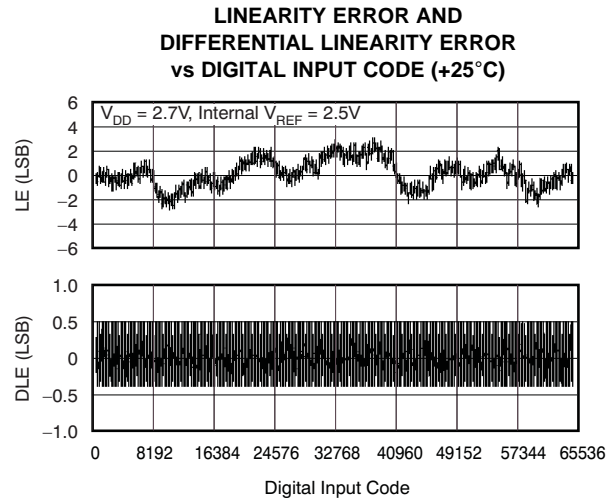
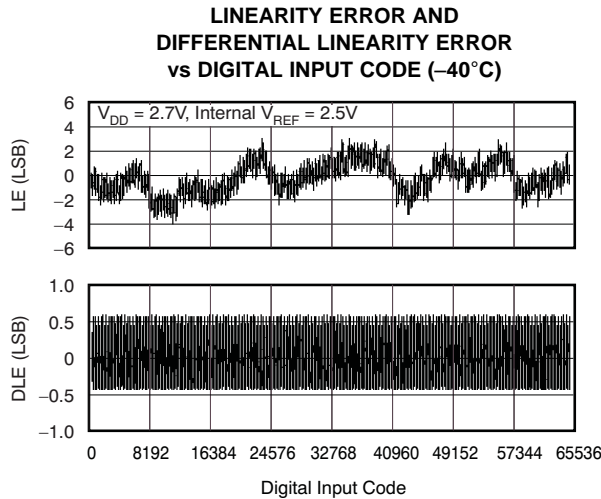
**POWER-SUPPLY CURRENT  
HISTOGRAM**



**Figure 43.**

## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 2.7V$

At  $T_A = +25^\circ C$ , internal reference used, and DAC output not loaded, unless otherwise noted



## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 2.7V$ (continued)

At  $T_A = +25^\circ C$ , internal reference used, and DAC output not loaded, unless otherwise noted

**SUPPLY CURRENT  
vs DIGITAL INPUT CODE**

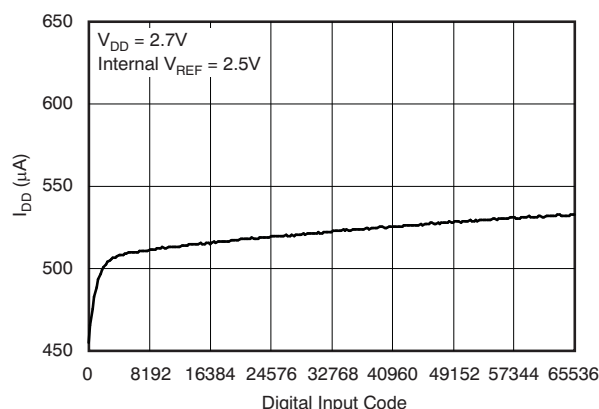


Figure 50.

**POWER-SUPPLY CURRENT  
vs LOGIC INPUT VOLTAGE**

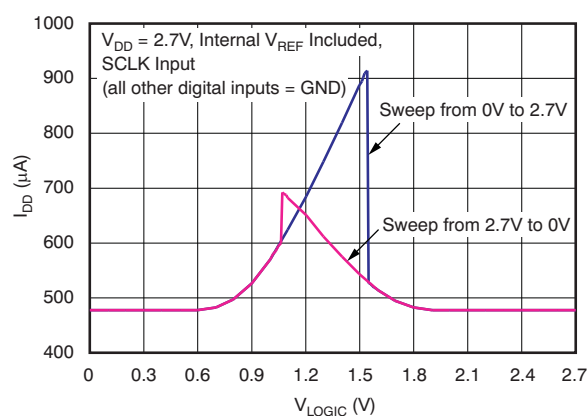
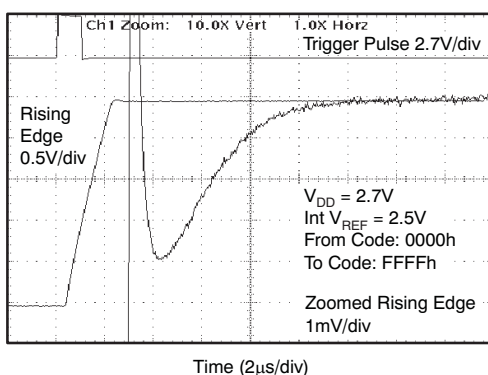


Figure 51.

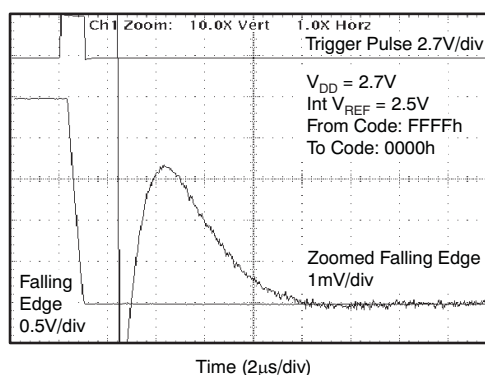
**FULL-SCALE SETTling TIME:  
2.7V RISING EDGE**



Time (2μs/div)

Figure 52.

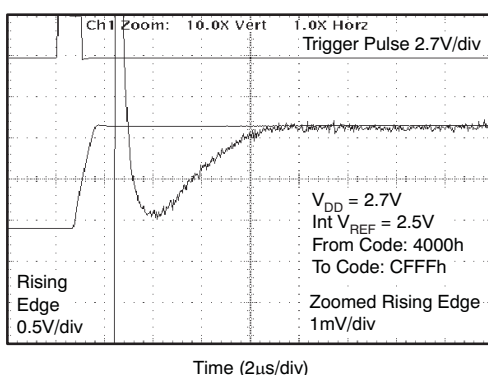
**FULL-SCALE SETTling TIME:  
2.7V FALLING EDGE**



Time (2μs/div)

Figure 53.

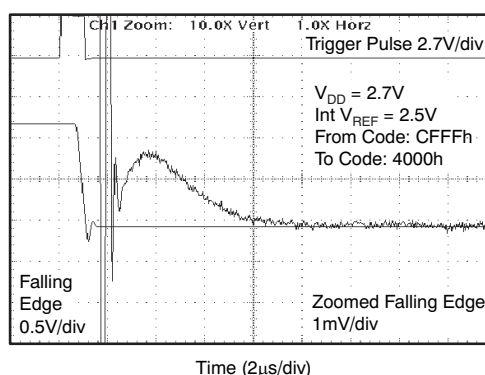
**HALF-SCALE SETTling TIME:  
2.7V RISING EDGE**



Time (2μs/div)

Figure 54.

**HALF-SCALE SETTling TIME:  
2.7V FALLING EDGE**



Time (2μs/div)

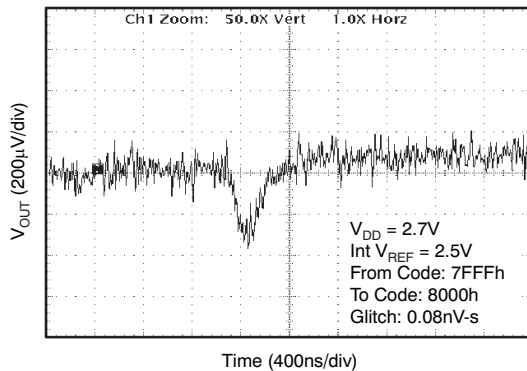
Figure 55.



## TYPICAL CHARACTERISTICS: DAC at $V_{DD} = 2.7V$ (continued)

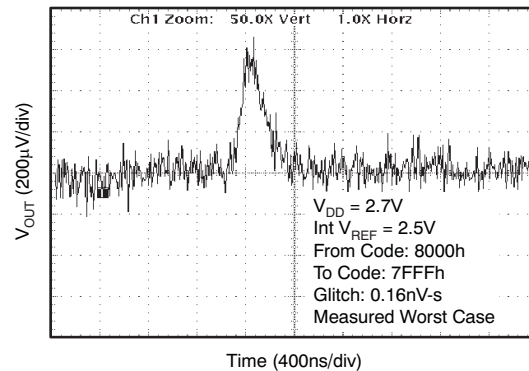
At  $T_A = +25^\circ C$ , internal reference used, and DAC output not loaded, unless otherwise noted

**GLITCH ENERGY:  
2.7V, 1LSB STEP, RISING EDGE**



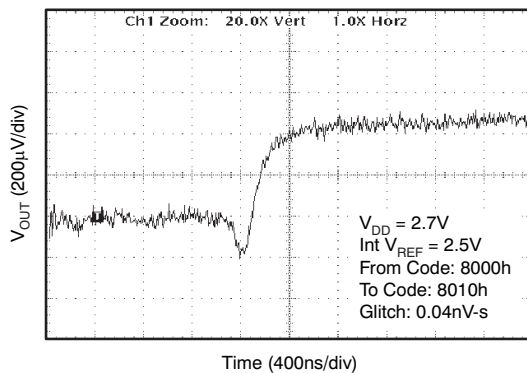
**Figure 56.**

**GLITCH ENERGY:  
2.7V, 1LSB STEP, FALLING EDGE**



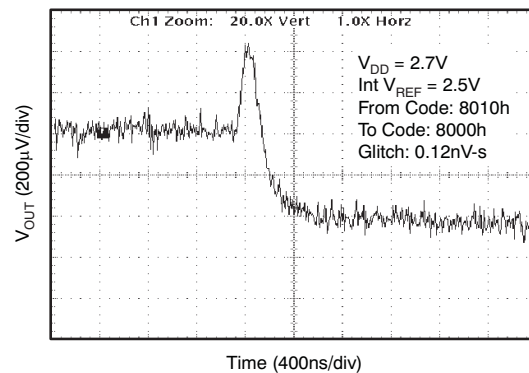
**Figure 57.**

**GLITCH ENERGY:  
2.7V, 16LSB STEP, RISING EDGE**



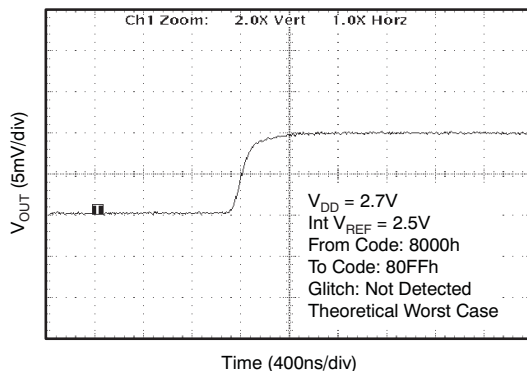
**Figure 58.**

**GLITCH ENERGY:  
2.7V, 16LSB STEP, FALLING EDGE**



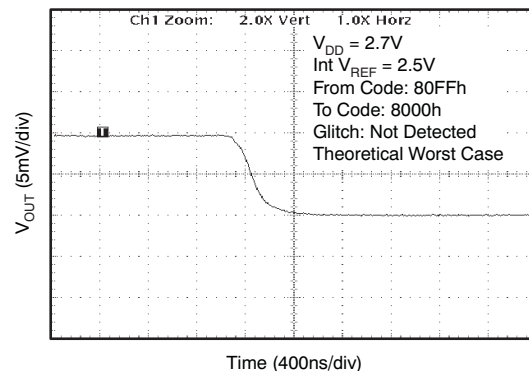
**Figure 59.**

**GLITCH ENERGY:  
2.7V, 256LSB STEP, RISING EDGE**



**Figure 60.**

**GLITCH ENERGY:  
2.7V, 256LSB STEP, FALLING EDGE**



**Figure 61.**

## THEORY OF OPERATION

### DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC8560 architecture consists of a string DAC followed by an output buffer amplifier. Figure 62 shows a block diagram of the DAC architecture.

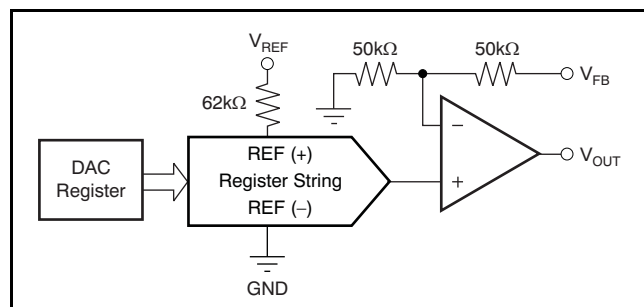


Figure 62. DAC8560 Architecture

The input coding to the DAC8560 is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = \frac{D_{IN}}{65536} \times V_{REF} \quad (1)$$

where  $D_{IN}$  = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

### RESISTOR STRING

The resistor string section is shown in Figure 63. It is simply a string of resistors, each of value  $R$ . The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors.

### OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0V to  $V_{DD}$ . It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics. The slew rate is 1.8V/μs with a full-scale settling time of 8μs with the output unloaded.

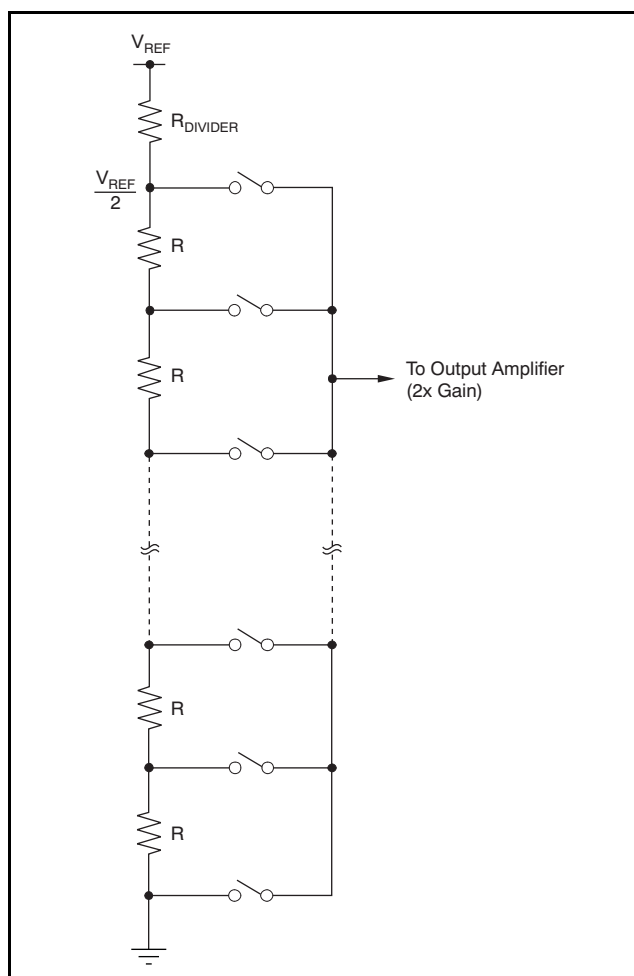


Figure 63. Resistor String

The inverting input of the output amplifier is available at the  $V_{FB}$  pin. This feature allows better accuracy in critical applications by tying the  $V_{FB}$  point and the amplifier output together directly at the load. Other signal conditioning circuitry may also be connected between these points for specific applications.

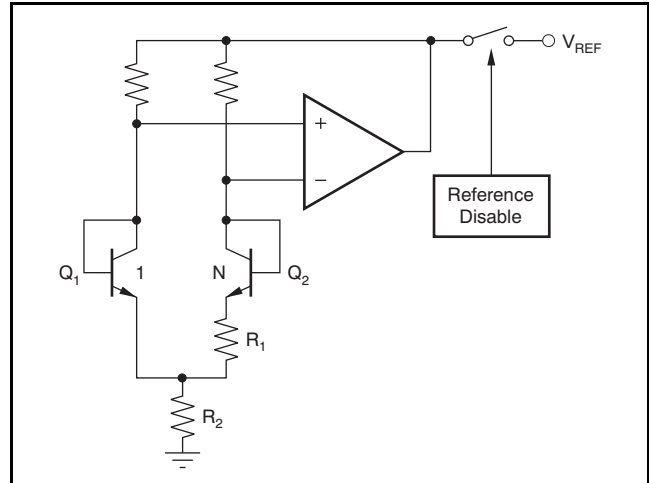
## INTERNAL REFERENCE

The DAC8560 includes a 2.5V internal reference that is enabled by default. The internal reference is externally available at the  $V_{REF}$  pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC8560 is a bipolar transistor-based, precision bandgap voltage reference. The basic bandgap topology is shown in [Figure 64](#). Transistors  $Q_1$  and  $Q_2$  are biased such that the current density of  $Q_1$  is greater than that of  $Q_2$ . The difference of the two base-emitter voltages ( $V_{BE1} - V_{BE2}$ ) has a positive temperature coefficient and is forced across resistor  $R_1$ . This voltage is gained up and added to the base-emitter voltage of  $Q_2$ , which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

## Enable/Disable Internal Reference

The DAC8560 internal reference is enabled by default; however, the reference can be disabled for debugging or evaluation purposes. A serial command requiring at least two additional SCLK cycles at the end of the 24-bit write sequence (see [Serial Interface](#) section) must be used to disable the internal reference. For proper operation, a total of at least 26 SCLK cycles are required for each enable/disable internal reference update sequence, during which SYNC must be held low. To disable the internal reference, execute the write sequence illustrated in [Table 1](#) followed by at least two additional SCLK falling edges while SYNC is low.



**Figure 64. Simplified Schematic of the Bandgap Reference**

To then enable the reference, either perform a power-cycle to reset the device, or sequentially execute the two write sequences in [Table 2](#) and [Table 3](#). Each of these write sequences must be followed by at least two additional SCLK falling edges while  $\overline{\text{SYNC}}$  remains low.

During the time that the internal reference is disabled, the DAC will function normally using an external reference. At this point, the internal reference is disconnected from the  $V_{REF}$  pin (tri-state). Do not attempt to drive the  $V_{REF}$  pin externally and internally at the same time indefinitely.

### Table 1. Write Sequence for Disabling the DAC8560 Internal Reference

[illegible]

### Table 2. Enabling the DAC8560 Internal Reference (Write Sequence 1 of 2)

[illegible]

### Table 3. Enabling the DAC8560 Internal Reference (Write Sequence 2 of 2)

[illegible]

**SERIAL INTERFACE**

The DAC8560 has a 3-wire serial interface (  $\overline{\text{SYNC}}$ , SCLK, and  $\text{D}_{\text{IN}}$  ) that is compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram for an example of a typical write sequence.

The write sequence begins by bringing the  $\overline{\text{SYNC}}$  line LOW. Data from the  $\text{D}_{\text{IN}}$  line is clocked into the 24-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 30MHz, making the DAC8560 compatible with high-speed DSPs. On the 24th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed.

At this point, the  $\overline{\text{SYNC}}$  line may be kept LOW or brought HIGH. In either case, it must be brought HIGH for a minimum of 33ns before the next write sequence so that a falling edge of  $\overline{\text{SYNC}}$  can initiate the next write sequence. As previously mentioned, it must be brought HIGH again before the next write sequence.

**INPUT SHIFT REGISTER**

The input shift register is 24 bits wide, as shown in [Table 4](#). The first six bits must be '000000'. The next two bits (PD1 and PD0) are control bits that set the desired mode of operation (normal mode or any one of three power-down modes) as indicated in [Table 5](#).

A more complete description of the various modes is located in the [Power-Down Modes](#) section. The next 16 bits are the data bits, which are transferred to the DAC register on the 24th falling edge of SCLK under normal operation (see [Table 5](#)).

**$\overline{\text{SYNC}}$  INTERRUPT**

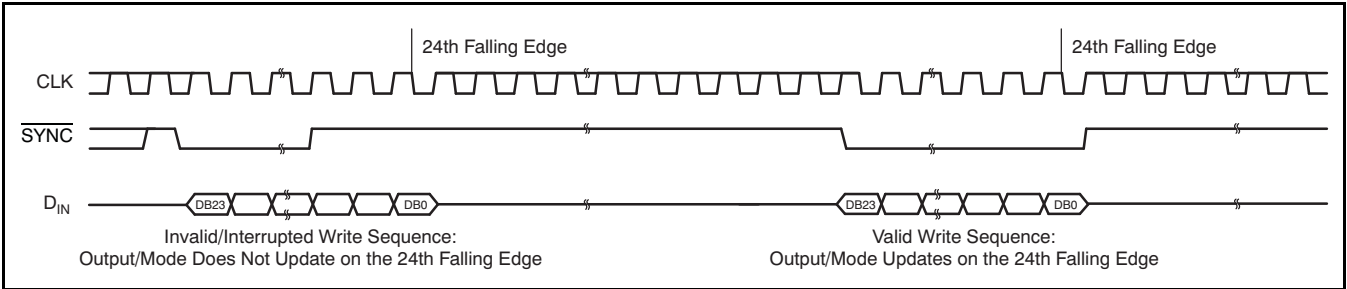
In a normal write sequence, the  $\overline{\text{SYNC}}$  line is kept LOW for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if  $\overline{\text{SYNC}}$  is brought HIGH before the 24th falling edge, it acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents, nor a change in the operating mode occurs, as shown in [Figure 65](#).

**POWER-ON RESET**

The DAC8560 contains a power-on-reset circuit that controls the output voltage during power up. On power up, all registers are filled with zeros and the output voltage is zero-scale; it remains there until a valid write sequence is made to the DAC. This feature is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

**Table 4. DAC8560 Data Input Register Format**

DB23										DB0													
0	0	0	0	0	0	PD 1	PD 0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0



**Figure 65.  $\overline{\text{SYNC}}$  Interrupt Facility**

## POWER-DOWN MODES

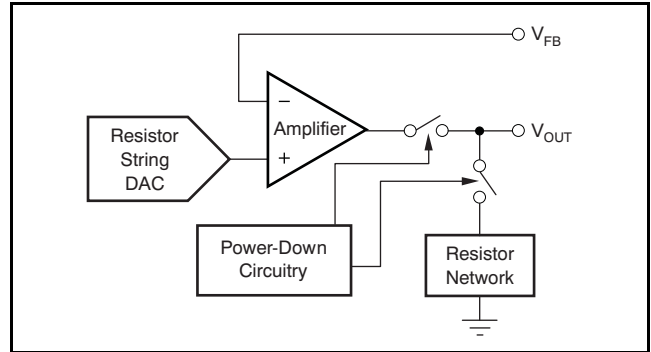
The DAC8560 supports four separate modes of operation. These modes are programmable by setting two bits (PD1 and PD0) in the control register. Table 5 shows how to control the operating mode with data bits PD1 (DB17) and PD0 (DB16).

**Table 5. Operating Modes**

PD1 (DB17)	PD0 (DB16)	OPERATING MODE
0	0	Normal operation
0	1	Power-down 1 kΩ to GND
1	0	Power-down 100 kΩ to GND
1	1	Power-down High-Z

When both bits are set to '0', the device works normally with its typical current consumption of 530μA at 5.5V. However, for the three power-down modes, the supply current falls to 1.2μA at 5.5V (0.7μA at 3.6V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As shown in Table 5, there are three different power-down options.  $V_{OUT}$  can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open circuited (High-Z). The output stage is illustrated in Figure 66.



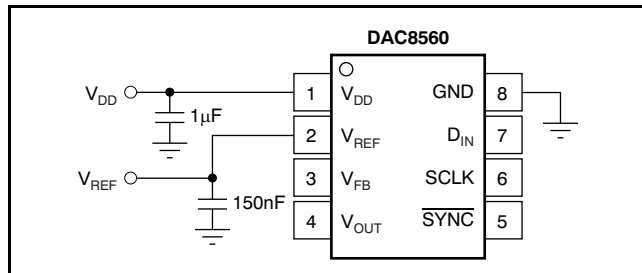
**Figure 66. Output Stage During Power Down**

All analog circuitry is shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power down. The time to exit power-down is typically 2.5μs for  $V_{DD} = 5V$ , and 5μs for  $V_{DD} = 3V$ . See the Typical Characteristics for more information.

## APPLICATION INFORMATION

### INTERNAL REFERENCE

The DAC8560 internal reference does not require an external load capacitor for stability because it is stable with any capacitive load. However, for improved noise performance, an external load capacitor of 150nF or larger connected to the  $V_{REF}$  output is recommended. Figure 67 shows the typical connections required for operation of the DAC8560 internal reference. A supply bypass capacitor at the  $V_{DD}$  input is also recommended.



**Figure 67. Typical Connections for Operating the DAC8560 Internal Reference**

### Supply Voltage

The DAC8560 internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the [Load Regulation](#) section. The stability of the DAC8560 internal reference with variations in supply voltage (line regulation, DC PSRR) is also exceptional. Within the specified supply voltage range of 2.7V to 5.5V, the variation at  $V_{REF}$  is smaller than 10µV/V; see the [Typical Characteristics](#).

### Temperature Drift

The DAC8560 internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the *box* method, which is described by [Equation 2](#):

$$\text{Drift Error} = \left( \frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^6 \text{ (ppm/}^\circ\text{C)} \quad (2)$$

Where:

$V_{REF\_MAX}$  = maximum reference voltage observed within temperature range  $T_{RANGE}$ .

$V_{REF\_MIN}$  = minimum reference voltage observed within temperature range  $T_{RANGE}$ .

$V_{REF}$  = 2.5V, target value for reference output voltage.

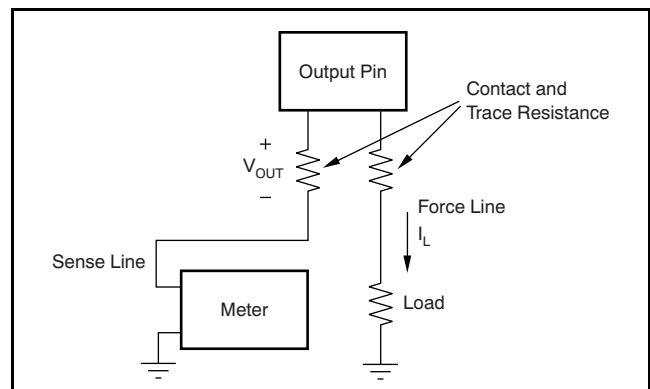
The DAC8560 internal reference (grades C and D) features an exceptional typical drift coefficient of 2ppm/°C from –40°C to +120°C. Characterizing a large number of units, a maximum drift coefficient of 5ppm/°C (grades C and D) is observed. Temperature drift results are summarized in the [Typical Characteristics](#).

### Noise Performance

Typical 0.1Hz to 10Hz voltage noise can be seen in [Figure 8, Internal Reference Noise](#). Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the AC performance. The output noise spectrum at  $V_{REF}$  without any external components is depicted in [Figure 7, Internal Reference Noise Density vs Frequency](#). Another noise density spectrum is also shown in [Figure 7](#), which was obtained using a 4µF load capacitor at  $V_{REF}$  for noise filtering. Internal reference noise impacts the DAC output noise; see the [DAC Noise Performance](#) section for more details.

### Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the DAC8560 internal reference is measured using force and sense contacts as pictured in [Figure 68](#). The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the DAC8560 internal reference. Measurement results are summarized in the [Typical Characteristics](#). Force and sense lines should be used for applications requiring improved load regulation.



**Figure 68. Accurate Load Regulation of the DAC8560 Internal Reference**

## Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses, as shown in Figure 6, the typical long-term stability curve. The typical drift value for the DAC8560 internal reference is 50ppm from 0 hours to 1900 hours. This parameter is characterized by powering-up and measuring 20 units at regular intervals for a period of 1900 hours.

## Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at +25°C, cycling the device through the specified temperature range, and returning to +25°C. It is expressed in Equation 3:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{REF\_PRE}} - V_{\text{REF\_POST}}|}{V_{\text{REF\_NOM}}} \right) \times 10^6 \text{ (ppm)} \quad (3)$$

Where:

$V_{\text{HYST}}$  = thermal hysteresis.

$V_{\text{REF\_PRE}}$  = output voltage measured at +25°C pre-temperature cycling.

$V_{\text{REF\_POST}}$  = output voltage measured after the device has been cycled through the temperature range of –40°C to +120°C, and returned to +25°C.

## DAC NOISE PERFORMANCE

Typical noise performance for the DAC8560 with the internal reference enabled is shown in Figure 39 to Figure 41. Output noise spectral density at pin  $V_{\text{OUT}}$  versus frequency is depicted in Figure 39 for full-scale, midscale, and zero scale input codes. The typical noise density for midscale code is 170nV/√Hz at 1kHz and 100nV/√Hz at 1MHz. High-frequency noise can be improved by filtering the reference noise as shown in Figure 40, where a 4μF load capacitor is connected to the  $V_{\text{REF}}$  pin and compared to the no-load condition. Integrated output noise between 0.1Hz and 10Hz is close to 50μV<sub>pp</sub> (midscale), as shown in Figure 41.

## BIPOLAR OPERATION USING THE DAC8560

The DAC8560 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in either Figure 69 or Figure 70. The circuit shown gives an output voltage range of ± $V_{\text{REF}}$ . Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

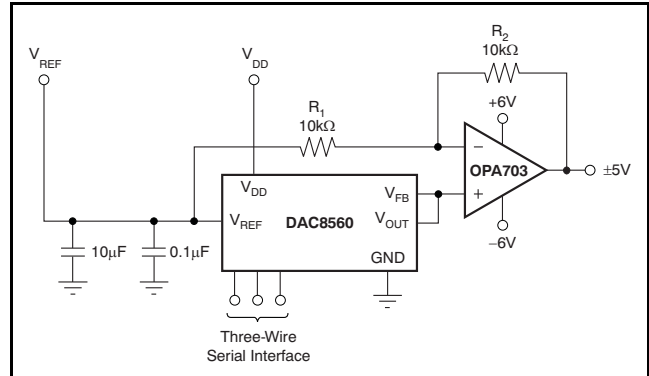


Figure 69. Bipolar Output Range Using External Reference at 5V

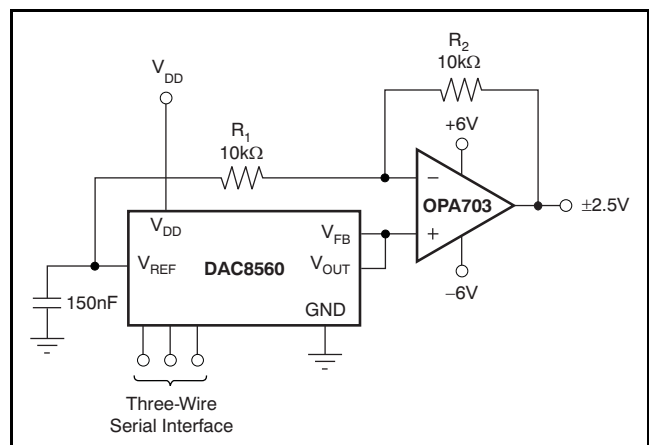


Figure 70. Bipolar Output Range Using Internal Reference

The output voltage for any input code can be calculated as using Equation 4:

$$V_o = \left[ V_{\text{REF}} \times \left( \frac{D}{65536} \right) \times \left( \frac{R_1 + R_2}{R_1} \right) - V_{\text{REF}} \times \left( \frac{R_2}{R_1} \right) \right] \quad (4)$$

where D represents the input code in decimal (0–65535).

With  $V_{\text{REF}} = 5\text{V}$ ,  $R_1 = R_2 = 10\text{k}\Omega$ .

$$V_o = \left( \frac{10 \times D}{65536} \right) - 5\text{V} \quad (5)$$

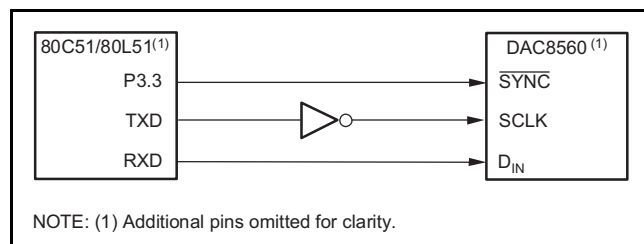
This result has an output voltage range of ±5V with 0000h corresponding to a –5V output and FFFFh corresponding to a 5V output, as shown in Figure 69. Similarly, using the internal reference, a ±2.5V output voltage range can be achieved, as shown in Figure 70.



## MICROPROCESSOR INTERFACING

### DAC8560 TO 8051 Interface

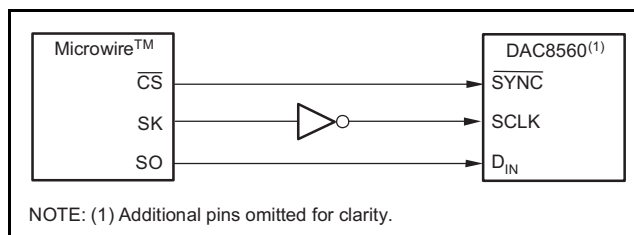
See [Figure 71](#) for a serial interface between the DAC8560 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC8560, while RXD drives the serial data line of the device. The  $\overline{\text{SYNC}}$  signal is derived from a bit-programmable pin on the port of the 8051. In this case, port line P3.3 is used. When data is to be transmitted to the DAC8560, P3.3 is taken LOW. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left LOW after the first eight bits are transmitted, then a second write cycle is initiated to transmit the second byte of data. P3.3 is taken HIGH following the completion of the third write cycle. The 8051 outputs the serial data in a format which has the LSB first. The DAC8560 requires its data with the MSB as the first bit received. The 8051 transmit routine must therefore take this into account, and *mirror* the data as needed.



**Figure 71. DAC8560 to 80C51/80L51 Interface**

### DAC8560 to Microwire Interface

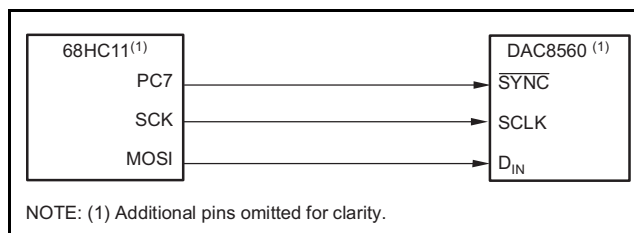
[Figure 72](#) shows an interface between the DAC8560 and any Microwire compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the DAC8560 on the rising edge of the SK signal.



**Figure 72. DAC8560 to Microwire Interface**

### DAC8560 to 68HC11 Interface

[Figure 73](#) shows a serial interface between the DAC8560 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC8560, while the MOSI output drives the serial data line of the DAC. The  $\overline{\text{SYNC}}$  signal is derived from a port line (PC7), similar to the 8051 diagram.



**Figure 73. DAC8560 to 68HC11 Interface**

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data is being transmitted to the DAC, the  $\overline{\text{SYNC}}$  line is held LOW (PC7). Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data is transmitted MSB first.) In order to load data to the DAC8560, PC7 is left LOW after the first eight bits are transferred, then a second and third serial write operation is performed to the DAC. PC7 is taken HIGH at the end of this procedure.



## LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC8560 offers single-supply operation, and it often is used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

As a result of the single ground pin of the DAC8560, all return currents, including digital and analog return currents for the DAC, must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to  $V_{DD}$  should be well regulated and low noise. Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection,  $V_{DD}$  should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor and 0.1 $\mu$ F bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100 $\mu$ F electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors – all designed to essentially low-pass filter the supply, removing the high-frequency noise.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2006) to Revision A	Page
• Changed Output Voltage parameter min/max values from 2.4995 and 2.5005 to 2.4975 and 2.5025, respectively .....	4
• Changed Initial Accuracy parameter min/max values from –0.02 and 0.02 to –0.1 and 0.1, respectively .....	4
<hr/>	
Changes from Revision A (May 2011) to Revision B	Page
• Changed Revision date from A, May 2011 to B, November 2011 .....	1
• Changed "Zero-code error drift" in the ELEC CHARA table, TYP from $\pm 20$ to $\pm 4$ .....	3

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8560IADGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IADGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IADGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IADGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IBDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IBDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IBDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560ICDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560ICDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560ICDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IDDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IDDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>
DAC8560IDDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	D860	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8560IADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560IADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560IBDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560IBDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560ICDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560ICDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560IDDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC8560IDDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8560IADGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC8560IADGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8560IBDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC8560IBDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8560ICDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC8560ICDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
DAC8560IDDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
DAC8560IDDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0

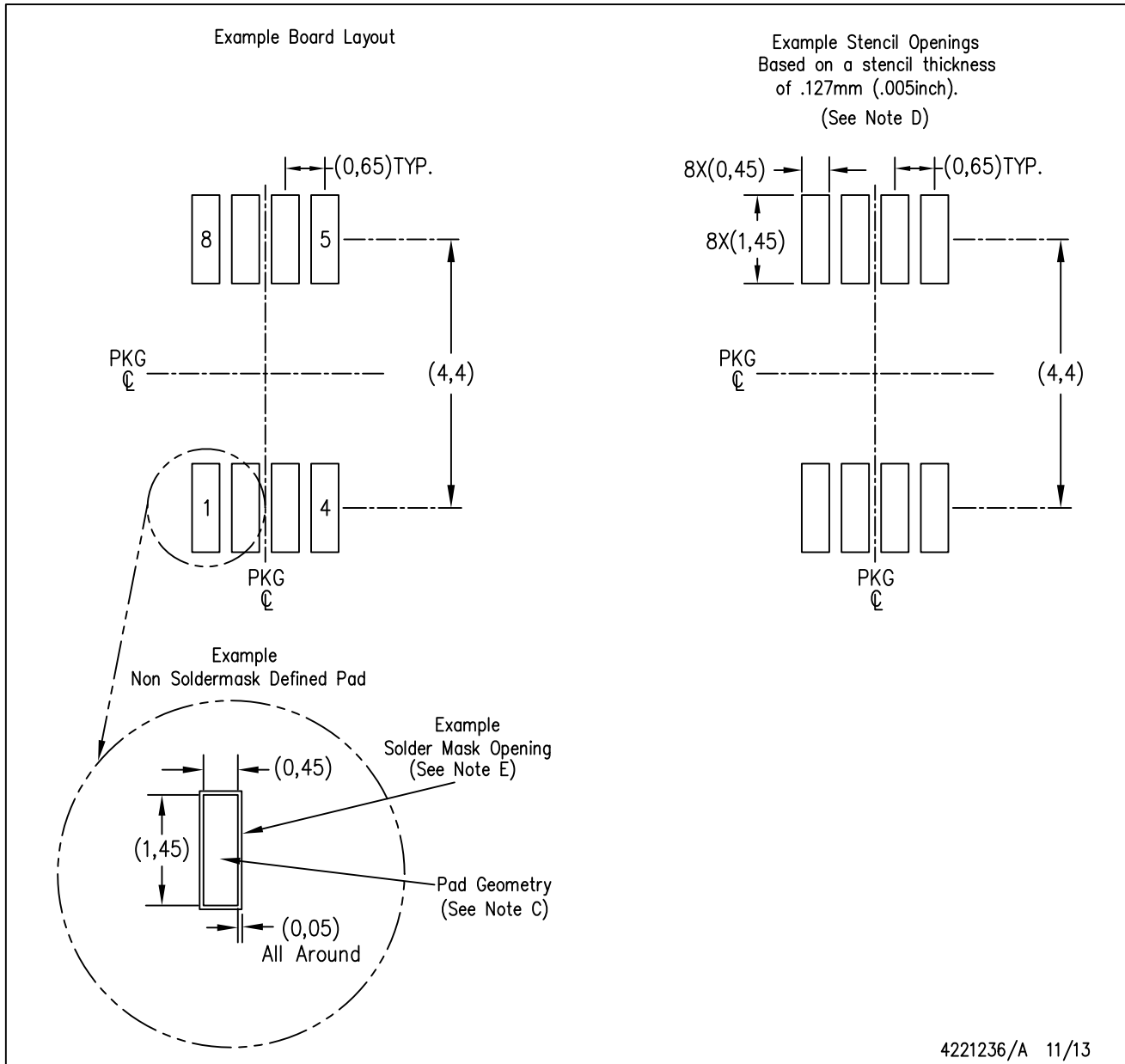
DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
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  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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