Precision, Low-Noise, Rail-to-Rail Output, 36-V, Zero-Drift Operational Amplifiers

Check for Samples: OPA188

FEATURES

- **Low Offset Voltage: 25 µV (max)**
- **Zero-Drift: 0.03 µV/°C**
- **Low Noise: 8.8 nV/√Hz**
  - **0.1-Hz to 10-Hz Noise: 0.25 μV_{PP}**
- **Excellent DC Precision:**
  - **PSRR: 142 dB**
  - **CMRR: 146 dB**
  - **Open-Loop Gain: 136 dB**
- **Gain Bandwidth: 2 MHz**
- **Quiescent Current: 510 µA (max)**
- **Wide Supply Range: ±2 V to ±18 V**
- **Rail-to-Rail Output**
- **Input Includes Negative Rail**
- **RFI Filtered Inputs**
- ***Micro*SIZE Packages**

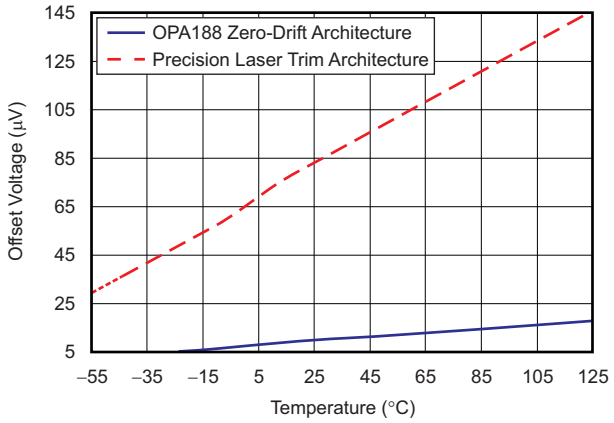
APPLICATIONS

- **Bridge Amplifiers**
- **Strain Gauges**
- **Transducer Applications**
- **Temperature Measurement**
- **Electronic Scales**
- **Medical Instrumentation**
- **Resistance Temperature Detectors**

DESCRIPTION

The OPA188 operational amplifier uses TI proprietary auto-zeroing techniques to provide low offset voltage (25 µV, max), and near zero-drift over time and temperature. This miniature, high-precision, low-quiescent current amplifier offers high input impedance and rail-to-rail output swing within 15 mV of the rails. The input common-mode range includes the negative rail. Either single or dual supplies can be used in the range of +4 V to +36 V (±2 V to ±18 V).

The single version is available in the *Micro*SIZE SOT23-5, MSOP-8, and SO-8 packages. All versions are specified for operation from –40°C to +125°C.



Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (µV, max)	OFFSET VOLTAGE DRIFT (µV/°C, max)	BANDWIDTH (MHz)	INPUT VOLTAGE NOISE (μV_{PP}, f = 0.1 Hz to 10 Hz)
Single	OPA188 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA333 (5 V)	±10	±0.05	0.35	1.1
	OPA378 (5 V)	±50	±0.25	0.9	0.4
	OPA735 (12 V)	±5	±0.05	1.6	2.5
Dual	OPA2188 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA2333 (5 V)	±10	±0.05	0.35	1.1
	OPA2378 (5 V)	±50	±0.25	0.9	0.4
	OPA2735 (12 V)	±5	±0.05	1.6	2.5
Quad	OPA4188 (4 V to 36 V)	±25	±0.085	2	0.25
	OPA4330 (5 V)	±50	±0.25	0.35	1.1

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE
OPA188	SOT23-5	DBV	–40°C to +125°C
	SO-8	D	–40°C to +125°C
	MSOP-8	DGK	–40°C to +125°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Supply voltage		±20, 40 (single supply)	V
Signal input terminals(2)	Voltage	(V–) – 0.5 to (V+) + 0.5	V
	Current	±10	mA
	Differential	±0.7	V
Output short-circuit(3)		Continuous	
Temperature range	Operating(4), T_A	–55 to +150	°C
	Storage, T_{stg}	–65 to +150	°C
	Junction, T_J	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	1.5	kV
	Charged device model (CDM)	1	kV

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, V-, or V+.
(4) Provided device does not exceed maximum junction temperature (T_J) at any time.

ELECTRICAL CHARACTERISTICS: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = +8 V to +36 V)

At T_A = +25°C, R_L = 10 kΩ connected to V_S / 2[1], and V_{CM} = V_{OUT} = V_S / 2[1], unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±6	±25	µV
			T_A = –40°C to +125°C		±0.03	±0.085	µV/°C
PSRR	Power-supply rejection ratio		V_S = 4 V to 36 V, T_A = –40°C to +125°C		±0.075	±0.3	µV/V
	Long-term stability[2]				4		µV
INPUT BIAS CURRENT							
I_B	Input bias current		V_{CM} = V_S / 2		±160	±1400	pA
			T_A = –40°C to +125°C			±8	nA
I_{OS}	Input offset current				±320	±2800	pA
			T_A = –40°C to +125°C			±4	nA
NOISE							
e_n	Input voltage noise		f = 0.1 Hz to 10 Hz		250		nV_{PP}
			f = 0.1 Hz to 10 Hz		40		nVrms
	Input voltage noise density		f = 1 kHz		8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density		f = 1 kHz		7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range		T_A = –40°C to +125°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio		(V–) < V_{CM} < (V+) – 1.5 V	120	134		dB
			(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V	130	146		dB
			(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V, T_A = –40°C to +125°C	120	126		dB
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 6		MΩ || pF
Z_{IC}	Common-mode				6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		(V–) + 0.5 V < V_O < (V+) – 0.5 V	130	136		dB
			(V–) + 0.5 V < V_O < (V+) – 0.5 V, T_A = –40°C to +125°C	120	126		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				2		MHz
SR	Slew rate		G = +1		0.8		V/µs
t_S	Settling time	0.1%	V_S = ±18 V, G = 1, 10-V step		20		µs
		0.01%	V_S = ±18 V, G = 1, 10-V step		27		µs
t_{OR}	Overload recovery time		V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise		1 kHz, G = 1, V_{OUT} = 1 Vrms		0.0001%		

(1) V_S / 2 = midsupply.
(2) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

ELECTRICAL CHARACTERISTICS: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = +8 V to +36 V) (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S / 2[1], and V_{CM} = V_{OUT} = V_S / 2[1], unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		T_A = –40°C to +125°C		310	350	mV
I_{SC}	Short-circuit current	Sinking		-18		mA
		Sourcing		+16		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		4 to 36 (±2 to ±18)			V
I_Q	Quiescent current (per amplifier)	V_S = ±4 V to V_S = ±18 V		450	510	µA
		I_O = 0 mA, T_A = –40°C to +125°C			540	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		+125	°C
T_A	Operating temperature range		–55		+150	°C
T_{stg}	Storage temperature range		–65		+150	°C

ELECTRICAL CHARACTERISTICS: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V)

At T_A = +25°C, R_L = 10 kΩ connected to V_S / 2 (1), and V_{CM} = V_{OUT} = V_S / 2 (1), unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±6	±25	µV
		T_A = –40°C to +125°C		±0.03	±0.085	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, T_A = –40°C to +125°C		0.075	0.3	µV/V
	Long-term stability (2)			4		µV
INPUT BIAS CURRENT						
I_B	Input bias current			±160	±1400	pA
		T_A = –40°C to +125°C			±8	nA
I_{OS}	Input offset current			±320	±2800	pA
		T_A = –40°C to +125°C			±4	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		250		nV_{PP}
		f = 0.1 Hz to 10 Hz		40		nVrms
	Input voltage noise density	f = 1 kHz		8.8		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1 kHz		7		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V	114	120		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V, T_A = –40°C to +125°C	110	120		dB
INPUT IMPEDANCE						
Z_{ID}	Differential			100 || 6		MΩ || pF
Z_{IC}	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 5 kΩ	110	120		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V	120	130		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, T_A = –40°C to +125°C	110	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 Vrms		0.0001%		

(1) V_S / 2 = midsupply.
(2) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

ELECTRICAL CHARACTERISTICS: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V) (continued)

At T_A = +25°C, R_L = 10 kΩ connected to V_S / 2[(1)], and V_{CM} = V_{OUT} = V_S / 2[(1)], unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		T_A = –40°C to +125°C		310	350	mV
I_{SC}	Short-circuit current	Sinking		-18		mA
		Sourcing		+16		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		4 to 36 (±2 to ±18)			V
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		425	480	µA
		I_O = 0 mA, T_A = –40°C to +125°C			525	µA
TEMPERATURE RANGE						
	Specified temperature range		–40		+125	°C
T_A	Operating temperature range		–55		+150	°C
T_{stg}	Storage temperature range		–65		+150	°C

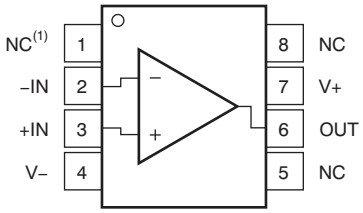
THERMAL INFORMATION

THERMAL METRIC[(1)]		OPA188			UNITS
		D (SO)	DGK (MSOP)	DBV (SOT23)	
		8 PINS	8 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.0	180.4	158.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	68.5	67.9	60.7	
θ_{JB}	Junction-to-board thermal resistance	63.5	102.1	44.8	
ψ_{JT}	Junction-to-top characterization parameter	13.7	10.4	1.6	
ψ_{JB}	Junction-to-board characterization parameter	62.8	100.3	44.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

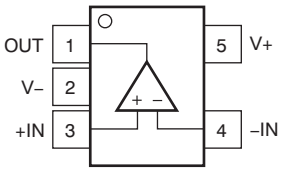
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

OPA188
D, DGK PACKAGES (SO-8, MSOP-8)
(TOP VIEW)



OPA188
DBV PACKAGE (SOT23-5)
(TOP VIEW)



(1) NC = no connection.

FUNCTIONAL BLOCK DIAGRAM

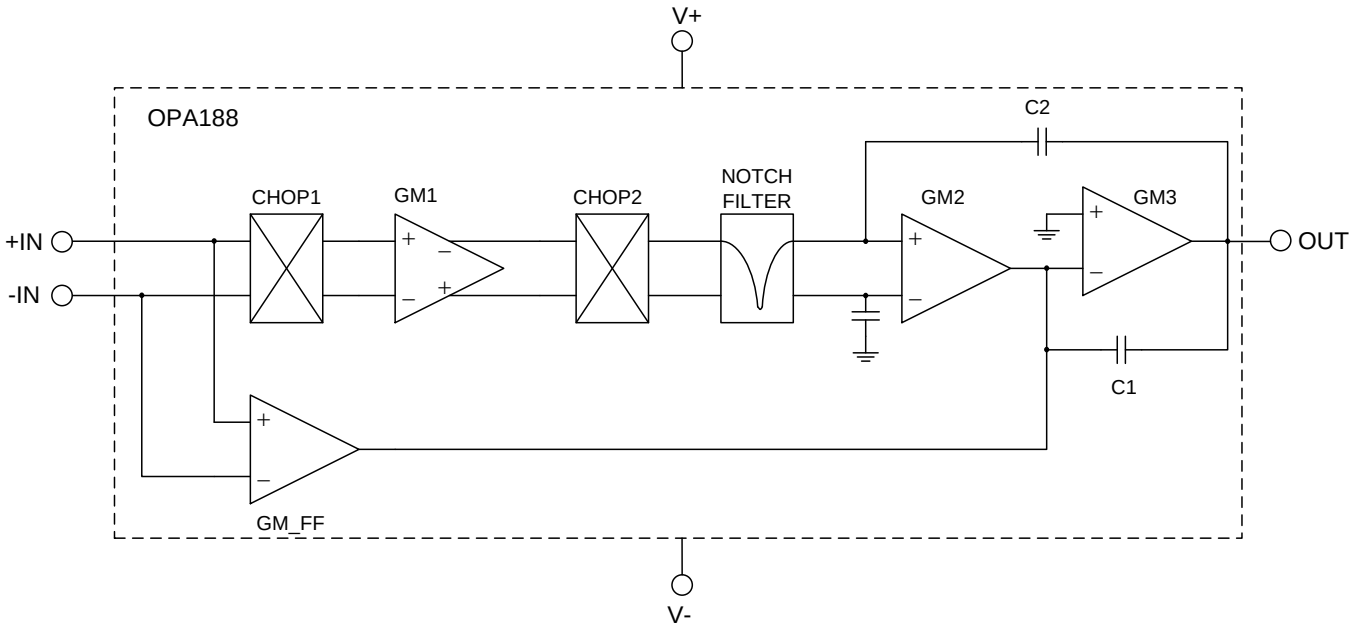


Figure 1. Functional Block Diagram

Table 1. Component Count

COMPONENT	COUNT
Transistors	636
Diodes	5
Resistors	41
Capacitors	72

Figure 1 shows a representation of the proprietary OPA188 architecture. Table 1 contains both the active and passive component count for this device. The component count allows for accurate reliability calculations.

TYPICAL CHARACTERISTICS

Table 2. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 2
Offset Voltage Drift Distribution	Figure 3
Offset Voltage vs Temperature	Figure 4
Offset Voltage vs Common-Mode Voltage	Figure 5, Figure 6
Offset Voltage vs Power Supply	Figure 7
Open-Loop Gain and Phase vs Frequency	Figure 8
Closed-Loop Gain vs Frequency	Figure 9
I_B and I_{OS} vs Common-Mode Voltage	Figure 10
Input Bias Current vs Temperature	Figure 11
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 12
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 13
CMRR vs Temperature	Figure 14, Figure 15
PSRR vs Temperature	Figure 16
0.1-Hz to 10-Hz Noise	Figure 17
Input Voltage Noise Spectral Density vs Frequency	Figure 18
THD+N Ratio vs Frequency	Figure 19
THD+N vs Output Amplitude	Figure 20
Quiescent Current vs Supply Voltage	Figure 21
Quiescent Current vs Temperature	Figure 22
Open-Loop Gain vs Temperature	Figure 23
Open-Loop Output Impedance vs Frequency	Figure 24
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 25, Figure 26
No Phase Reversal	Figure 27
Positive Overload Recovery	Figure 28
Negative Overload Recovery	Figure 29
Small-Signal Step Response (100 mV)	Figure 30, Figure 31
Large-Signal Step Response	Figure 32, Figure 33
Large-Signal Settling Time (10-V Positive Step)	Figure 34
Large-Signal Settling Time (10-V Negative Step)	Figure 35
Short-Circuit Current vs Temperature	Figure 36
Maximum Output Voltage vs Frequency	Figure 37
EMIRR IN+ vs Frequency	Figure 38

TYPICAL CHARACTERISTICS

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

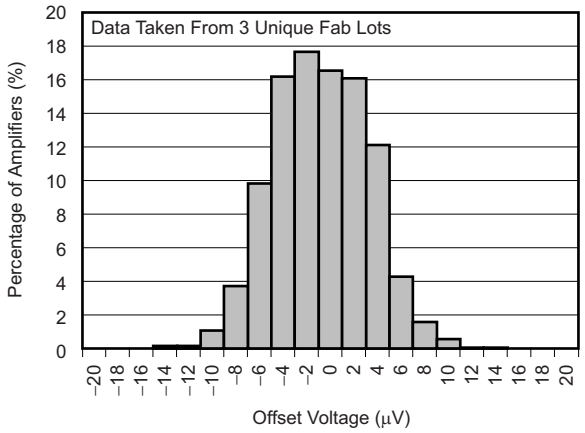


Figure 2. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

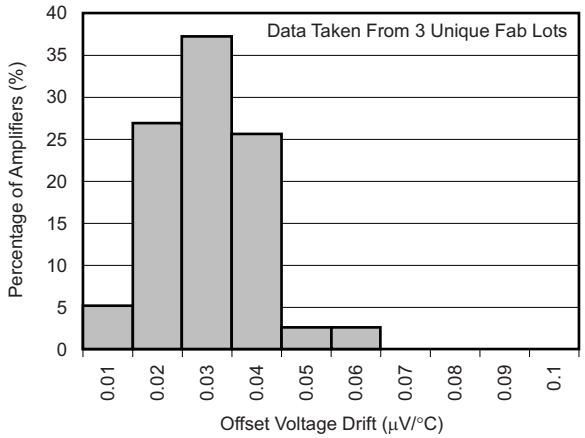


Figure 3. OFFSET VOLTAGE DRIFT DISTRIBUTION

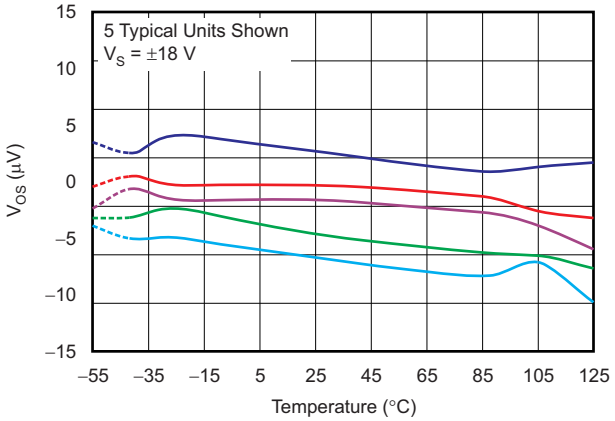


Figure 4. OFFSET VOLTAGE vs TEMPERATURE

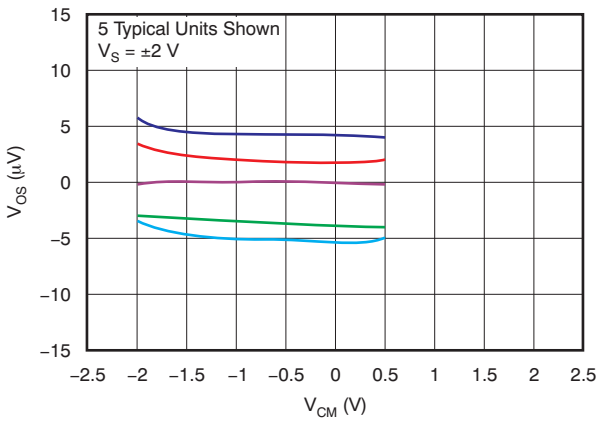


Figure 5. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

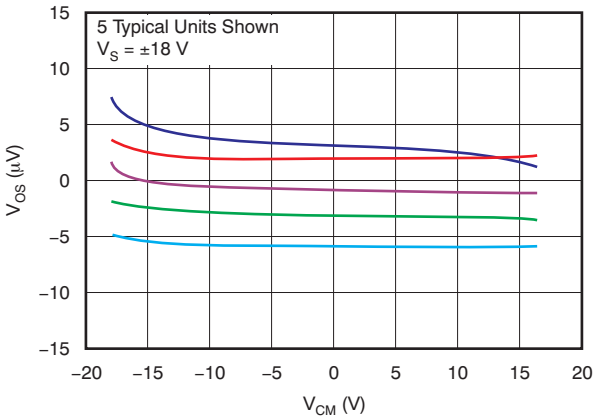


Figure 6. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

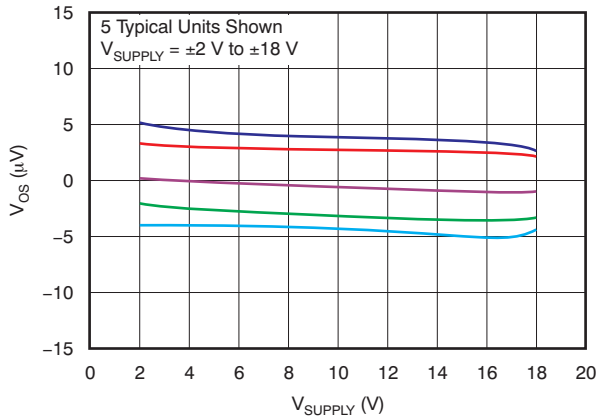


Figure 7. OFFSET VOLTAGE vs POWER SUPPLY

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

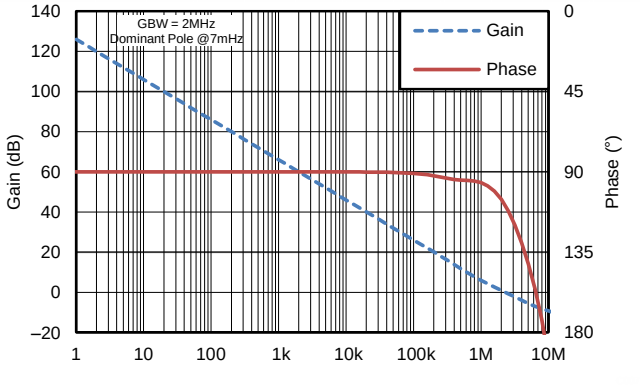


Figure 8. OPEN-LOOP GAIN AND PHASE vs FREQUENCY

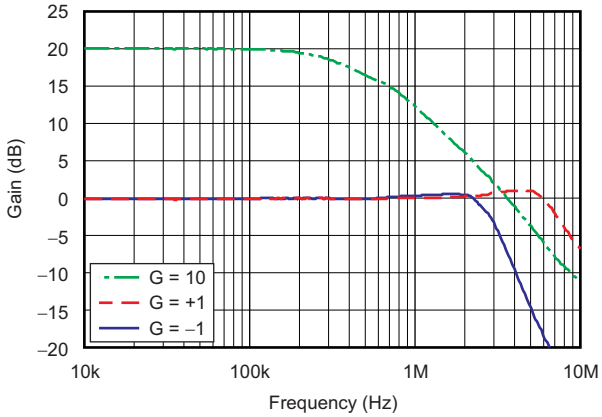


Figure 9. CLOSED-LOOP GAIN vs FREQUENCY

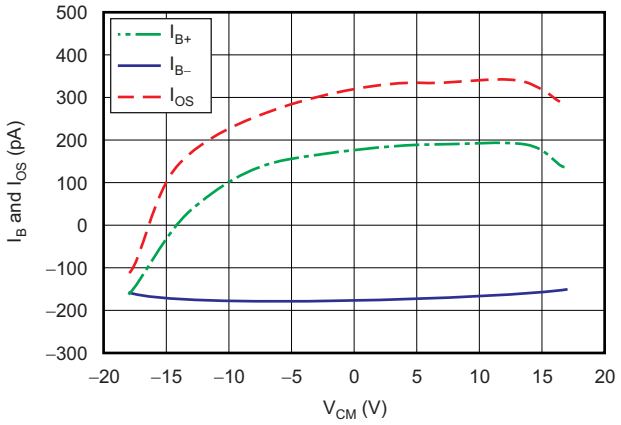


Figure 10. I_B AND I_{OS} vs COMMON-MODE VOLTAGE

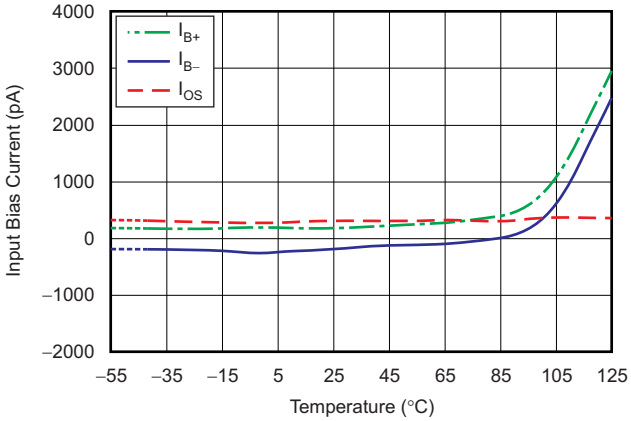


Figure 11. INPUT BIAS CURRENT vs TEMPERATURE

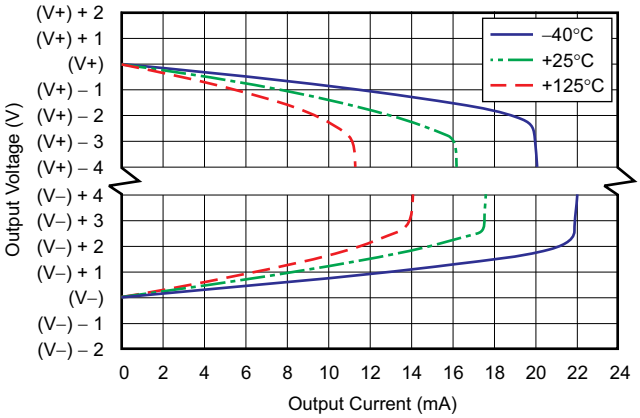


Figure 12. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (Maximum Supply)

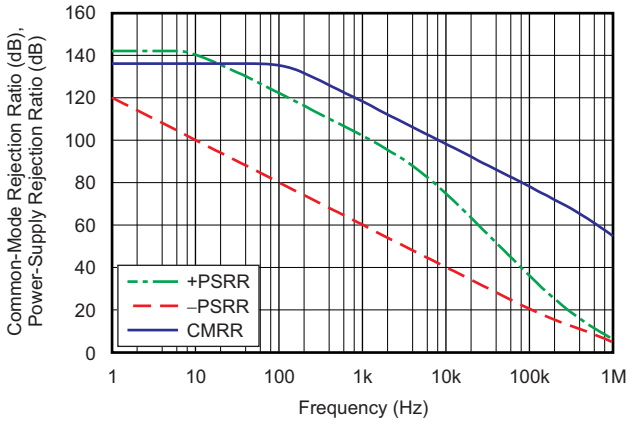


Figure 13. CMRR AND PSRR vs FREQUENCY (Referred-to-Input)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

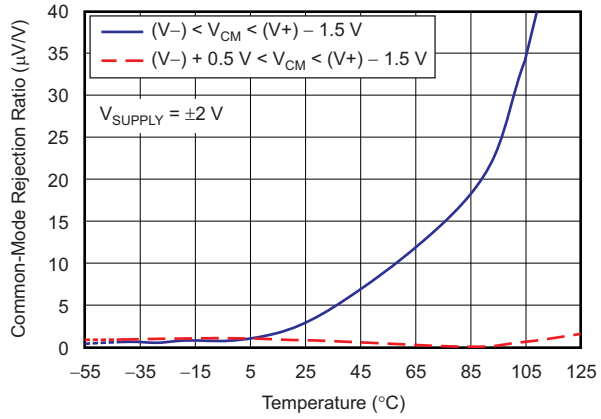


Figure 14. CMRR vs TEMPERATURE

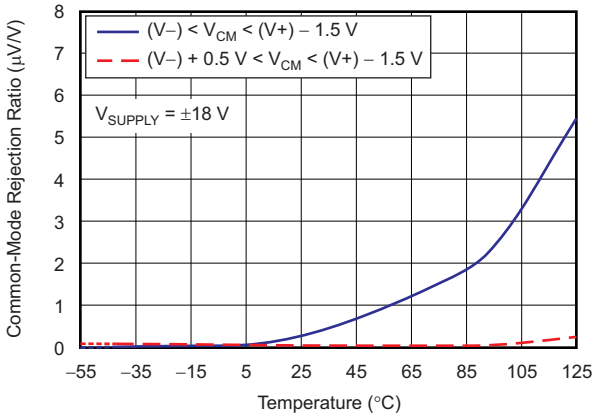


Figure 15. CMRR vs TEMPERATURE

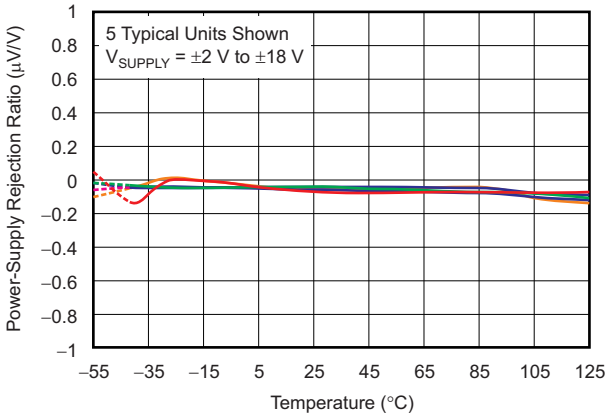


Figure 16. PSRR vs TEMPERATURE

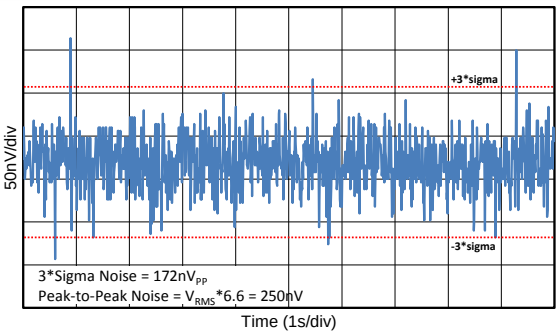


Figure 17. 0.1-Hz TO 10-Hz NOISE

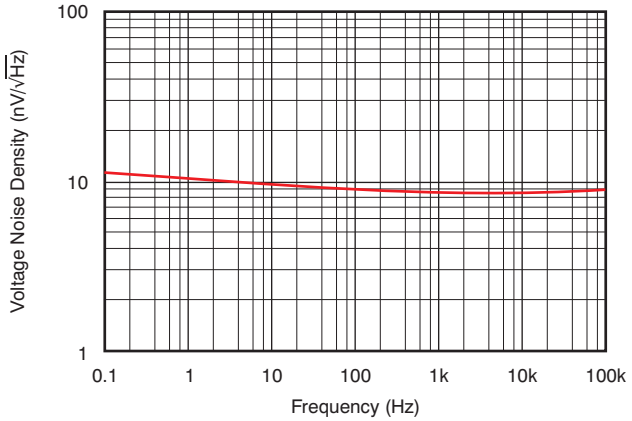


Figure 18. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

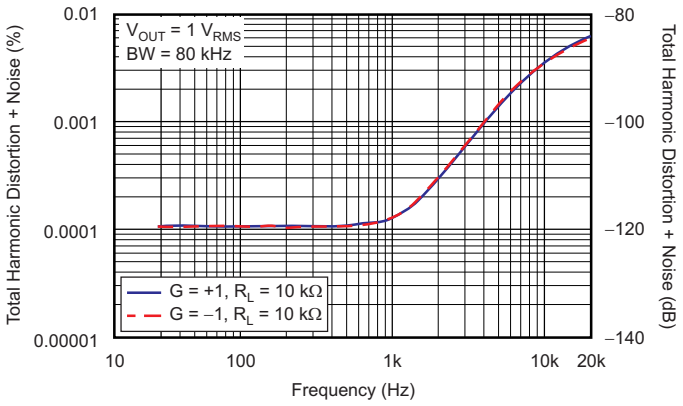


Figure 19. THD+N RATIO vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

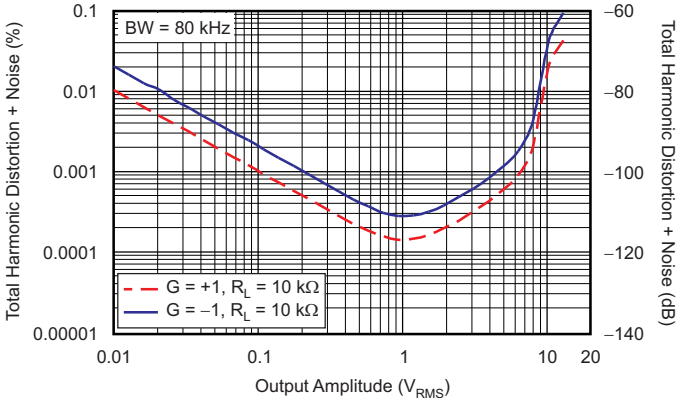


Figure 20. THD+N vs OUTPUT AMPLITUDE

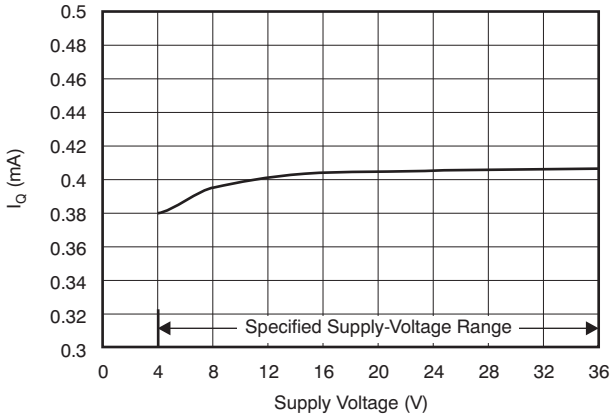


Figure 21. QUIESCENT CURRENT vs SUPPLY VOLTAGE

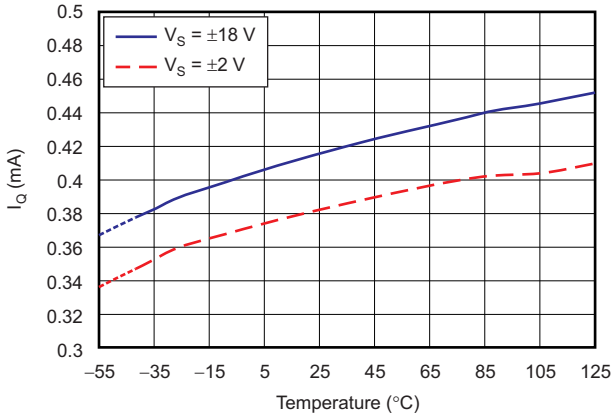


Figure 22. QUIESCENT CURRENT vs TEMPERATURE

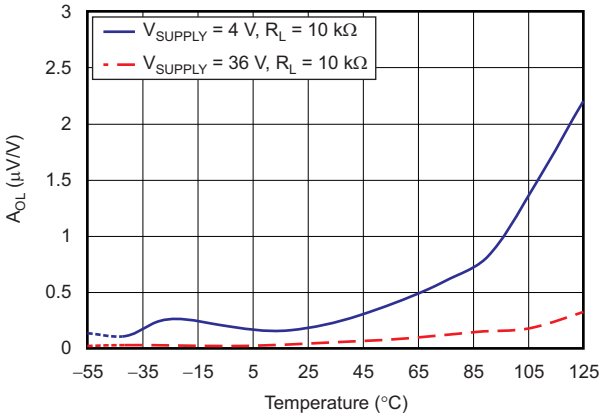


Figure 23. OPEN-LOOP GAIN vs TEMPERATURE

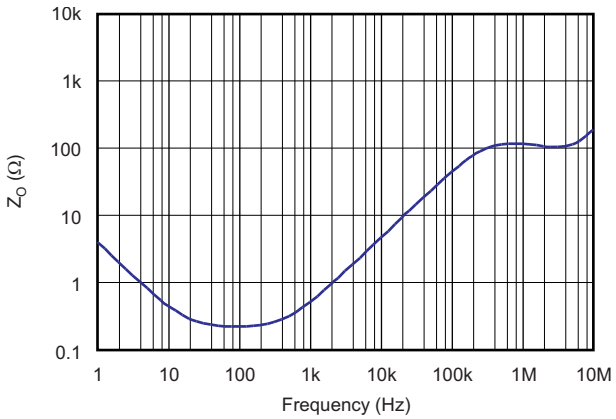


Figure 24. OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

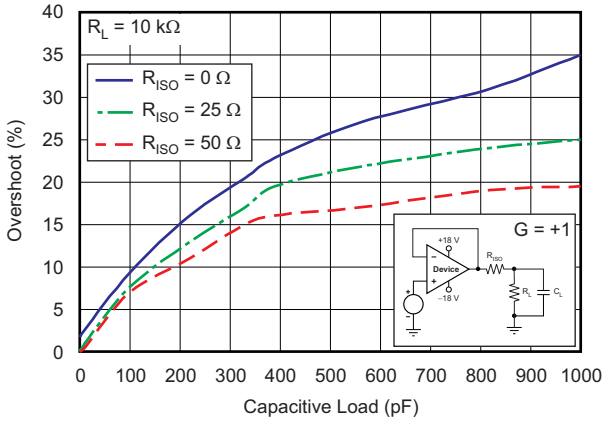


Figure 25. SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

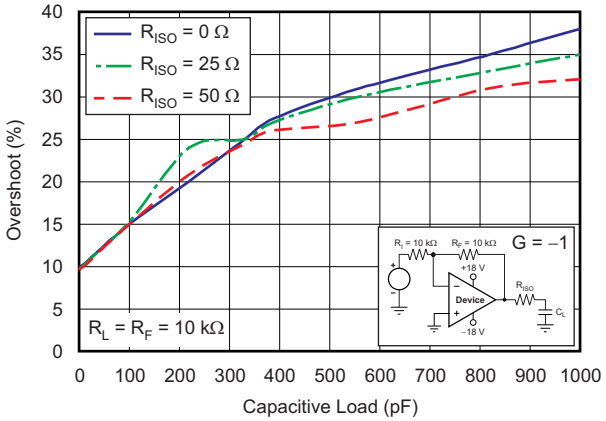


Figure 26. SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100-mV Output Step)

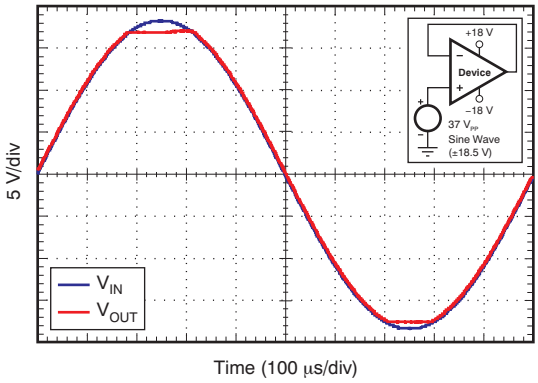


Figure 27. NO PHASE REVERSAL

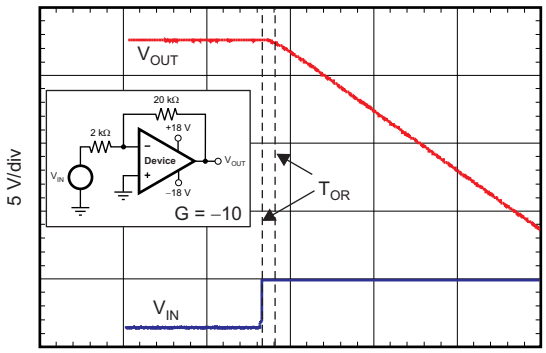


Figure 28. POSITIVE OVERLOAD RECOVERY

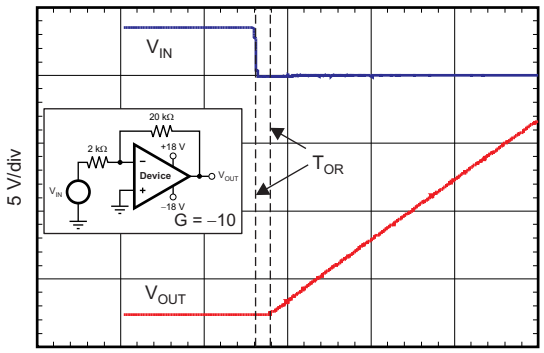


Figure 29. NEGATIVE OVERLOAD RECOVERY

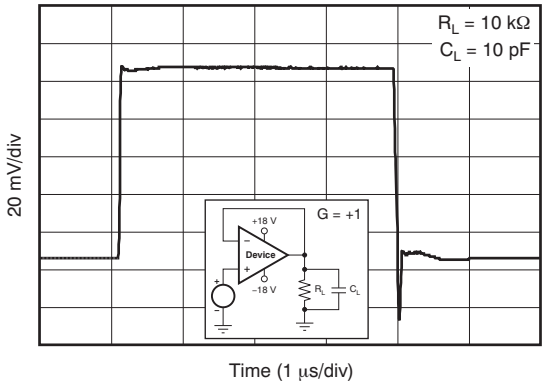


Figure 30. SMALL-SIGNAL STEP RESPONSE (100 mV)

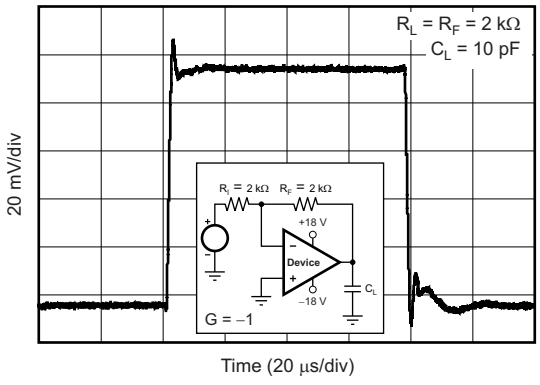


Figure 31. SMALL-SIGNAL STEP RESPONSE (100 mV)

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

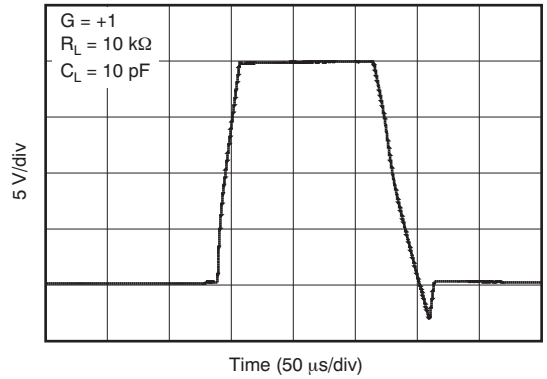


Figure 32. LARGE-SIGNAL STEP RESPONSE

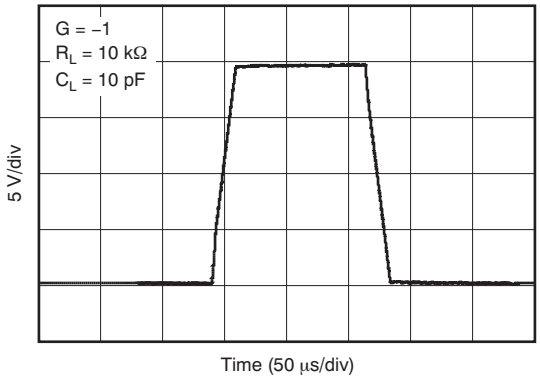


Figure 33. LARGE-SIGNAL STEP RESPONSE

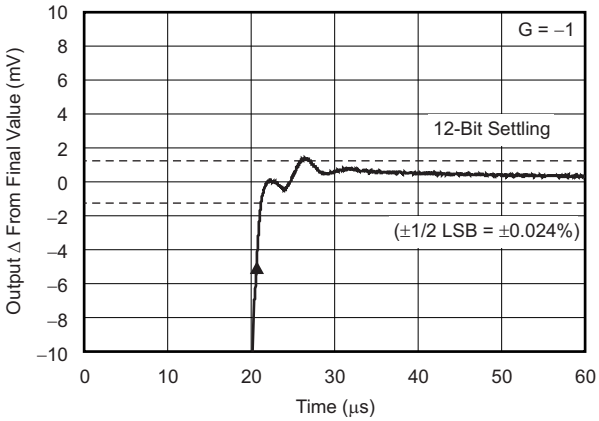


Figure 34. LARGE-SIGNAL SETTLING TIME (10-V Positive Step)

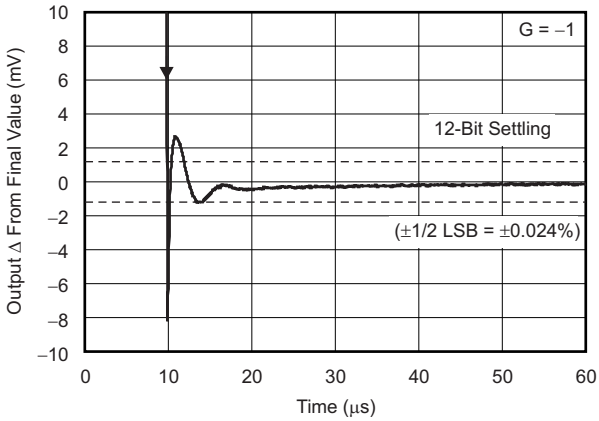


Figure 35. LARGE-SIGNAL SETTLING TIME (10-V Negative Step)

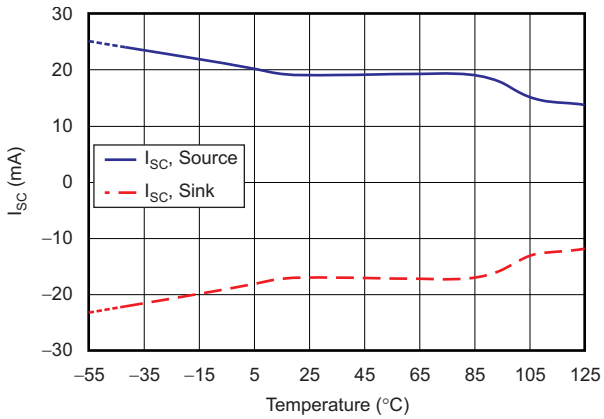


Figure 36. SHORT-CIRCUIT CURRENT vs TEMPERATURE

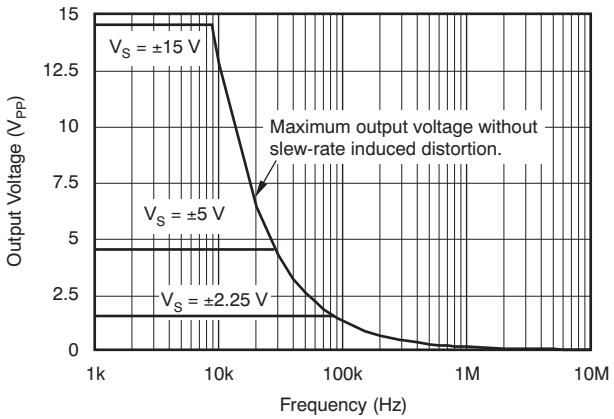


Figure 37. MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

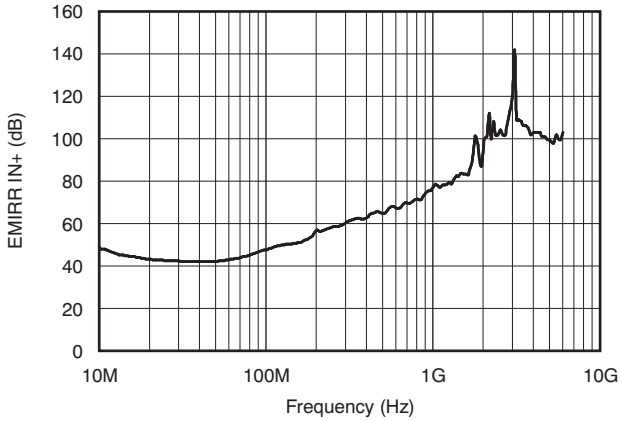


Figure 38. EMIRR IN+ vs FREQUENCY

APPLICATION INFORMATION

The OPA188 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085 µV per degree Celsius provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

OPERATING CHARACTERISTICS

The OPA188 is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics section.

EMI REJECTION

The OPA188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 39 shows the results of this testing on the OPA188. Table 3 shows the EMIRR IN+ values for the OPA188 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 3 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the Application Report *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

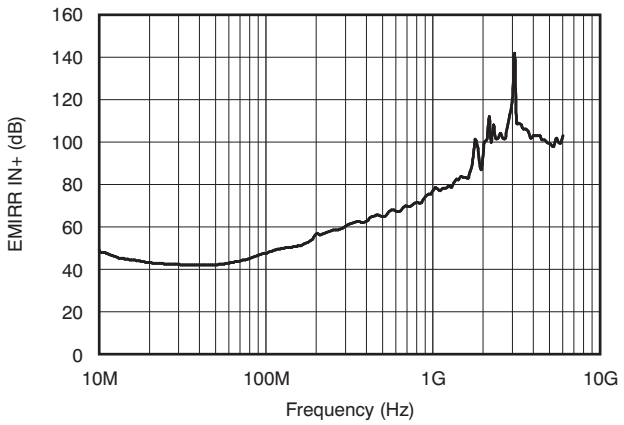


Figure 39. EMIRR Testing

Table 3. OPA188 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	62.2 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	74.7 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	100.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	102.4 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	104.8 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	100.3 dB

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Including:

- Low-ESR, 0.1-µF ceramic bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.
- In order to reduce parasitic coupling, run the input traces as far away from the supply lines as possible.
- A ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

PHASE-REVERSAL PROTECTION

The OPA188 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 40.

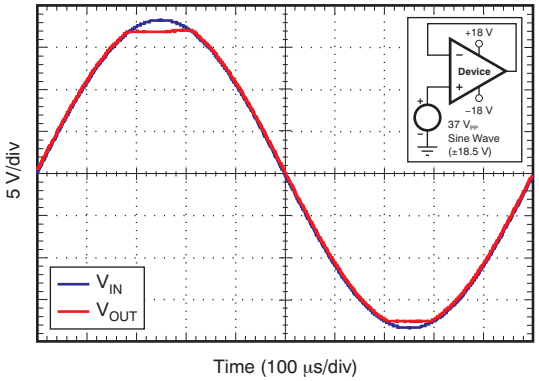


Figure 40. No Phase Reversal

INPUT BIAS CURRENT CLOCK FEEDTHROUGH

Zero-drift amplifiers, such as the OPA188, use switching on their inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce very short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents them from being amplified, however they may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

INTERNAL OFFSET CORRECTION

The OPA188 op amp uses an auto-calibration technique with a time-continuous 750-kHz op amp in the signal path. This amplifier is zero-corrected every 3 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

CAPACITIVE LOAD AND STABILITY

The device dynamic characteristics are optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the amplifier phase margin and can lead to gain peaking or oscillations. As a result, larger capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to the Applications Report, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from www.ti.com, for details of analysis techniques and application circuits.

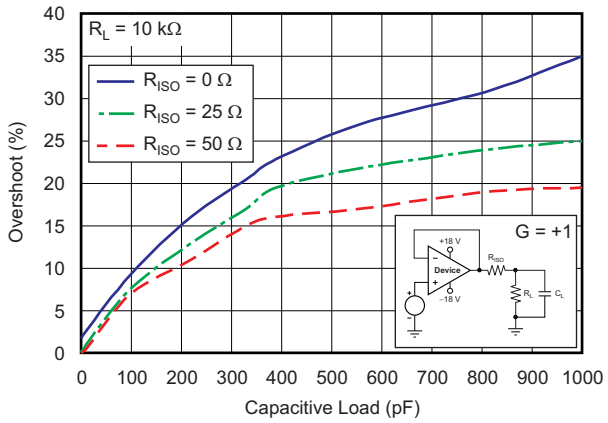


Figure 41. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

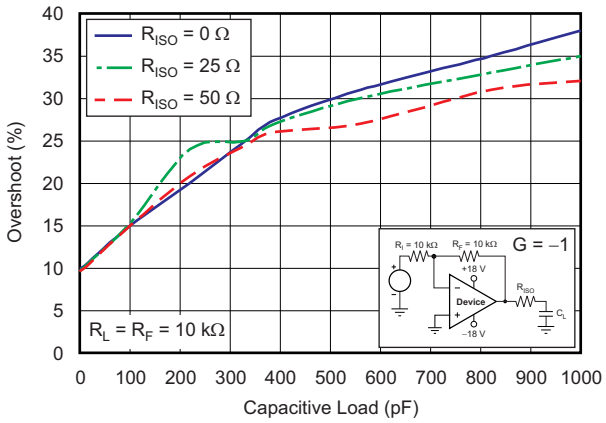


Figure 42. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. See Figure 43 for an illustration of the ESD circuits contained in the OPA188 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA188 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

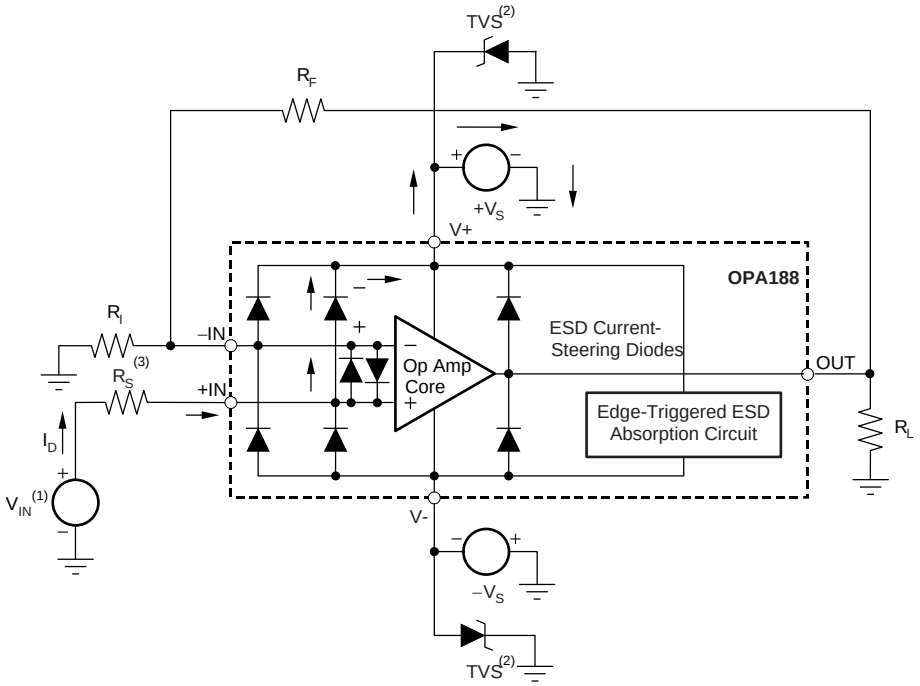
When the operational amplifier connects into a circuit (such as the one Figure 43 depicts), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 43 shows a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current-steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins, as shown in Figure 43. The zener voltage must be selected such that the diode does not turn on during normal operation. However, the zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500$ mV.

(2) TVS: $+V_{S(max)} > V_{TVSBR\ (min)} > +V_S$.

(3) Suggested value is approximately 1 kΩ.

Figure 43. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

The OPA188 input terminals are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 43. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA188. Figure 43 shows an example configuration that implements a current-limiting feedback resistor.

APPLICATION EXAMPLES

The following application examples highlight only a few of the circuits where the OPA188 can be used.

TINA-TI™ (Free Download Software)

Using a TINA-TI SPICE-Based Analog Simulation Program with the OPA188

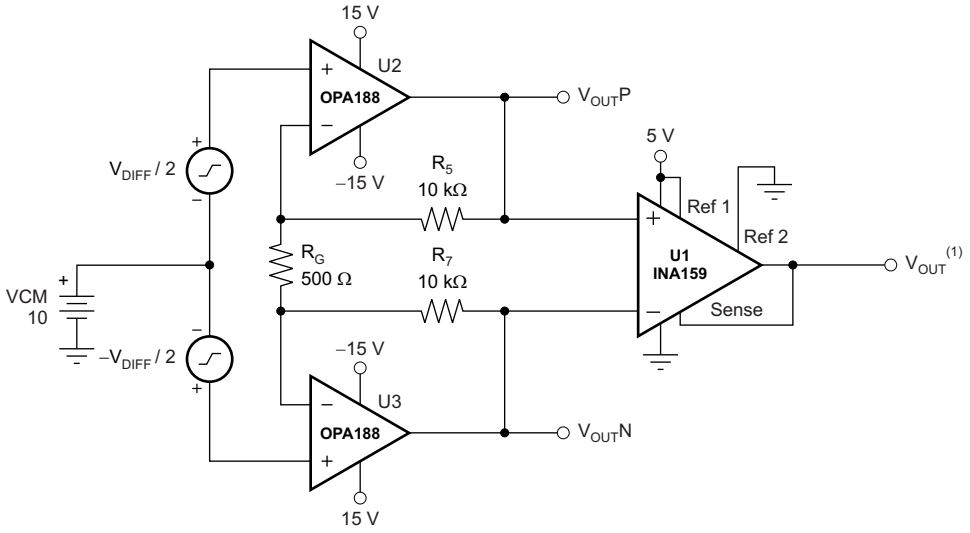
TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

Figure 44 shows an example of how the OPA188 can be used as a high-voltage, high-impedance front-end for a precision, discreet instrumentation amplifier with attenuation. The INA159 provides the attenuation that allows this circuit to easily interface with 3.3-V or 5-V analog-to-digital converters (ADCs). Click the following link download the TINA-TI file: Discreet INA.



(1) $V_{OUT} = V_{DIFF} \times (41 / 5) + (Ref 1) / 2$.

Figure 44. Discrete INA + Attenuation for ADC with 3.3-V Supply

Figure 45 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: Bridge Amplifier Circuit.

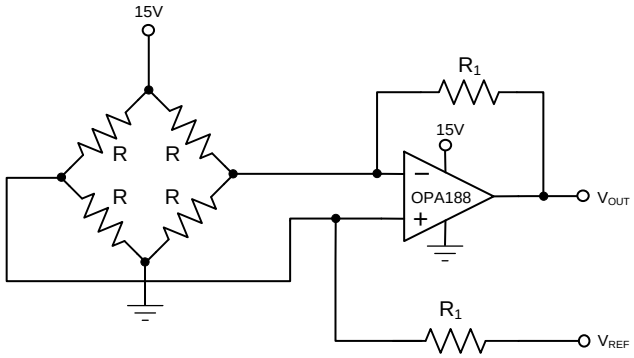


Figure 45. Bridge Amplifier

Figure 46 shows the OPA188 configured in a low-side current-sensing application. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the OPA188, with a gain of 201. The load current is set from 0 A to 500 mA, which corresponds to an output voltage range from 0 V to 10 V. The output range can be adjusted by changing the shunt resistor or gain of the configuration. Click the following link to download the TINA-TI file: Current-Sensing Circuit.

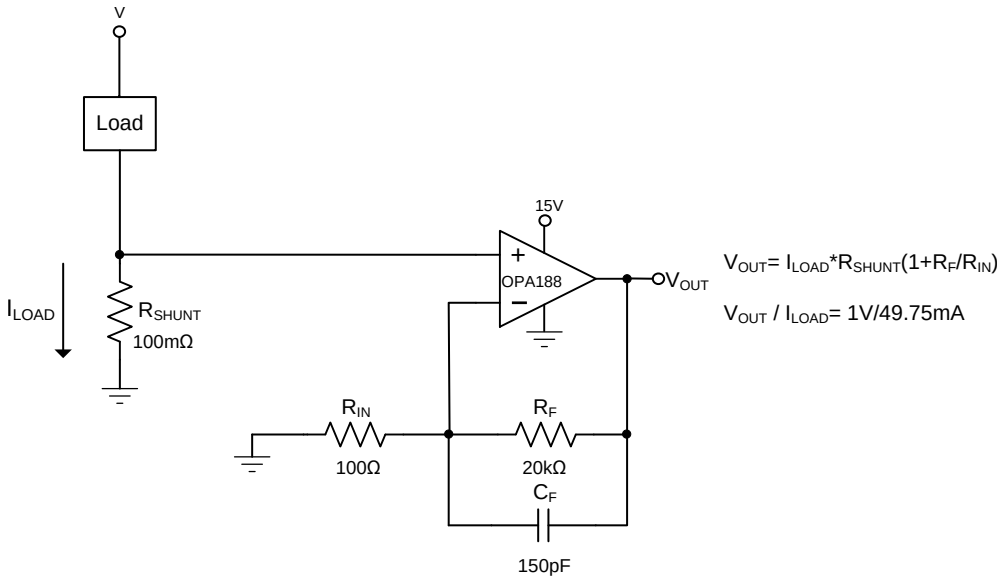


Figure 46. Low-Side Current Monitor

Figure 47 shows the OPA188 configured as a precision programmable power supply using the 16-bit, voltage output DAC8581 and the OPA548 high-current amplifier. This application amplifies the digital-to-analog converter (DAC) voltage by a value of five and handles a large variety of capacitive and current loads. The OPA188 in the front-end provides precision and low drift across a wide range of inputs and conditions. Click the following link to download the TINA-TI file: Programmable Power-Supply Circuit.

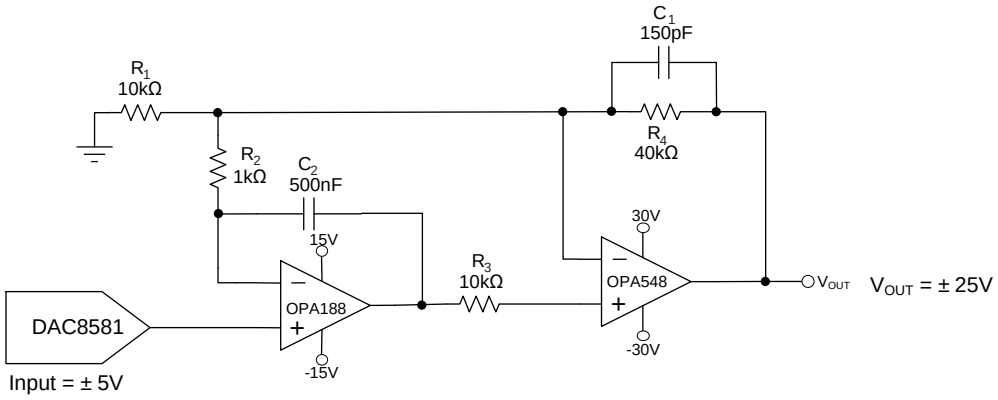
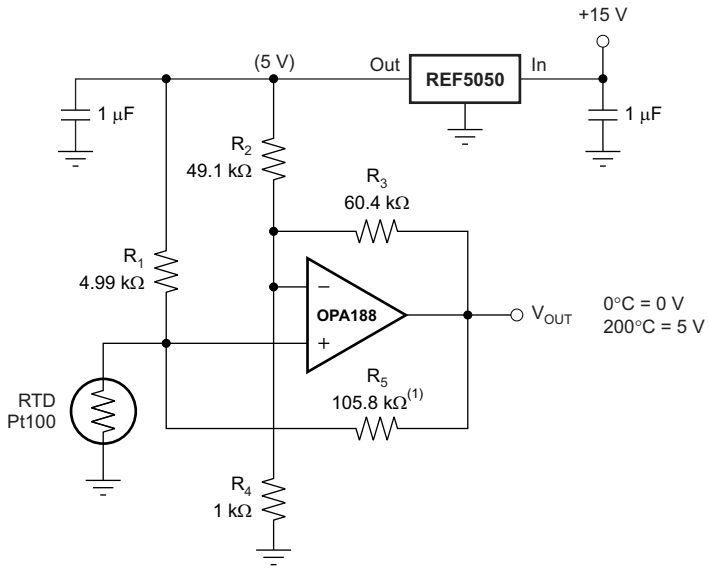


Figure 47. Programmable Power Supply

Refer to the Applications Report, *Analog linearization of resistance temperature detectors* (SLYT442) for an in-depth analysis of Figure 48. Click the following link to download the TINA-TI file: RTD Amplifier with Linearization.



(1) R_5 provides positive-varying excitation to linearize output.

Figure 48. RTD Amplifier with Linearization

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2013) to Revision A	Page
• Changed document status to Production Data	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA188AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA188	Samples
OPA188AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXZ	Samples
OPA188AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXZ	Samples
OPA188AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXX	Samples
OPA188AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXX	Samples
OPA188AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA188	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

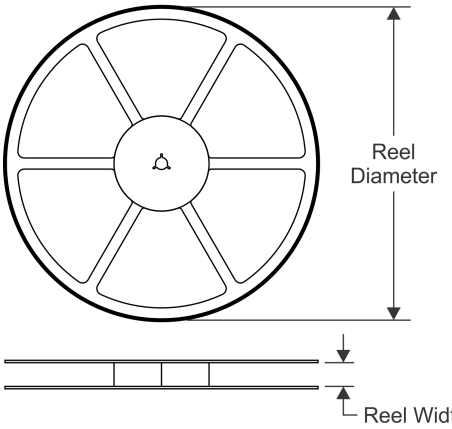
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

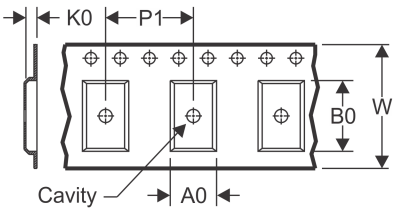
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

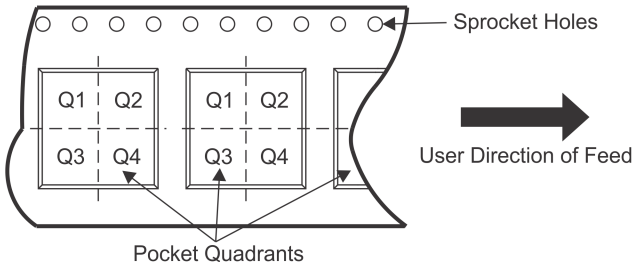


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

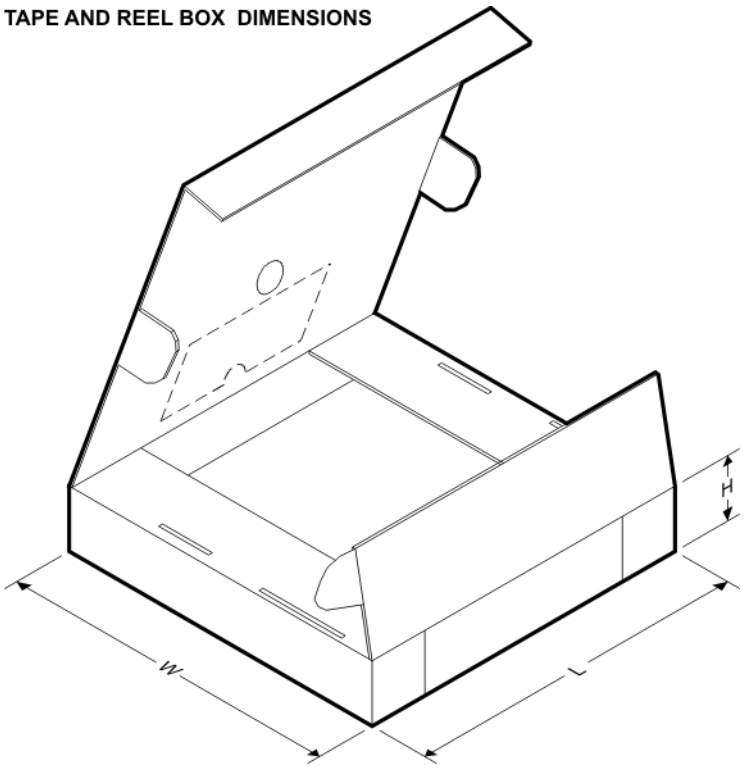
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA188AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA188AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA188AIDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

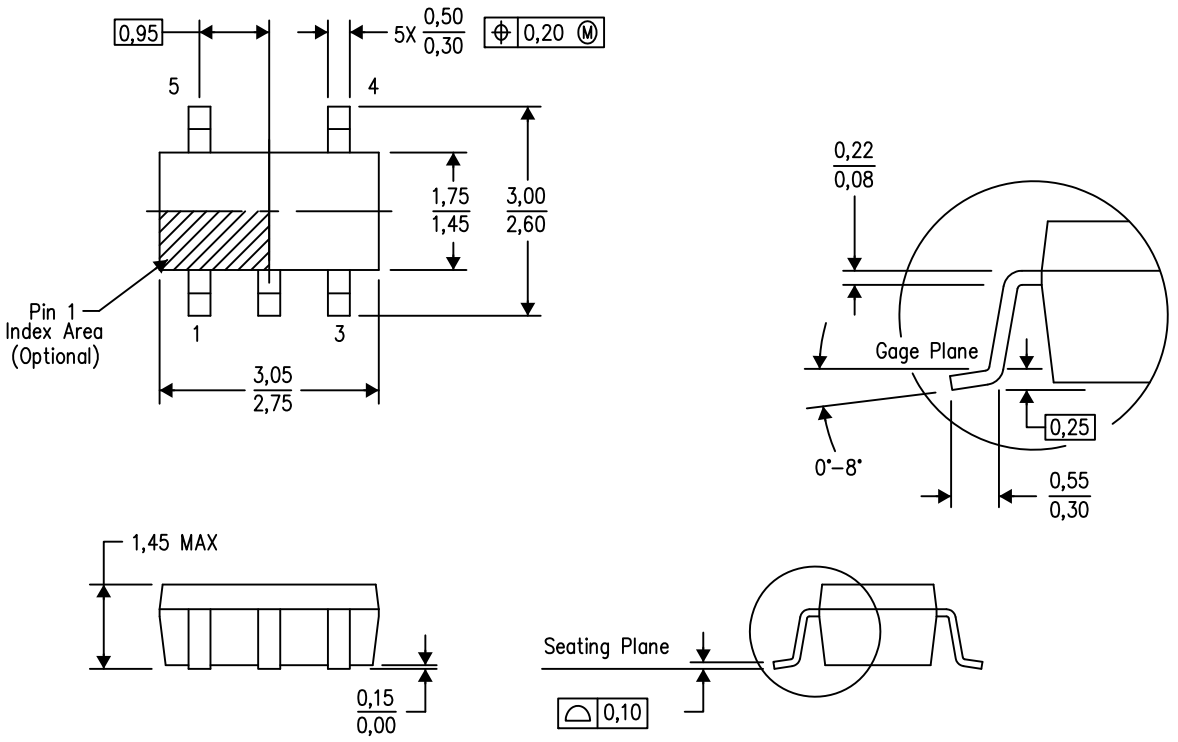
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA188AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA188AIDBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
OPA188AIDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
OPA188AIDGKT	VSSOP	DGK	8	250	202.0	201.0	28.0

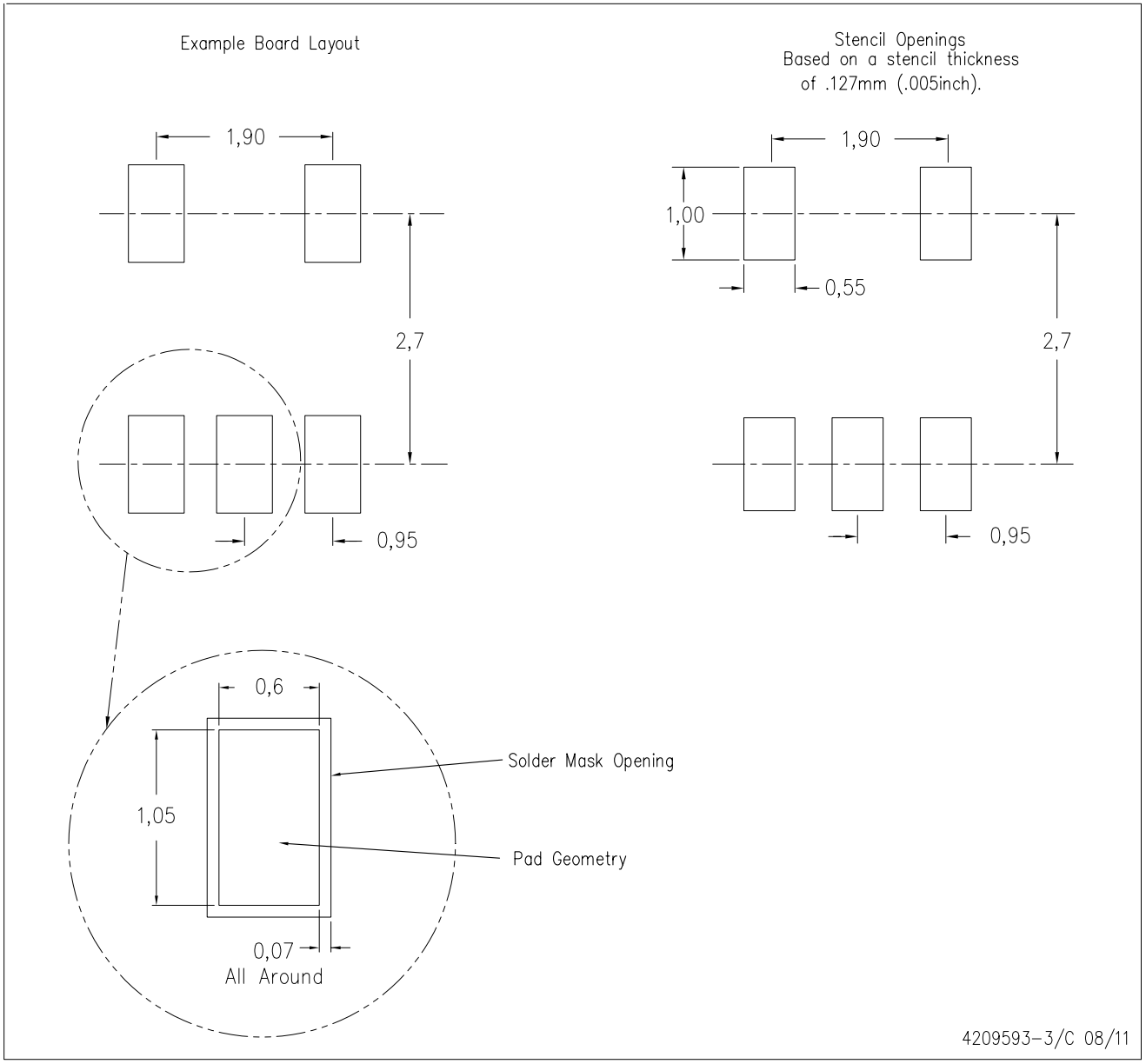
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

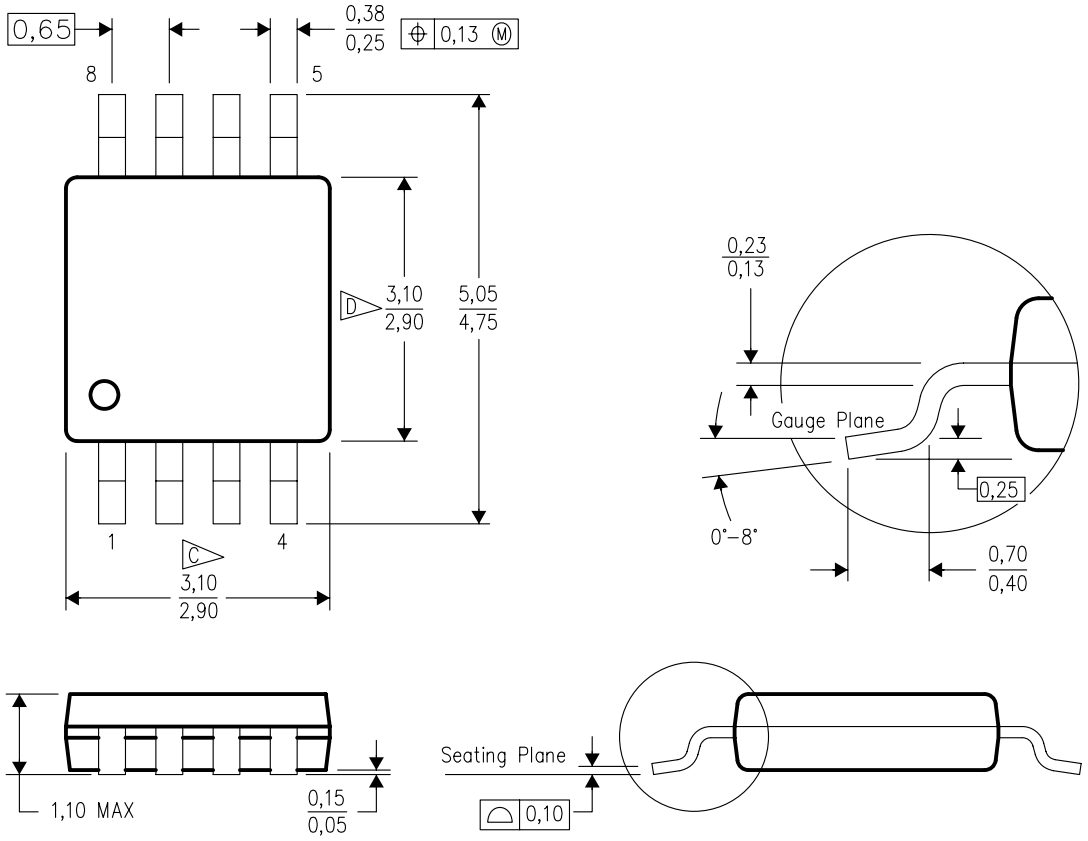
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

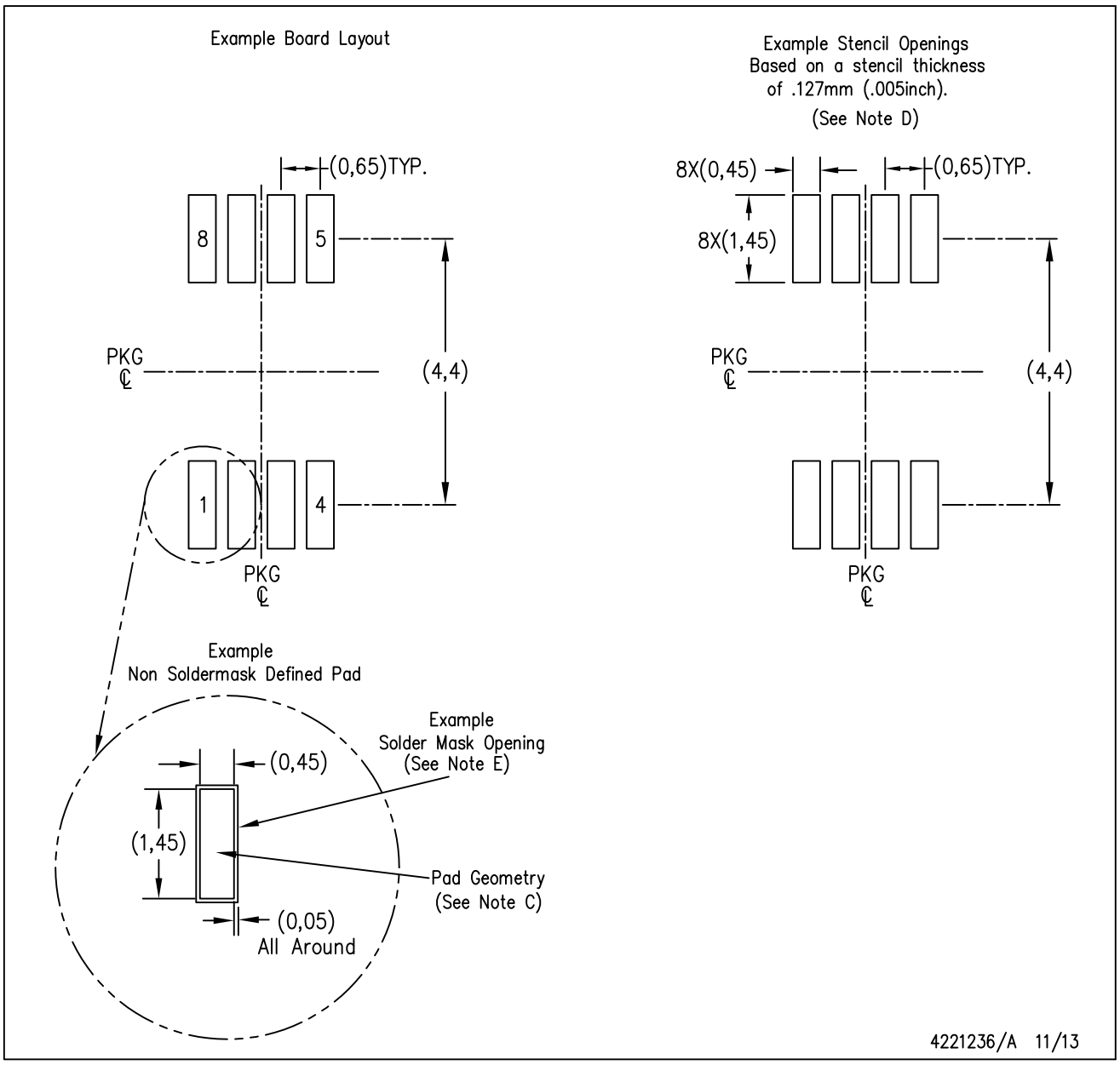
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

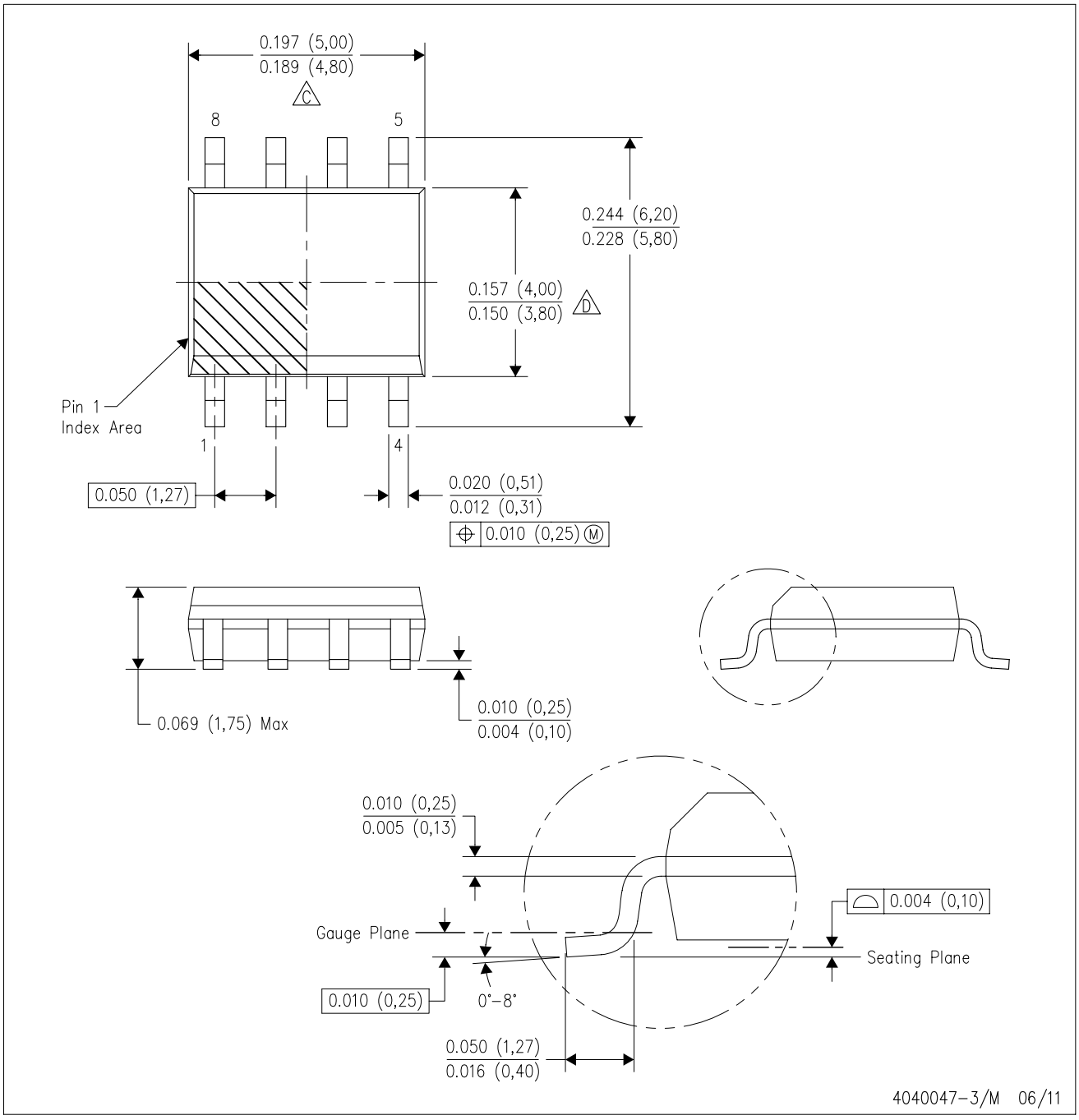
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



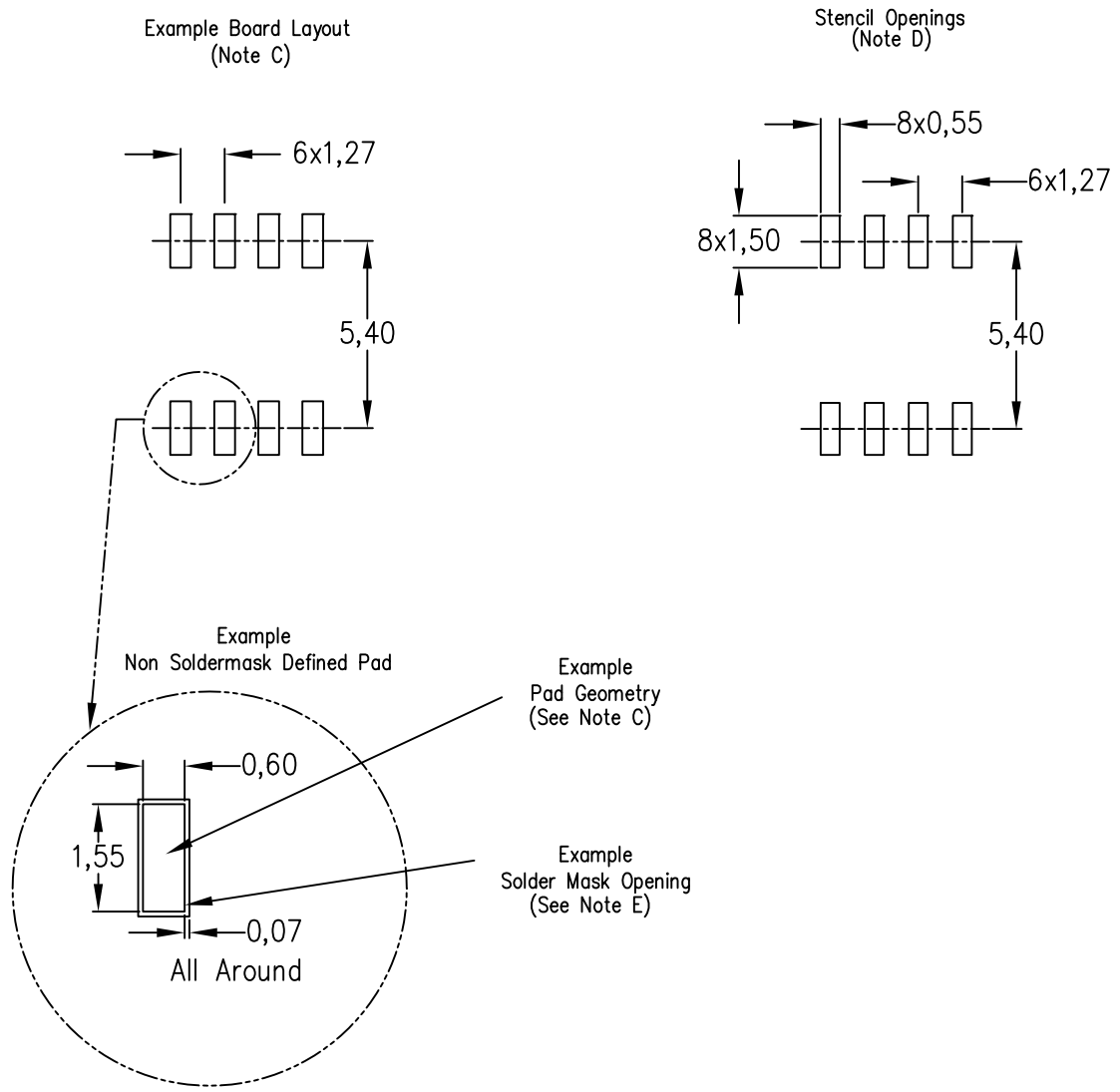
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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