Average circuit eigenvalue sampling on NISQ devices

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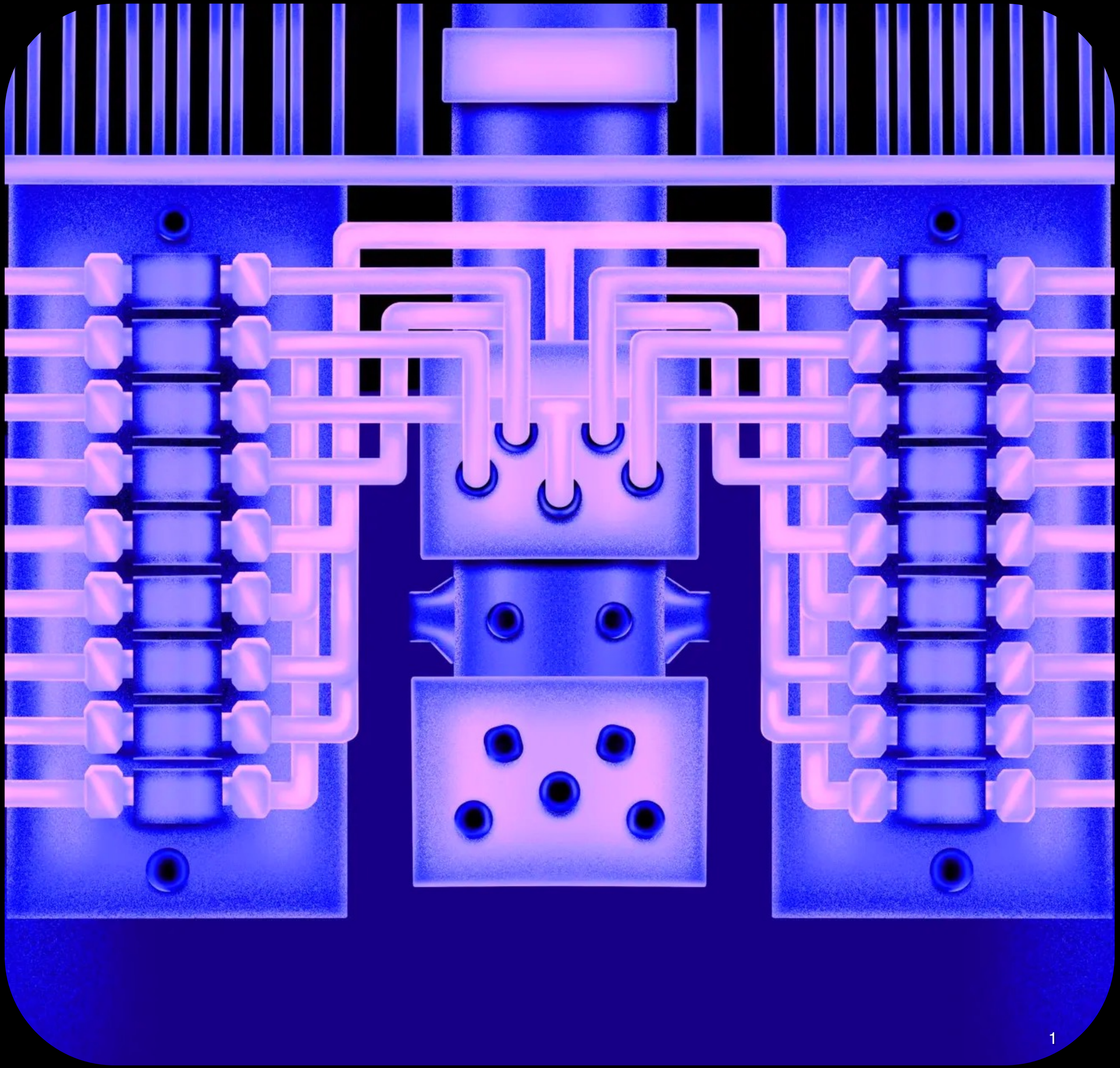


Average circuit eigenvalue sampling

Introduced by Steven T. Flammia in https://arxiv.org/abs/2108.05803.

Allows us to estimate the Pauli error channels of the individual gates of a device's native gateset in "parallel".

We present the following:

- A step-by-step implementation for NISQ devices.
- Simulation and real-device results.
- Possible future steps to extend protocol to non-Clifford gatesets.

Averaged circuits

We consider circuits composed of Clifford gates as $\tilde{\mathcal{C}} = \tilde{\mathcal{G}}_T \cdots \tilde{\mathcal{G}}_1$. Each gate can be twirled to **isolate the Pauli noise** around its implementation. The **$\mathcal{G}$-twisted twirl** of a noisy gate $\mathcal{G}$ is defined as

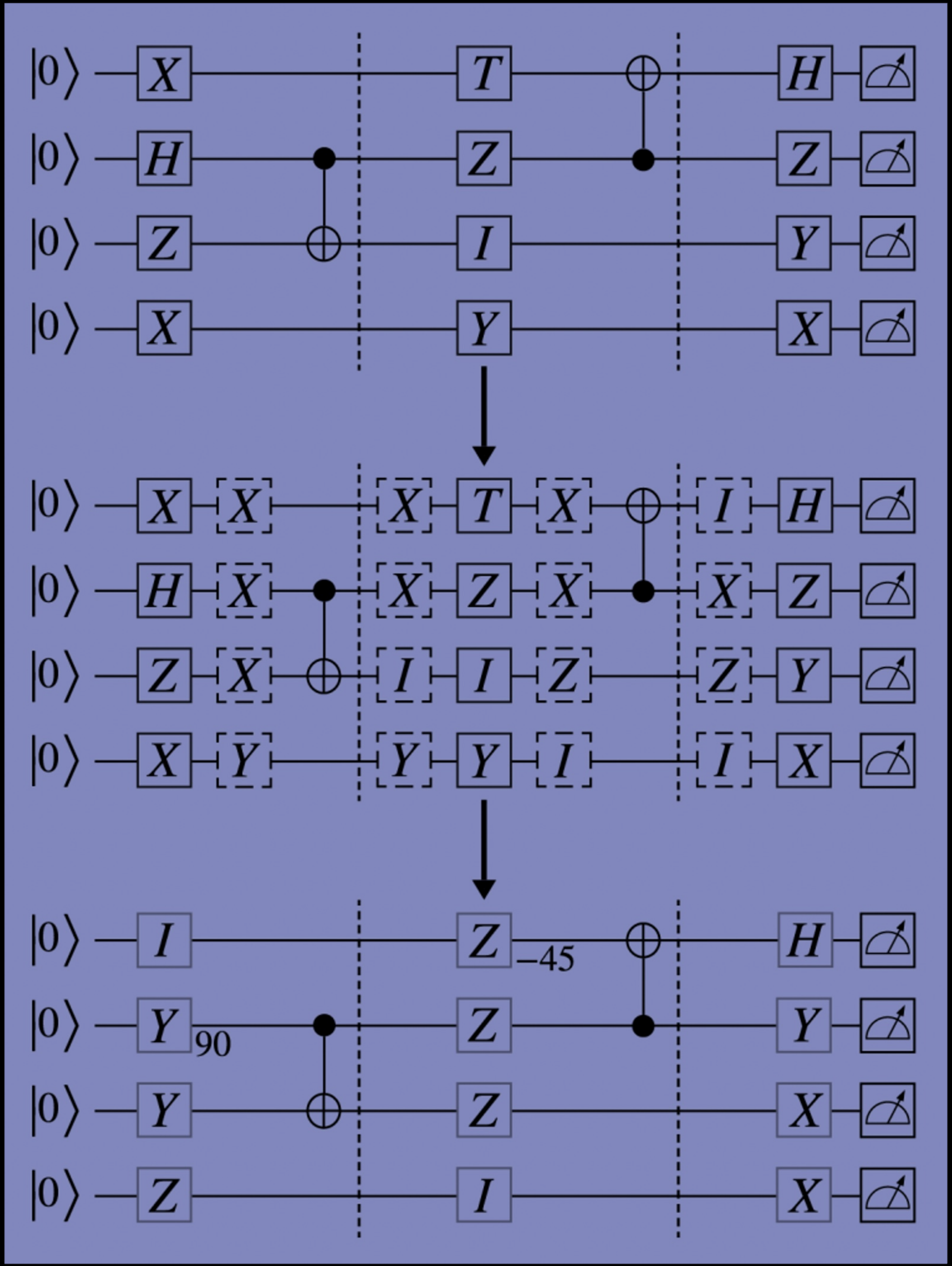
$$\tilde{\mathcal{G}}^P(\rho) = \frac{1}{4^n} \sum_a P_{a'}^\dagger \tilde{\mathcal{G}}\left(P_a \rho P_a^\dagger\right) P_{a'} = \mathcal{G}(\mathcal{E}^P(\rho))$$

In a circuit, this looks like the following:

$$\text{------ } \tilde{\mathcal{G}} \text{ ------} \rightarrow \text{------ } P_a \text{ ------ } \tilde{\mathcal{G}} \text{ ------ } P_{a'} \text{ ------}$$

Where $P_{a'} = \mathcal{G}(P_a) = \mathcal{G} P_a \mathcal{G}^\dagger$ and P_a is chosen at random.

Original $\tilde{\mathcal{C}}$



Ensemble of circuits $\tilde{\mathcal{C}}^P$

arxiv:2010.00215

Eigenvalue sampling

Given a noisy averaged implementation $\tilde{\mathcal{C}}^P$ of a circuit $\mathcal{C}$, we define the **circuit eigenvalue** of this circuit with respect to some Pauli P_a as

$$\tilde{\mathcal{C}}^P(P_a) = \Lambda_{c,a}\mathcal{C}^P(P_a) = \Lambda_{c,a}P_{a'}$$

$$\Lambda_{c,a} = \frac{1}{2^n}\mathrm{Tr}(P_{a'}\tilde{\mathcal{C}}^P(P_a))$$

However, we can't send a Pauli directly through a circuit, but we can send its eigenvectors.

$$\Lambda_{c,a} = \frac{1}{2^n}[\mathrm{Tr}(P_{a'}\tilde{\mathcal{C}}^P(\rho_+)) - \mathrm{Tr}(P_{a'}\tilde{\mathcal{C}}^P(\rho_-))]$$

Circuit and gate eigenvalues

We can characterize the individual **gate eigenvalues** from the circuit eigenvalues.
We have the following equality:

$$\tilde{\mathcal{C}}^P(P_a) = \prod_{k=1}^{M} \lambda_{k,a_k} \mathcal{C}(P_a)$$

Where the circuits have M gates and each gate eigenvalue is:

$$\tilde{\mathcal{G}}_i^P(P_{a_i}) = \lambda_{i,a_i} \mathcal{G}(P_{a_i}) = \lambda_{i,a_i} P_{a_j}$$

Then, the circuit and gate eigenvalues are related by:

$$\Lambda_{\mathcal{C},a_1} = \prod_{k=1}^{M} \lambda_{k,a_k}$$

Solving the model

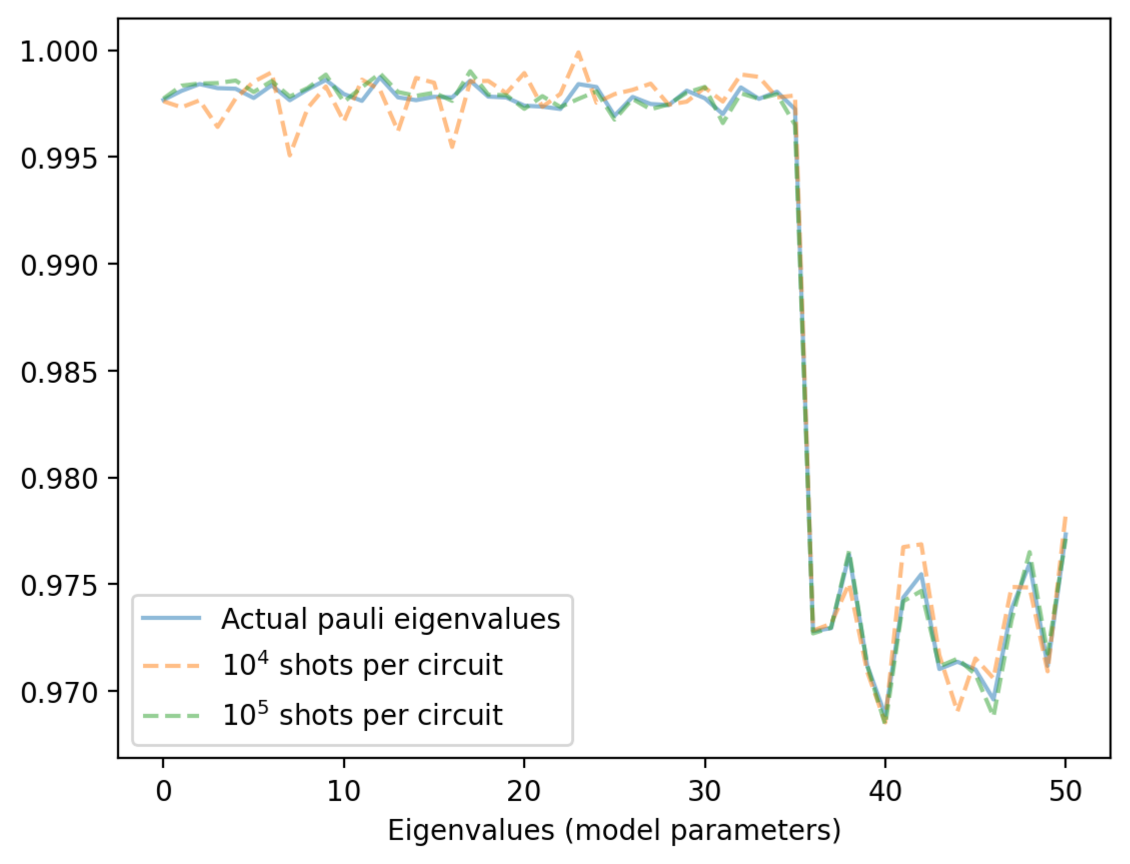
- For every circuit and input Pauli, we define an index $\mu = \left(\mathcal{C}_k, a_{k_i}\right)$.
- We do the same for gates, defining an index $\nu = \left(\mathcal{G}_k, a_{k_i}\right)$.
- We then define $\Lambda_\mu = e^{-b_\mu}$ and $\lambda_\nu = e^{-x_\nu}$.
- We construct a design matrix A that depends on the circuits and input Paulis.
- To get the gate eigenvalues, we solve $A\vec{x} = \vec{b}$ (e.g., via least squares).

Protocol

- Define the **gateset** we want to characterize .
- Construct a collection of **random circuits** built from gates in this gateset.
  + Each circuit consists of two sections: a **mirror section** with alternating moments of one- and two-qubit gates, followed by the same operations in reverse; and a **fully random section**.
- For each circuit, we get a set of **good Pauli operators** we can send through.
  + An example criteria to characterize the good operators is that we require them to have at most weight two both when going into the circuit and when coming out.
- Construct a **design matrix** from the set of circuits and corresponding Pauli operators.
- Use the difference trick to get the circuit eigenvalues.
- Solve the model!

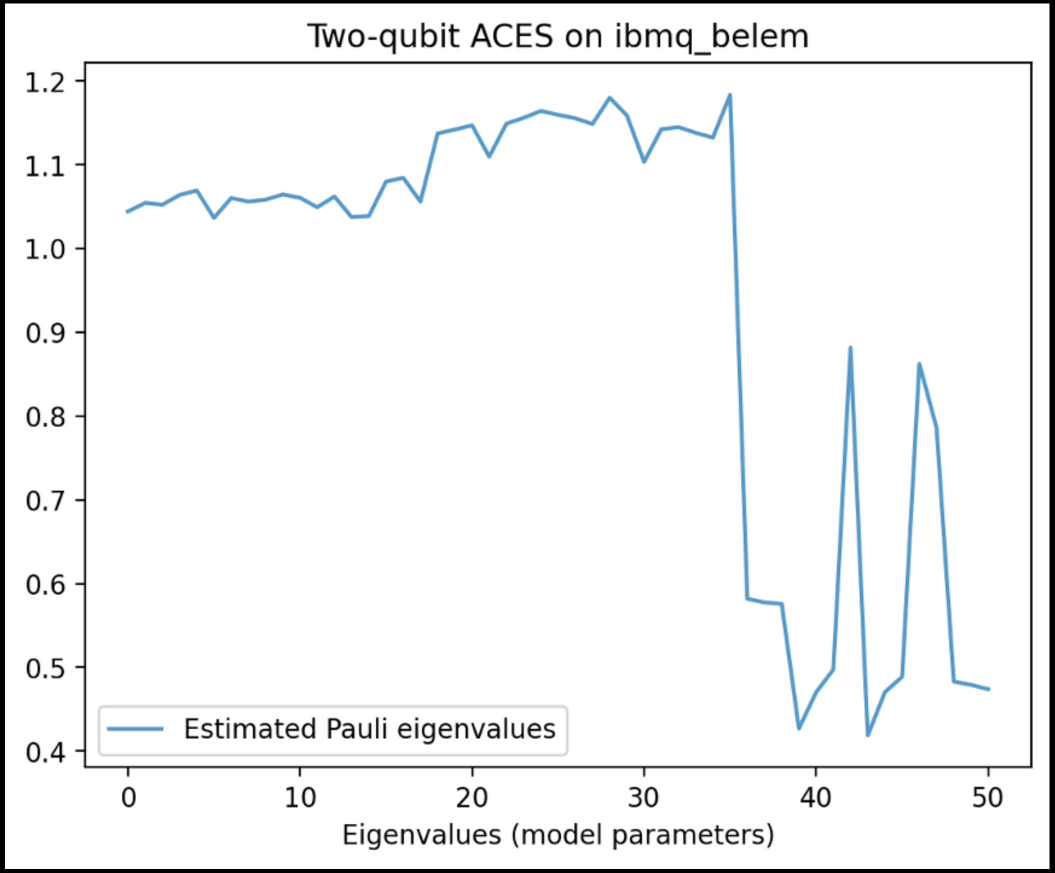
2-qubit simulation

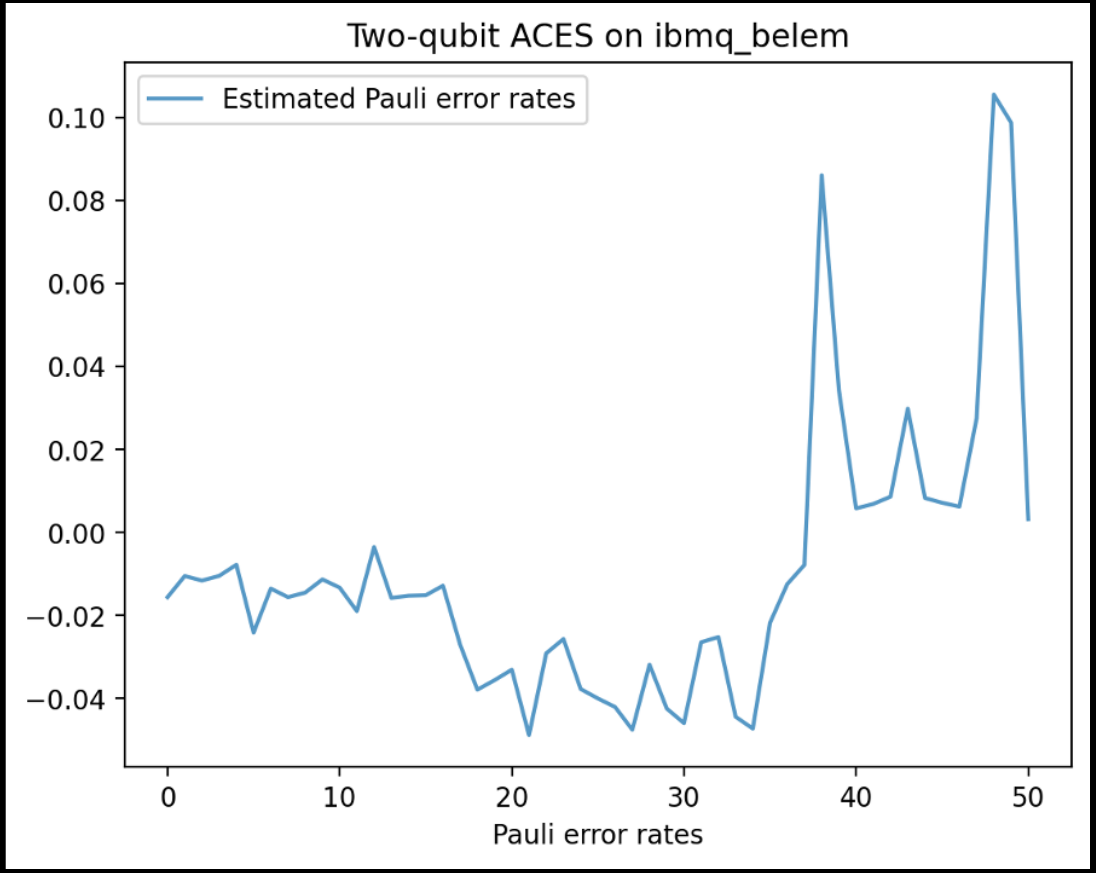
4 mirror + 6 random, 10 circuits, 10 twirls



2-qubit IBMQ Belem

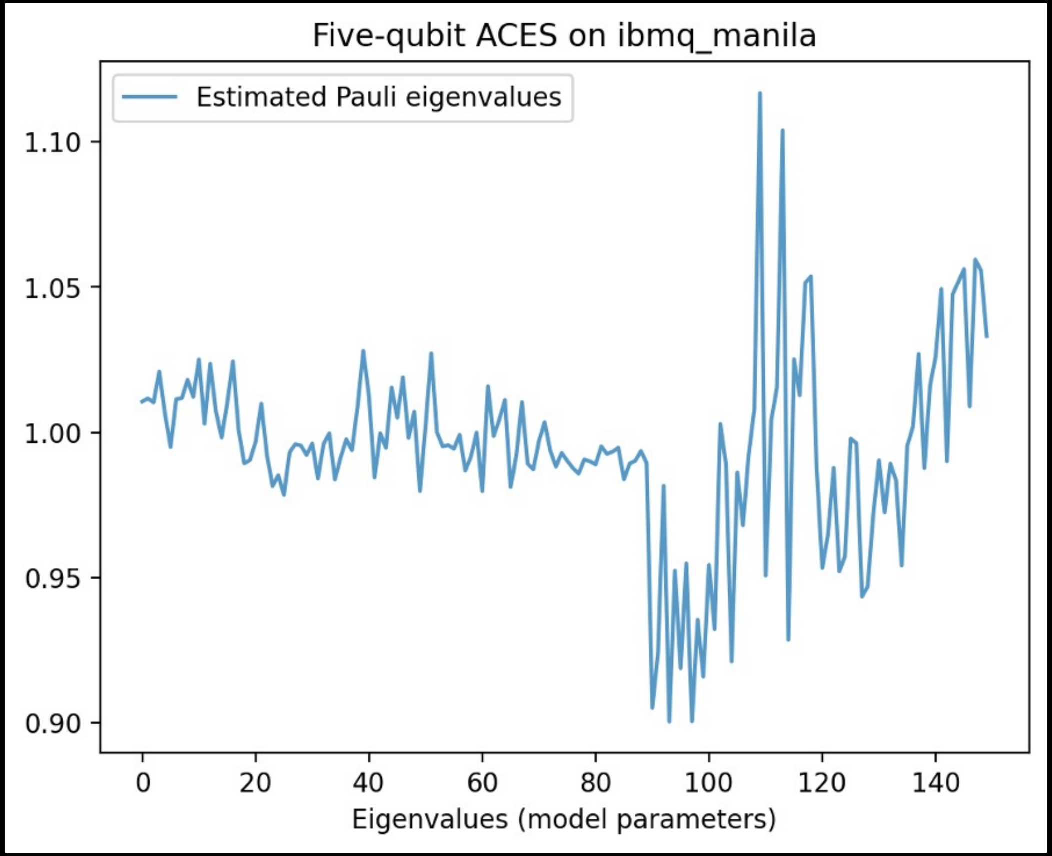
4 mirror + 6 random, 10 circuits, no twirls

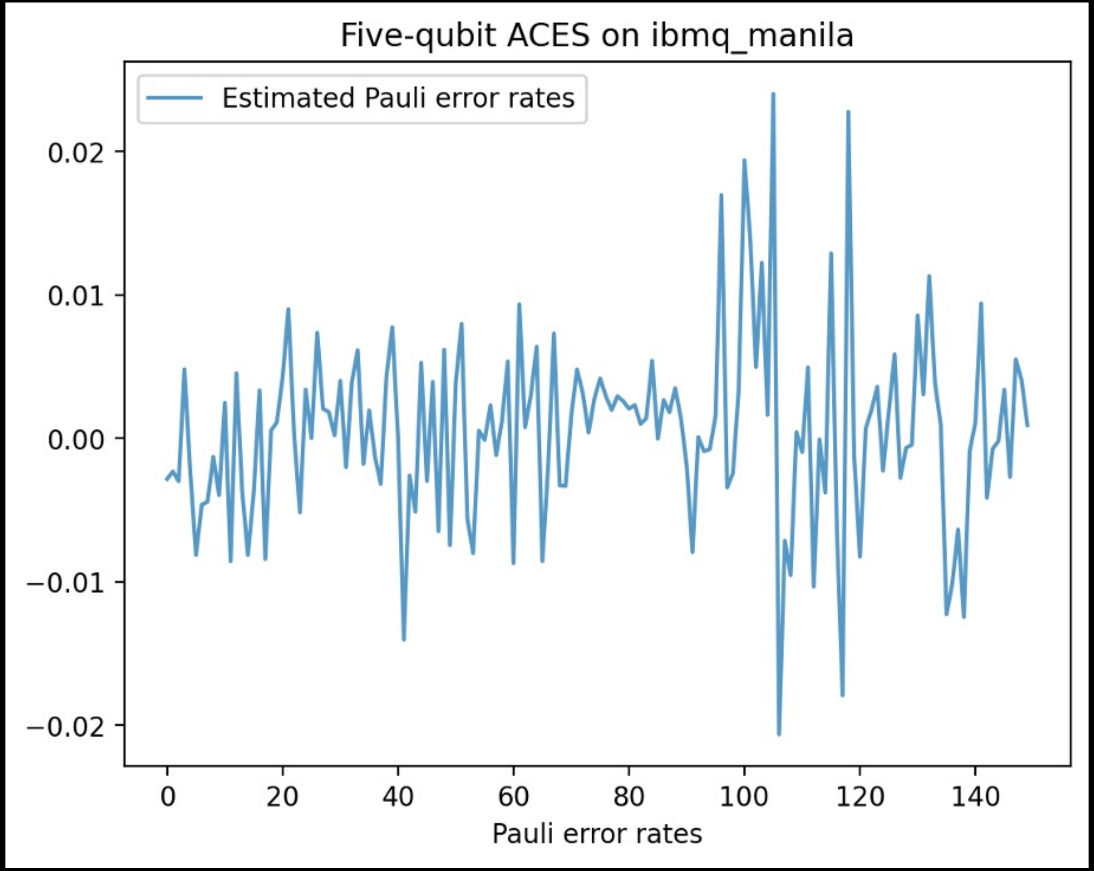




5-qubit IBMQ Manila

4 mirror + 6 random, 10 circuits, no twirls





Challenges and future directions

- We can **characterize** the Pauli error channel for each gate in a device.
  + With this, we can backtrack our output through the circuit and get a **more accurate result**.
- It is only **efficient** to backtrack (simulate) through Clifford circuits, which reduces the application scope of this protocol.
  + The original paper mentions that “ACES can accommodate circuits with a constant number of T gates in specific configurations” and “extending beyond this to universal gate sets in general is an important question for future research”.
  + Current work on expanding this protocol to **T + Clifford gatesets**.

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Feel free to reach out with any comments or feedback!