AVR496: Brushless DC Motor Control using ATtiny861

Features

- BLDC Motor Control in Sensor Mode
- Timer 1 Waveform Generator Use
- Hardware Implementation
- Code Example

References

[1] ATtiny261/461/861 data sheet

[2] AVR449: Sinusoidal driving of 3-phase permanent magnet motor using

ATtiny261/461/861

[3] AVR430: MC300 Hardware User Guide[4] AVR469: MC301 Hardware User Guide

1. Introduction

This application note describes how to implement a brushless DC motor control in sensor mode using the ATtiny861 AVR microcontroller.

The high performance AVR[®] core a long with the Timer 1 of the ATtiny861 allows to design high speed brushless DC motor applications.

In this document, we will give a short description of brushless DC motor theory of operations, we will detail how to control a brushless DC motor in sensor mode and we will also give a short description of the ATAVRMC301 and ATAVRMC300 boards used in this application note.

This application note deals only with BLDC motor control application using Hall effect position sensors to control commutation sequence.

2. Theory of Operations

Brushless DC motors are used in a growing number of motor applications as they have many advantages:

They have no brushes so they require little or no maintenance.

They generate less acoustic and electrical noise than universal brushed DC motors.

They can be used in hazardous operation environments (with flammable products).

They have a good weight/size to power ratio...



8-bit **AVR**® Microcontroller

Application Note







Such motors have a little rotor inertia. The coils are attached to the stator. The commutation is controlled by electronics. Commutation times are provided either by position sensors or by coils Back Electromotive Force measurements.

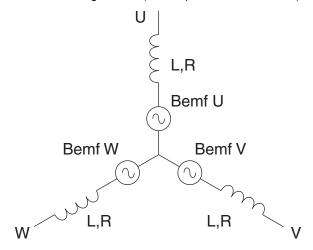
In sensor mode, Brushless DC motors usually consist of three main parts: a Stator, a Rotor and Hall Sensors.

2.1 Stator

A basic three phases BLDC motor Stator has three coils. In many motors, the number of coils is replicated to have a smaller torque ripple.

Figure 2-1 shows the electrical schematic of the stator. It consists of three coils each including three elements in series, an inductance, a resistance and one back electromotive force.

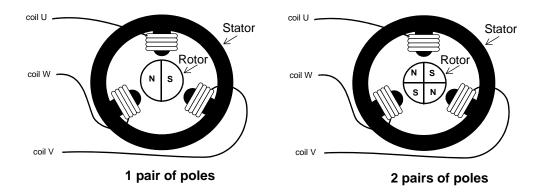
Figure 2-1. Stator Electrical Configuration (Three phases, three coils)



2.2 Rotor

The rotor in a BLDC motor consists of an even number of permanent magnets. The number of magnetic poles in the rotor also affects the step size and torque ripple of the motor. More poles give smaller steps and less torque ripple. The permanent magnets go from 1 to 5 pairs of poles. In certain cases it can go up to 8 pairs of poles. (Figure 2-2).

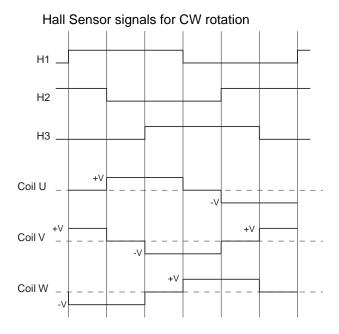
Figure 2-2. Three phase, three coil BLDC motor stator and rotor



2.3 Hall Sensor

Hall Sensors are placed every 120°. With these sensors, 6 different commutations are possible. Phase commutation depends on Hall Sensor values.

Power supply to the coils changes when Hall Sensor values change. With right synchronized commutations, the torque remains nearly constant and high.



2.4 Phase Commutations

To simplify the explanation of how to operate a three phases BLDC motor, a typical BLDC motor with only three coils is considered. As previously shown, phases commutation depends on the Hall Sensor values. When motor coils are correctly powered, a magnetic field is created and the rotor moves. The most elementary commutation driving method used for BLDC motors is an onoff scheme: a coil is either conducting or not conducting. Only two windings are powered at the same time and the third winding is floating. Connecting the coils to the power and neutral bus induces the current flow. This is referred to as trapezoidal commutation or block commutation.

To command brushless DC motors, a power stage made of 3 half bridges is used. Figure 2-4 below shows a 3 half bridge schematic.





Figure 2-4.

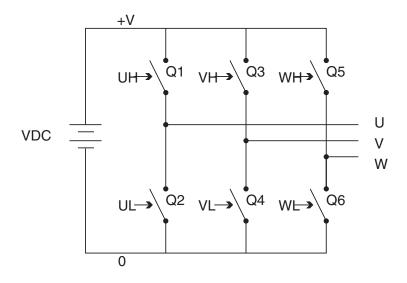


Table 2-1.

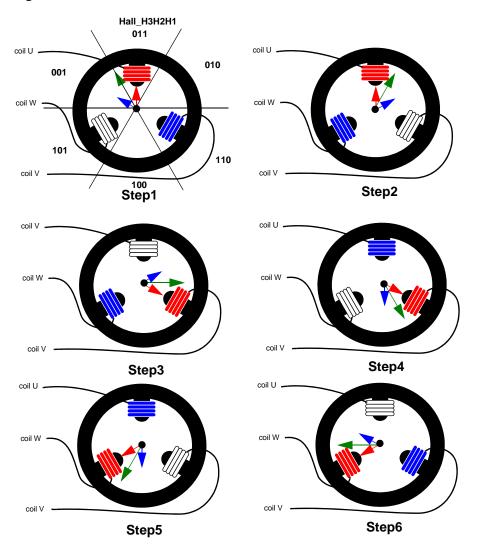
Hall Sensors Value (H3 H2 H1)	Phase	Switches
101	U-V	Q1 ; Q4
001	U-W	Q1 ; Q6
011	V-W	Q3 ; Q6
010	V-U	Q3 ; Q2
110	W-U	Q5 ; Q2
100	W-V	Q5 ; Q4

 $ElectricalFieldRotation = MecanicalRotation \times P(poles)$

2.5 Speed and Torque Control

current flow through the coils, the speed and torque of the motor can be adjusted. The most common way to control the current flow is to control the average current flow through the coils. The duty cycle of the PWM(Pulse Width Modulation) outputs are used to adjust the average voltage and thereby the average current, inducing the speed. To give an idea, the PWM frequency is chosen is the range from 10kHz to 200kHz according to the application (maximum of transistor switching frequency, electrical parameters of motors, commutation losses, audible frequency...)

Figure 2-5.



voltage by the switch Q1 and Phase V is connected by the switch Q4, Phase W is unpowered as the others swiches (Q2,Q3,Q5 and Q6) are opened. Two flux vectors are generated by phase U (red arrow) and phase V (blue arrow). The sum of the two vectors give the stator flux vector (green arrow). Then the rotor tries to follow the stator flux. As soon as the rotor reaches a given position, the Hall Sensors gives a new logical state of this position (from "010" to "011") and the next voltage pattern is selected and applied to the BLDC motor. Phase V is unpowered and Phase W is connected to the ground, resulting in a new stator flux vector 'Step2'.

The switching sequence described in schematic Figure 2-3 and Table 1, shows six different stator flux vectors corresponding to the six commutation steps. The six steps provide one electrical field rotation.





3. ATtiny861 microcontroller

3.1 Generating PWM signals with dead-time with ATtiny261/461/861

The Timer/Counter1 (TC1) module of the ATtinyX61 family is very well suited for driving three-phase motors. It can be run from a 64MHz PLL, and has a resolution of 10 bits. Six PWM outputs can be generated from this timer, grouped into three complementary output pairs with configurable dead-time. The "PWM6" mode is perfect for block commutation of brushless DC motors. For a maximum safety, a hardware fault protection unit can disable the PWM drivers without any intervention from the CPU.

To control a triple half-bridge driver stage, the "Phase and frequency correct PWM mode" of TC1 is used. In this mode, three pair of complementary PWM outputs with hardware dead-time insertion can be generated. This is exactly what is needed to generate three-phase sinusoidal drive waveforms with a triple half-bridge driver stage and chosen in the PWM generation.

The operation of one of the three complementary output pairs can be seen in Figure 3 2. The counter counts in an up-down counting mode. The OCR1x register specifies the current duty cycle. An intermediate waveform, labeled as OCW1x in the figure, is generated by clearing the output on a compare match when up-counting and setting the output on compare match when down-counting. This intermediate waveform feeds to the dead time generator, which in turn generates two outputs from this waveform. The non-inverted output, OC1x, follows OCW1x, except it will not go high until a specified dead-time period, DT1H, has elapsed after OCW1x goes high.

The inverted output, $\overline{OC1x}$, follows the inverted OCW1x signal, except it will not go high until a specified dead-time period, DT1L, has elapsed after OCW1x goes low. The result is a pair of complementary outputs with dead-time.

To control the duty cycle of one half-bridge, only one register, OCR1x needs to be changed. The average voltage output of the half-bridge will be proportional to this signal.

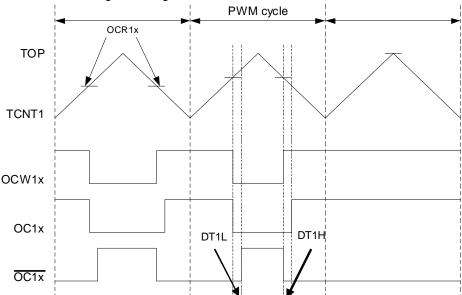


Figure 3-1. Generating PWM signals.

3.2 PWM base frequency

Timer/counter1 clock will be referred to as fCLK,T/C1 in the following.

The PWM frequency as a function of Timer/Counter1 clock frequency can be calculated from Figure 3-2.

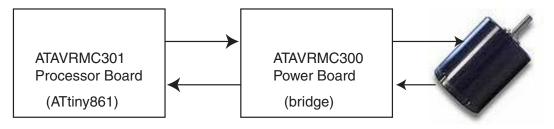
Figure 3-2. PWM base frequency as a function of timer clock frequency.

$$f_{PWM} = \frac{f_{CLK, T/(C1)}}{2 \cdot TOP - 2}$$

The PWM frequency with a Timer/Counter1 clock frequency of 64 MHz and 10 bit resolution is thus 31,28kHz.

4. Hardware Description

Figure 4-1. ATAVRMC301 & ATAVRMC300 connection



The power bridge (Q1 to Q6) is controlled through 6 signals UL, UH, VL, VH, WL, WH which are modulated by the PWM signal to adjust the motor DC voltage. See "Speed and Torque Control" on page 4.





Figure 4-2.

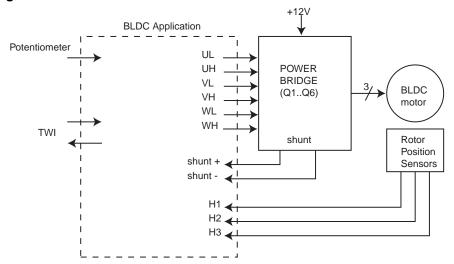
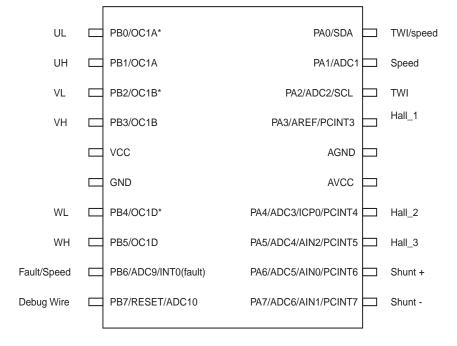


Figure 4-3.



5. Software Description

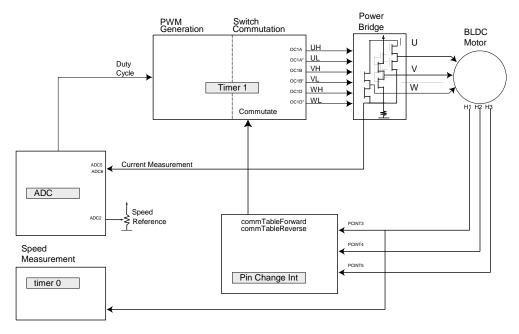
5.1 Preamble

And html documentation is delivered with the AVR496 software package. It can be opened thanks to the readme.html file located in the source directory.

main.c ushell_task.c USI_TWI_Slave.c

5.2 BLDC Motor Control Implementation

Figure 5-1.







5.3 Function description

```
void main(void):

void Commutate(void):

void SpeedMeasurement(void):

void PLLInit(void):

void PWMInit(void):

void HallSensorInit(void):

void ADCInit(void):

void PortsInit(void):

void TWInit(void):

underrupt void HallChangelSR():

interrupt void ADCISR():

void TimerOlnit(void):

interrupt void ovfl_timerO(void):
```

CPU & Memory usage

All measurements have been realized with Fosc = 8MHz. They also depend on the motor type (numbers of pair of poles). With a motor of 4 pairs of poles, Hall Sensor frequency is four times as high as the motor frequency.

All results in Figure 5-1 are obtained with a three-phase BLDC motor with four pairs of poles and a maximum speed of 6600 rpm. (Motor provided with the ATAVRMC300 kit).

Microcontroller utilization rate

Function	Parameters	Activation Time	Activation Period	Ratio CPU %
HallChangelSR()	Speed = 6600 rpm	10μS	380µS	2.7
ADCISR()	Speed = 6600 rpm	4µS	25µS	16

With the same conditions, the microcontroller memory usage is:

- 1332 bytes of CODE memory (Flash occupation = 17%).
 Including communication protocole through TWI
- 153 bytes of DATA memory (SRAM occupation = 30%).
 Including stack and communication protocole through TWI

ATAVRMC300 & ATAVRMC301 Configuration and Use

Table 6-1.

Jumper	Position	Comment
J1(VHa)	Pin1 & 2 shorted	VHa = +5V
J2(VCC)	Open	Vcc = +5V

ATAVRMC301 jumper settings

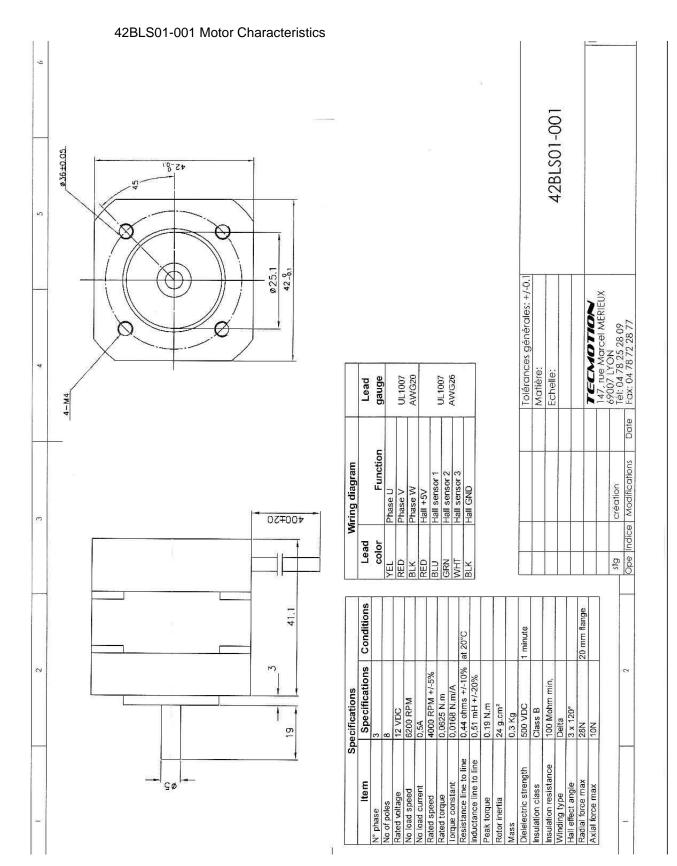
J. F 3-		
J8	Speed => Potentiometer SCL => TWI	Select speed reference
J9	All mounted	Connect PBO/PB1/PB2 to UL/UH/VL
J10	Not mounted	
J11	SH+	Connect Shunt+ to PA6
J12	SH-	Connect Shunt- to PA7
J13	Not mounted	
J15	H1	Connect H1 to PA1
J16	H2	Connect H2 to PA4
J17	H3	Connect H3 to PA5
J19	See Hardware User Guide	Select UVCC for USB stage

7. Conclusion

8. Appendix









Headquarters

Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131 USA

Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

International

Atmel Asia

Unit 1-5 & 16, 19/F BEA Tower, Millennium City 5 418 Kwun Tong Road Kwun Tong, Kowloon Hong Kong

Tel: (852) 2245-6100 Fax: (852) 2722-1369 Atmel Europe

Le Krebs 8, Rue Jean-Pierre Timbaud BP 309 78054 Saint-Quentin-en-

Yvelines Cedex France

Tel: (33) 1-30-60-70-00 Fax: (33) 1-30-60-71-11

Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033

Japan Tel: (81) 3-3523-3551

Fax: (81) 3-3523-7581

Product Contact

Web Site

Technical Support avr@atmel.com

Sales Contact

www.atmel.com/contacts

Literature Requests

Disclaimer: The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

© 2009 Atmel Corporation. All rights reserved. Atmel logo and combinations thereof, AVR® and others are registered trademarks or trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be trademarks of others.