# 1. Description

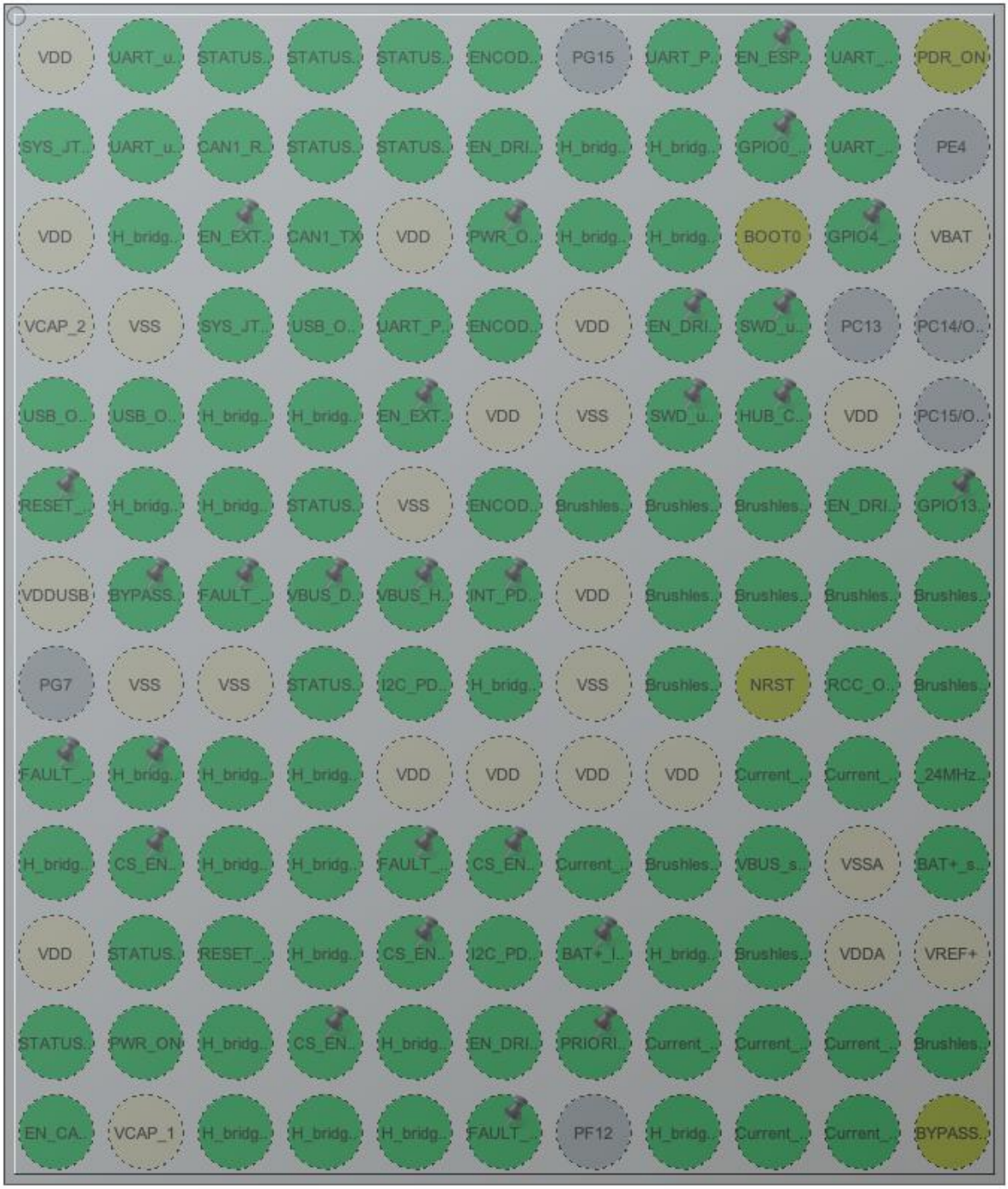
## 1.1. Project

| | |
|---|---|
| Project Name | Programmer_pinout_rev1 |
| Board Name | custom |
| Generated with: | STM32CubeMX 5.5.0 |
| Date | 07/27/2020 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F7 |
| MCU Line | STM32F7x6 |
| MCU name | STM32F746ZGYx |
| MCU Package | WLCSP143 |
| MCU Pin number | 143 |

## 2. Pinout Configuration



# 3. Pins Configuration

| Pin Number WLCSP143 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| A1 | VDD | Power | | |
| A2 | PC10 | I/O | USART3_TX | UART_uC_ESP_TX |
| A3 | PD2 * | I/O | GPIO_Output | STATUS_LED1_R |
| A4 | PD5 * | I/O | GPIO_Output | STATUS_LED2_R |
| A5 | PD7 * | I/O | GPIO_Output | STATUS_LED2_B |
| A6 | PG12 | I/O | SPI6_MISO | ENCODERS_GATE_DRIVERS |
| A8 | PB6 | I/O | USART1_TX | UART_PROG_ESP |
| A9 | PB8 * | I/O | GPIO_Output | EN_ESP32 |
| A10 | PE1 | I/O | UART8_TX | UART_CMD |
| A11 | PDR_ON | Reset | | |
| B1 | PA14 | I/O | SYS_JTCK-SWCLK | |
| B2 | PC11 | I/O | USART3_RX | UART_uC_ESP_RX |
| B3 | PD0 | I/O | CAN1_RX | |
| B4 | PD3 * | I/O | GPIO_Output | STATUS_LED1_G |
| B5 | PD4 * | I/O | GPIO_Output | STATUS_LED1_B |
| B6 | PG11 * | I/O | GPIO_Output | EN_DRIVER_3 |
| B7 | PB3 | I/O | TIM2_CH2 | H_bridge_mot2AN |
| B8 | PB7 | I/O | TIM4_CH2 | H_bridge_mot3BN |
| B9 | PB9 * | I/O | GPIO_Output | GPIO0_ESP32 |
| B10 | PE0 | I/O | UART8_RX | UART_CMD |
| C1 | VDD | Power | | |
| C2 | PA15 | I/O | TIM2_CH1 | H_bridge_mot2AP |
| C3 | PC12 * | I/O | GPIO_Output | EN_EXTENSION_TOP |
| C4 | PD1 | I/O | CAN1_TX | |
| C5 | VDD | Power | | |
| C6 | PG10 | I/O | GPIO_EXTI10 | PWR_ON_BTN_STATE_n |
| C7 | PB4 | I/O | TIM3_CH1 | H_bridge_mot2CP |
| C8 | PB5 | I/O | TIM3_CH2 | H_bridge_mot2CN |
| C9 | BOOT0 | Boot | | |
| C10 | PE3 * | I/O | GPIO_Output | GPIO4_ESP32 |
| C11 | VBAT | Power | | |
| D1 | VCAP_2 | Power | | |
| D2 | VSS | Power | | |
| D3 | PA13 | I/O | SYS_JTMS-SWDIO | |
| D4 | PA11 | I/O | USB_OTG_FS_DM | |

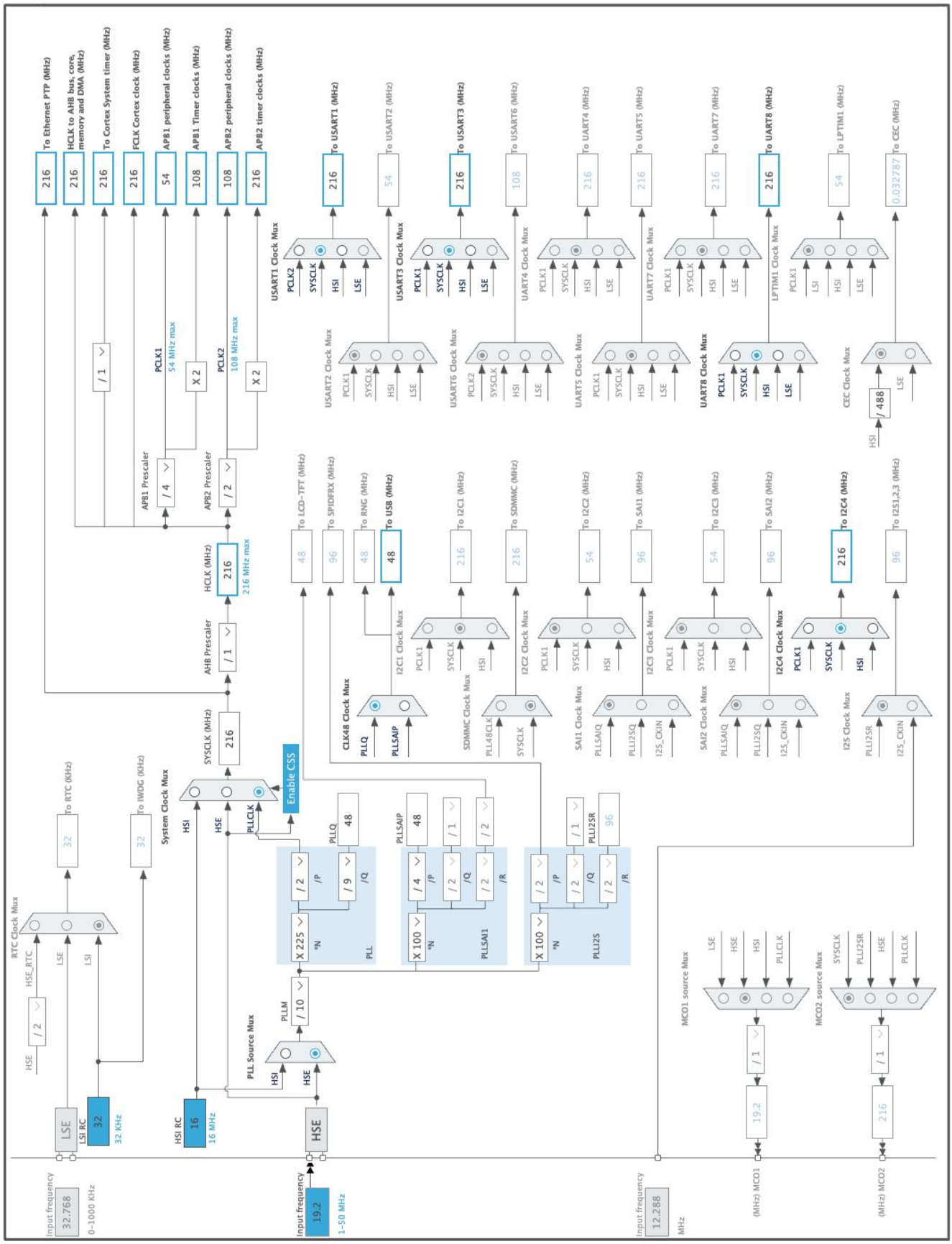
| Pin Number WLCSP143 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| D5 | PA10 | I/O | USART1_RX | UART_PROG_ESP |
| D6 | PG13 | I/O | SPI6_SCK | ENCODERS_GATE_DRIVERS |
| D7 | VDD | Power | | |
| D8 | PE2 * | I/O | GPIO_Output | EN_DRIVER_4 |
| D9 | PE5 * | I/O | GPIO_Output | SWD_uC_SWCLK |
| E1 | PA12 | I/O | USB_OTG_FS_DP | |
| E2 | PA9 | I/O | USB_OTG_FS_VBUS | |
| E3 | PC9 | I/O | TIM3_CH4 | H_bridge_mot3AN |
| E4 | PC8 | I/O | TIM8_CH3 | H_bridge_mot4CP |
| E5 | PG9 * | I/O | GPIO_Output | EN_EXTENSION_BOTTOM |
| E6 | VDD | Power | | |
| E7 | VSS | Power | | |
| E8 | PE6 * | I/O | GPIO_Output | SWD_uC_SWDIO |
| E9 | PF1 * | I/O | GPIO_Output | HUB_CONNECT |
| E10 | VDD | Power | | |
| F1 | PA8 * | I/O | GPIO_Output | RESET_HUB_n |
| F2 | PC6 | I/O | TIM8_CH1 | H_bridge_mot4AP |
| F3 | PC7 | I/O | TIM8_CH2 | H_bridge_mot4BP |
| F4 | PD6 * | I/O | GPIO_Output | STATUS_LED2_G |
| F5 | VSS | Power | | |
| F6 | PG14 | I/O | SPI6_MOSI | ENCODERS_GATE_DRIVERS |
| F7 | PF7 | I/O | ADC3_IN5 | Brushless_sense_mot1A |
| F8 | PF5 | I/O | ADC3_IN15 | Brushless_sense_mot1C |
| F9 | PF4 | I/O | ADC3_IN14 | Brushless_sense_mot1B |
| F10 | PF2 * | I/O | GPIO_Output | EN_DRIVER_2 |
| F11 | PF0 * | I/O | GPIO_Output | GPIO13_ESP32 |
| G1 | VDDUSB | Power | | |
| G2 | PG8 * | I/O | GPIO_Output | BYPASS_HUB_n |
| G3 | PG3 | I/O | GPIO_EXTI3 | FAULT_DRIVER_3_n |
| G4 | PG6 * | I/O | GPIO_Output | VBUS_DEVICES |
| G5 | PG4 | I/O | GPIO_EXTI4 | VBUS_HOST |
| G6 | PG5 | I/O | GPIO_EXTI5 | INT_PD_CTRL_n |
| G7 | VDD | Power | | |
| G8 | PF9 | I/O | ADC3_IN7 | Brushless_sense_mot2A |
| G9 | PF10 | I/O | ADC3_IN8 | Brushless_sense_mot2B |
| G10 | PF6 | I/O | ADC3_IN4 | Brushless_sense_mot3A |
| G11 | PF3 | I/O | ADC3_IN9 | Brushless_sense_mot3C |
| H2 | VSS | Power | | |

| Pin Number WLCSP143 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| H3 | VSS | Power | | |
| H4 | PD10 * | I/O | GPIO_Output | STATUS_LED3_B |
| H5 | PD13 | I/O | I2C4_SDA | I2C_PD_CONTROLLER |
| H6 | PD12 | I/O | TIM4_CH1 | H_bridge_mot3BP |
| H7 | VSS | Power | | |
| H8 | PC0 | I/O | ADC3_IN10 | Brushless_sense_mot2C |
| H9 | NRST | Reset | | |
| H10 | PH1/OSC_OUT | I/O | RCC_OSC_OUT | |
| H11 | PF8 | I/O | ADC3_IN6 | Brushless_sense_mot3B |
| J1 | PG2 | I/O | GPIO_EXTI2 | FAULT_DRIVER_4_n |
| J2 | PD14 | I/O | TIM4_CH3 | H_bridge_mot3CP |
| J3 | PB15 | I/O | TIM8_CH3N | H_bridge_mot4CN |
| J4 | PE10 | I/O | TIM1_CH2N | H_bridge_mot1BN |
| J5 | VDD | Power | | |
| J6 | VDD | Power | | |
| J7 | VDD | Power | | |
| J8 | VDD | Power | | |
| J9 | PC3 | I/O | ADC2_IN13 | Current_sense_mot1B |
| J10 | PC2 | I/O | ADC2_IN12 | Current_sense_mot1A |
| J11 | PH0/OSC_IN | I/O | RCC_OSC_IN | _24MHz_IN |
| K1 | PD15 | I/O | TIM4_CH4 | H_bridge_mot3CN |
| K2 | PD11 * | I/O | GPIO_Output | CS_ENCODER1_n |
| K3 | PB14 | I/O | TIM8_CH2N | H_bridge_mot4BN |
| K4 | PE11 | I/O | TIM1_CH2 | H_bridge_mot1BP |
| K5 | PG1 | I/O | GPIO_EXTI1 | FAULT_DRIVER_2_n |
| K6 | PF13 * | I/O | GPIO_Output | CS_ENCODER4_n |
| K7 | PB1 | I/O | ADC2_IN9 | Current_sense_mot4A |
| K8 | PA1 | I/O | ADC3_IN1 | Brushless_sense_mot4A |
| K9 | PA0/WKUP | I/O | ADC1_IN0 | VBUS_sense |
| K10 | VSSA | Power | | |
| K11 | PC1 | I/O | ADC1_IN11 | BAT+_sense |
| L1 | VDD | Power | | |
| L2 | PD8 * | I/O | GPIO_Output | STATUS_LED3_R |
| L3 | PE15 * | I/O | GPIO_Output | RESET_uC |
| L4 | PE12 | I/O | TIM1_CH3N | H_bridge_mot1CN |
| L5 | PE7 * | I/O | GPIO_Output | CS_ENCODER2_n |
| L6 | PF14 | I/O | I2C4_SCL | I2C_PD_CONTROLLER |
| L7 | PB2 * | I/O | GPIO_Output | BAT+_INRUSH_LIMIT_n |
| L8 | PA7 | I/O | TIM8_CH1N | H_bridge_mot4AN |

| Pin Number WLCSP143 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| L9 | PA2 | I/O | ADC3_IN2 | Brushless_sense_mot4B |
| L10 | VDDA | Power | | |
| L11 | VREF+ | Power | | |
| M1 | PD9 * | I/O | GPIO_Output | STATUS_LED3_G |
| M2 | PB12 * | I/O | GPIO_Output | PWR_ON |
| M3 | PB10 | I/O | TIM2_CH3 | H_bridge_mot2BP |
| M4 | PE14 * | I/O | GPIO_Output | CS_ENCODER3_n |
| M5 | PE8 | I/O | TIM1_CH1N | H_bridge_mot1AN |
| M6 | PF15 * | I/O | GPIO_Output | EN_DRIVER_1 |
| M7 | PF11 * | I/O | GPIO_Output | PRIORITY_TO_VBUS |
| M8 | PC4 | I/O | ADC2_IN14 | Current_sense_mot4B |
| M9 | PA5 | I/O | ADC2_IN5 | Current_sense_mot2B |
| M10 | PA4 | I/O | ADC2_IN4 | Current_sense_mot2A |
| M11 | PA3 | I/O | ADC3_IN3 | Brushless_sense_mot4C |
| N1 | PB13 * | I/O | GPIO_Output | EN_CAN_PROG_n |
| N2 | VCAP_1 | Power | | |
| N3 | PB11 | I/O | TIM2_CH4 | H_bridge_mot2BN |
| N4 | PE13 | I/O | TIM1_CH3 | H_bridge_mot1CP |
| N5 | PE9 | I/O | TIM1_CH1 | H_bridge_mot1AP |
| N6 | PG0 | I/O | GPIO_EXTI0 | FAULT_DRIVER_1_n |
| N8 | PB0 | I/O | TIM3_CH3 | H_bridge_mot3AP |
| N9 | PC5 | I/O | ADC2_IN15 | Current_sense_mot3B |
| N10 | PA6 | I/O | ADC2_IN6 | Current_sense_mot3A |
| N11 | BYPASS_REG | Reset | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | Programmer_pinout_rev1 |
| Project Folder | /Users/eliot/Documents/SmartGit/e-puck3-coreboard |
| Toolchain / IDE | EWARM V8 |
| Firmware Package Name and Version | STM32Cube FW_F7 V1.15.0 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy all used libraries into the project folder |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F7 |
| Line | STM32F7x6 |
| MCU | STM32F746ZGYx |
| Datasheet | 027590_Rev4 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

# 7. IPs and Middleware Configuration

## 7.1. ADC1

**mode: IN0**

**mode: IN11**

**mode: Temperature Sensor Channel**

**mode: Vrefint Channel**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 0 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. ADC2

**mode: IN4**

**mode: IN5**

**mode: IN6**

**mode: IN9**

**mode: IN12**
**mode: IN13**
**mode: IN14**
**mode: IN15**
### 7.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 4 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *7.3. ADC3*
**mode: IN1**
**mode: IN2**
**mode: IN3**
**mode: IN4**
**mode: IN5**
**mode: IN6**

### mode: IN7
### mode: IN8
### mode: IN9
### mode: IN10
### mode: IN14
### mode: IN15
### 7.3.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 4 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | **Channel 4 *** |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *7.4. CAN1*
### mode: Mode
### 7.4.1. Parameter Settings:

**Bit Timings Parameters:**

| | |
|---|---|
| Prescaler (for Time Quantum) | 16 |
| Time Quantum | |

| | |
|---|---|
| | **296.2962962962963 *** |
| Time Quanta in Bit Segment 1 | **5 Times *** |
| Time Quanta in Bit Segment 2 | **3 Times *** |
| ReSynchronization Jump Width | 1 Time |

**Basic Parameters:**

| | |
|---|---|
| Time Triggered Communication Mode | Disable |
| Automatic Bus-Off Management | Disable |
| Automatic Wake-Up Mode | Disable |
| No-Automatic Retransmission | Disable |
| Receive Fifo Locked Mode | Disable |
| Transmit Fifo Priority | Disable |

**Advanced Parameters:**

| | |
|---|---|
| Operating Mode | Normal |

## *7.5. GPIO*

## *7.6. I2C4*

### I2C: I2C

### 7.6.1. Parameter Settings:

**Timing configuration:**

| | |
|---|---|
| I2C Speed Mode | **Fast Mode Plus *** |
| I2C Speed Frequency (KHz) | 1000 |
| Rise Time (ns) | 0 |
| Fall Time (ns) | 0 |
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |
| Timing | **0x00A02B91 *** |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| General Call Address Detection | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |

## 7.7. RCC

### High Speed Clock (HSE): BYPASS Clock Source

### 7.7.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Flash Latency(WS) | 7 WS (8 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Over Drive | Enabled |
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 1 |

## 7.8. SPI6

### Mode: Full-Duplex Master

### 7.8.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | **16 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **54.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## 7.9. SYS

**Debug: Serial Wire**
**Timebase Source: SysTick**

## *7.10. TIM1*

**Trigger Source: ITR0**
**Clock Source : Internal Clock**
**Channel1: PWM Generation CH1 CH1N**
**Channel2: PWM Generation CH2 CH2N**
**Channel3: PWM Generation CH3 CH3N**

### 7.10.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 16 bits value) | 0 |
| auto-reload preload | Disable |
| Slave Mode Controller | Slave mode disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

**Break And Dead Time management - BRK Configuration:**

| | |
|---|---|
| BRK State | Disable |
| BRK Polarity | High |
| BRK Filter (4 bits value) | 0 |

**Break And Dead Time management - BRK2 Configuration:**

| | |
|---|---|
| BRK2 State | Disable |
| BRK2 Polarity | High |
| BRK2 Filter (4 bits value) | 0 |

**Break And Dead Time management - Output Configuration:**

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |
| Dead Time | 0 |

**PWM Generation Channel 1 and 1N:**

| | |
|---|---|
| Mode | PWM mode 1 |

| | |
|---|---|
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

**PWM Generation Channel 2 and 2N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

**PWM Generation Channel 3 and 3N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

## *7.11. TIM2*

**Slave Mode: Trigger Mode**
**Trigger Source: ITR0**
**Clock Source : Internal Clock**
**Channel1: PWM Generation CH1**
**Channel2: PWM Generation CH2**
**Channel3: PWM Generation CH3**
**Channel4: PWM Generation CH4**

### 7.11.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

| | |
|---|---|
| Slave Mode Controller | Trigger Mode |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (32 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.12. TIM3*

**Slave Mode: Trigger Mode**

**Trigger Source: ITR0**

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

### 7.12.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |

| | |
|---|---|
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |
| Slave Mode Controller | Trigger Mode |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.13. TIM4*

**Slave Mode: Trigger Mode**
**Trigger Source: ITR0**
**Clock Source : Internal Clock**
**Channel1: PWM Generation CH1**
**Channel2: PWM Generation CH2**
**Channel3: PWM Generation CH3**
**Channel4: PWM Generation CH4**

### 7.13.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |
| Slave Mode Controller | Trigger Mode |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**PWM Generation Channel 1:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 2:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 3:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

**PWM Generation Channel 4:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |

## *7.14. TIM8*

**Slave Mode: Trigger Mode**

**Trigger Source: ITR0**

**Clock Source : Internal Clock**

**Channel1: PWM Generation CH1 CH1N**

**Channel2: PWM Generation CH2 CH2N**

**Channel3: PWM Generation CH3 CH3N**

### 7.14.1. Parameter Settings:

### Counter Settings:

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| Repetition Counter (RCR - 16 bits value) | 0 |
| auto-reload preload | Disable |
| Slave Mode Controller | Trigger Mode |

### Trigger Output (TRGO) Parameters:

| | |
|---|---|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |
| Trigger Event Selection TRGO2 | Reset (UG bit from TIMx_EGR) |

### Break And Dead Time management - BRK Configuration:

| | |
|---|---|
| BRK State | Disable |
| BRK Polarity | High |
| BRK Filter (4 bits value) | 0 |

### Break And Dead Time management - BRK2 Configuration:

| | |
|---|---|
| BRK2 State | Disable |
| BRK2 Polarity | High |
| BRK2 Filter (4 bits value) | 0 |

### Break And Dead Time management - Output Configuration:

| | |
|---|---|
| Automatic Output State | Disable |
| Off State Selection for Run Mode (OSSR) | Disable |
| Off State Selection for Idle Mode (OSSI) | Disable |
| Lock Configuration | Off |
| Dead Time | 0 |

### PWM Generation Channel 1 and 1N:

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

### PWM Generation Channel 2 and 2N:

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |

| | |
|---|---|
| CH Idle State | Reset |
| CHN Idle State | Reset |

**PWM Generation Channel 3 and 3N:**

| | |
|---|---|
| Mode | PWM mode 1 |
| Pulse (16 bits value) | 0 |
| Fast Mode | Disable |
| CH Polarity | High |
| CHN Polarity | High |
| CH Idle State | Reset |
| CHN Idle State | Reset |

## *7.15. UART8*

### Mode: Asynchronous

### 7.15.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *7.16. USART1*

### Mode: Asynchronous

### 7.16.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *7.17. USART3*

**Mode: Asynchronous**

### 7.17.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |

| | |
|---|---|
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *7.18. USB_OTG_FS*

**Mode: Device_Only**

**mode: Activate_VBUS**

### 7.18.1. Parameter Settings:

| | |
|---|---|
| Speed | Full Speed 12MBit/s |
| Low power | Disabled |
| Link Power Management | Disabled |
| VBUS sensing | Enabled |
| Signal start of frame | Disabled |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA0/WKUP | ADC1_IN0 | Analog mode | No pull-up and no pull-down | n/a | VBUS_sense |
| | PC1 | ADC1_IN11 | Analog mode | No pull-up and no pull-down | n/a | BAT+_sense |
| ADC2 | PC3 | ADC2_IN13 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot1B |
| | PC2 | ADC2_IN12 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot1A |
| | PB1 | ADC2_IN9 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot4A |
| | PC4 | ADC2_IN14 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot4B |
| | PA5 | ADC2_IN5 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot2B |
| | PA4 | ADC2_IN4 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot2A |
| | PC5 | ADC2_IN15 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot3B |
| | PA6 | ADC2_IN6 | Analog mode | No pull-up and no pull-down | n/a | Current_sense_mot3A |
| ADC3 | PF7 | ADC3_IN5 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot1A |
| | PF5 | ADC3_IN15 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot1C |
| | PF4 | ADC3_IN14 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot1B |
| | PF9 | ADC3_IN7 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot2A |
| | PF10 | ADC3_IN8 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot2B |
| | PF6 | ADC3_IN4 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot3A |
| | PF3 | ADC3_IN9 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot3C |
| | PC0 | ADC3_IN10 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot2C |
| | PF8 | ADC3_IN6 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot3B |
| | PA1 | ADC3_IN1 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot4A |
| | PA2 | ADC3_IN2 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot4B |
| | PA3 | ADC3_IN3 | Analog mode | No pull-up and no pull-down | n/a | Brushless_sense_mot4C |
| CAN1 | PD0 | CAN1_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PD1 | CAN1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| I2C4 | PD13 | I2C4_SDA | Alternate Function Open Drain | Pull-up | **Very High *** | I2C_PD_CONTROLLER |
| | PF14 | I2C4_SCL | Alternate Function Open Drain | Pull-up | **Very High *** | I2C_PD_CONTROLLER |
| RCC | PH1/OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| | PH0/OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | _24MHz_IN |
| SPI6 | PG12 | SPI6_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** | ENCODERS_GATE_DRIVERS |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | | | | | * | |
| | PG13 | SPI6_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | ENCODERS_GATE_DRIVERS |
| | PG14 | SPI6_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | ENCODERS_GATE_DRIVERS |
| SYS | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| TIM1 | PE10 | TIM1_CH2N | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot1BN |
| | PE11 | TIM1_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot1BP |
| | PE12 | TIM1_CH3N | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot1CN |
| | PE8 | TIM1_CH1N | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot1AN |
| | PE13 | TIM1_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot1CP |
| | PE9 | TIM1_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot1AP |
| TIM2 | PB3 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot2AN |
| | PA15 | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot2AP |
| | PB10 | TIM2_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot2BP |
| | PB11 | TIM2_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot2BN |
| TIM3 | PB4 | TIM3_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot2CP |
| | PB5 | TIM3_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot2CN |
| | PC9 | TIM3_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot3AN |
| | PB0 | TIM3_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot3AP |
| TIM4 | PB7 | TIM4_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot3BN |
| | PD12 | TIM4_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot3BP |
| | PD14 | TIM4_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot3CP |
| | PD15 | TIM4_CH4 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot3CN |
| TIM8 | PC8 | TIM8_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot4CP |
| | PC6 | TIM8_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot4AP |
| | PC7 | TIM8_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot4BP |
| | PB15 | TIM8_CH3N | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot4CN |
| | PB14 | TIM8_CH2N | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot4BN |
| | PA7 | TIM8_CH1N | Alternate Function Push Pull | No pull-up and no pull-down | Low | H_bridge_mot4AN |
| UART8 | PE1 | UART8_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | UART_CMD |
| | PE0 | UART8_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | UART_CMD |
| USART1 | PB6 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High** * | UART_PROG_ESP |
| | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | | UART_PROG_ESP |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | | | | | **Very High *** | |
| USART3 | PC10 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | UART_uC_ESP_TX |
| | PC11 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | UART_uC_ESP_RX |
| USB_OTG_FS | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA9 | USB_OTG_FS_VBUS | Input mode | No pull-up and no pull-down | **n/a** | |
| GPIO | PD2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED1_R |
| | PD5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED2_R |
| | PD7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED2_B |
| | PB8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_ESP32 |
| | PD3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED1_G |
| | PD4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED1_B |
| | PG11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_DRIVER_3 |
| | PB9 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | GPIO0_ESP32 |
| | PC12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_EXTENSION_TOP |
| | PG10 | GPIO_EXTI10 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | PWR_ON_BTN_STATE_n |
| | PE3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | GPIO4_ESP32 |
| | PE2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_DRIVER_4 |
| | PE5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | SWD_uC_SWCLK |
| | PG9 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_EXTENSION_BOTTOM |
| | PE6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | SWD_uC_SWDIO |
| | PF1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | HUB_CONNECT |
| | PA8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | RESET_HUB_n |
| | PD6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED2_G |
| | PF2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_DRIVER_2 |
| | PF0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | GPIO13_ESP32 |
| | PG8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BYPASS_HUB_n |
| | PG3 | GPIO_EXTI3 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | FAULT_DRIVER_3_n |
| | PG6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | VBUS_DEVICES |
| | PG4 | GPIO_EXTI4 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | VBUS_HOST |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | PG5 | GPIO_EXTI5 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | INT_PD_CTRL_n |
| | PD10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED3_B |
| | PG2 | GPIO_EXTI2 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | FAULT_DRIVER_4_n |
| | PD11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | CS_ENCODER1_n |
| | PG1 | GPIO_EXTI1 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | FAULT_DRIVER_2_n |
| | PF13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | CS_ENCODER4_n |
| | PD8 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED3_R |
| | PE15 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | RESET_uC |
| | PE7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | CS_ENCODER2_n |
| | PB2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | BAT+_INRUSH_LIMIT_n |
| | PD9 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | STATUS_LED3_G |
| | PB12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PWR_ON |
| | PE14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | CS_ENCODER3_n |
| | PF15 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_DRIVER_1 |
| | PF11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | PRIORITY_TO_VBUS |
| | PB13 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | EN_CAN_PROG_n |
| | PG0 | GPIO_EXTI0 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | FAULT_DRIVER_1_n |

## 8.2. DMA configuration

| DMA request | Stream | Direction | Priority |
|---|---|---|---|
| ADC1 | DMA2_Stream0 | Peripheral To Memory | Low |
| ADC2 | DMA2_Stream3 | Peripheral To Memory | Low |
| ADC3 | DMA2_Stream1 | Peripheral To Memory | Low |
| SPI6_RX | DMA2_Stream6 | Peripheral To Memory | Low |
| SPI6_TX | DMA2_Stream5 | Memory To Peripheral | Low |
| UART8_RX | DMA1_Stream6 | Peripheral To Memory | Low |
| UART8_TX | DMA1_Stream0 | Memory To Peripheral | Low |
| USART3_RX | DMA1_Stream1 | Peripheral To Memory | Low |
| USART3_TX | DMA1_Stream4 | Memory To Peripheral | Low |
| I2C4_RX | DMA1_Stream2 | Peripheral To Memory | Low |
| I2C4_TX | DMA1_Stream5 | Memory To Peripheral | Low |
| USART1_RX | DMA2_Stream2 | Peripheral To Memory | Low |
| USART1_TX | DMA2_Stream7 | Memory To Peripheral | Low |

### *ADC1: DMA2_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *ADC2: DMA2_Stream3 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *ADC3: DMA2_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |

| | |
|---|---|
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Half Word |
| Memory Data Width: | Half Word |

### *SPI6_RX: DMA2_Stream6 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Byte *** |
| Memory Data Width: | **Byte *** |

### *SPI6_TX: DMA2_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | **Byte *** |
| Memory Data Width: | **Byte *** |

### *UART8_RX: DMA1_Stream6 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *UART8_TX: DMA1_Stream0 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART3_RX: DMA1_Stream1 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART3_TX: DMA1_Stream4 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*I2C4_RX: DMA1_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*I2C4_TX: DMA1_Stream5 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

*USART1_RX: DMA2_Stream2 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

### *USART1_TX: DMA2_Stream7 DMA request Settings:*

| | |
|---|---|
| Mode: | Normal |
| Use fifo: | Disable |
| Peripheral Increment: | Disable |
| Memory Increment: | **Enable *** |
| Peripheral Data Width: | Byte |
| Memory Data Width: | Byte |

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| DMA1 stream0 global interrupt | true | 0 | 0 |
| DMA1 stream1 global interrupt | true | 0 | 0 |
| DMA1 stream2 global interrupt | true | 0 | 0 |
| DMA1 stream4 global interrupt | true | 0 | 0 |
| DMA1 stream5 global interrupt | true | 0 | 0 |
| DMA1 stream6 global interrupt | true | 0 | 0 |
| DMA2 stream0 global interrupt | true | 0 | 0 |
| DMA2 stream1 global interrupt | true | 0 | 0 |
| DMA2 stream2 global interrupt | true | 0 | 0 |
| DMA2 stream3 global interrupt | true | 0 | 0 |
| DMA2 stream5 global interrupt | true | 0 | 0 |
| DMA2 stream6 global interrupt | true | 0 | 0 |
| DMA2 stream7 global interrupt | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| EXTI line0 interrupt | unused | | |
| EXTI line1 interrupt | unused | | |
| EXTI line2 interrupt | unused | | |
| EXTI line3 interrupt | unused | | |
| EXTI line4 interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| CAN1 TX interrupts | unused | | |
| CAN1 RX0 interrupts | unused | | |
| CAN1 RX1 interrupt | unused | | |
| CAN1 SCE interrupt | unused | | |
| EXTI line[9:5] interrupts | unused | | |
| TIM1 break interrupt and TIM9 global interrupt | unused | | |
| TIM1 update interrupt and TIM10 global interrupt | unused | | |
| | | | |

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| TIM1 trigger and commutation interrupts and TIM11 global interrupt | unused | | |
| TIM1 capture compare interrupt | unused | | |
| TIM2 global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| TIM4 global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| USART3 global interrupt | unused | | |
| EXTI line[15:10] interrupts | unused | | |
| TIM8 break interrupt and TIM12 global interrupt | unused | | |
| TIM8 update interrupt and TIM13 global interrupt | unused | | |
| TIM8 trigger and commutation interrupts and TIM14 global interrupt | unused | | |
| TIM8 capture compare interrupt | unused | | |
| USB On The Go FS global interrupt | unused | | |
| FPU global interrupt | unused | | |
| UART8 global interrupt | unused | | |
| SPI6 global interrupt | unused | | |
| I2C4 event interrupt | unused | | |
| I2C4 error interrupt | unused | | |

*** User modified value**

# 9. Software Pack Report