SIS3153
USB3/Ethernet VME Interface

User Manual

SIS GmbH
Harksheider Str. 102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

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Revision	Date	Modification
1.00	25.10.2013	First official release
1.01	29.10.2013	Minor touch up
1.02	26.11.2014	Hardware version 2 - FX3 boot mode added
1.03	01.12.2014	Software section, minor touch up
1.04	21.01.2015	USB cable length appendix
1.05	08.09.2015	Description of Switch 162-3: Link Led L (USB or Ethernet)
1.06	19.03.2018	P1/P2 schematic added

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1 Introduction

The SIS3153 USB3.0/Ethernet to VME interface is a single width 6U VME card.

Photograph of SIS3153

As we are aware, that no manual is perfect, we appreciate your feedback and will incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de.
Feel free to apply for an account for our Dokuwiki documentation web page also.

The SIS3153 firmware page is at www.struck.de/sis3153firm.html .

Information on SIS3153 applications, firmware news and other related issues will be posted on our DAQ blog at www.struck.de/blog also.

2 Functionality

The SIS3153 interfaces the popular Universal Serial Bus (USB) and Ethernet to the VMEbus. It uses the Cypress Semiconductor Corporation FX3 chip as USB3.0 host controller. The modules functionality comprises:

- Ethernet (UDP) connectivity (Described in 'SIS3153 - Ethernet Addendum')

- USB3.0 / Superspeed USB functionality
- USB2.0 and USB1.1 compliance
- VME master read cycles:
  - IACK, A16/A24/A32
  - D8/D16/D32/BLT32/MBLT64/2eVME/2eSST160/2eSST267/2eSST320
- VME master write cycles:
  - A16/A24/A32
  - D8/D16/D32/BLT32/MBLT64/2eVME
- VME slave; not implemented yet
- 2 digital front panel inputs (NIM or TTL level, select by jumper or register bits)
- 2 digital front panel outputs (NIM or TTL level , select by jumper or register bits)

Possible future firmware extensions comprise

- Optical connectivity

Note: A Gigabit 1000BASE-T copper SFP transceiver (Finisar FCLF-8520-3 or compatible, Struck part number 04333) is required for Ethernet operation. The transceiver is included with the SIS3153 if the card is ordered for Ethernet to VME Interface operation (Struck part number 05867).

3 USB device

The SIS3153USB device (USB peripheral) is hotplugging.

The SIS3153USB device in combination with the drivers supports access to following spaces.

- SIS3153 USB register space
- VME Bus

3.1 SIS3153 USB Register space

The driver offers the following calls:

```
int sis3153Usb_Register_Single_Read(HANDLE usbDevice,
                                    ULONG addr, ULONG* data) ;

int sis3153Usb_Register_Dma_Read(HANDLE usbDevice,
                                 ULONG addr, ULONG* dmabufs,
                                 ULONG req_nof_data, ULONG* got_nof_data) ;

int sis3153Usb_Register_Single_Write(HANDLE usbDevice,
                                     ULONG addr, ULONG data) ;

int sis3153Usb_Register_Dma_Write(HANDLE usbDevice,
                                  ULONG addr, ULONG* dmabufs,
                                  ULONG req_nof_data, ULONG* put_nof_data);
```

3.1.1 USB Register Space Address Map

Offset	R/W	Function/Register
0x0	R/W	USB Control/Status register
0x1	R	Module Id. and firmware version register
0x2	R	Serial Number register
0x3	R/W	LEMO IO control register
0x4	R/W	UDP protocol configuration register
0x10	R/W	USB VME Master Status/Control register
0x11	R	USB VME Master Cycle Status Register
0x12	R	USB VME Interrupt Status Register
0x100	KA	Key reset all
0x 0000 1000 .. 0x 0000 1FFF	R/W	Internal RAM
0x 0010 0000 .. 0x 001F FFFF	R	USB Address/Data Test space: Read Data = Read Address
0x 0020 0000 .. 0x 002F FFFF	R	USB Speed Test space: Read Data = Speed Counter The Speed Counter increments every 8ns (125 MHz)

The shorthand KA stands for key address. Write access with arbitrary data to a key address initiates the specified function

3.2 USB Register description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3153_CONTROL_STATUS       0x0
```

refers to the sis3153usb.h header file.

3.2.1 USB Control/Status Register(write/read)

```
#define SIS3153USB_CONTROL_STATUS         0x0
```

The control register is in charge of the control of some basic properties of the SIS3153 board, like enabling Led test mode. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.

On read access the same register represents the status register.

Bit	write Function	read Function
31	reserved	0
30	reserved	0
29	reserved	USB speed flag bit 1
28	reserved	USB speed flag bit 0
27	reserved	0
26	reserved	0
25	reserved	0
24	reserved	0
23	reserved	0
22	reserved	0
21	reserved	0
20	Clear SPI-Flash interface reset (*)	0
19	Clear USB internal access control bit 1 (*)	0
18	Clear USB internal access control bit 0 (*)	0
17	Clear Led test mode (*)	0
16	Switch off LED A (*)	0
15	reserved	Status reserved
..	..	..
6	..	..
5	reserved	Status reserved
4	Set SPI-Flash interface reset	Status SPI-Flash interface reset
3	Set USB internal access control bit 1	Status USB internal access control bit 1
2	Set USB internal access control bit 0	Status USB internal access control bit 0
1	Set Led test mode	Status Led test mode
0	Switch on LED A	Status User LED A (1=LED on, 0=LED off)

(*) denotes power up default setting, i.e. the power up reading of the register is 0x0

USB internal access control bits:

Bit 1	Bit 0	Internal read speed to USB3 controller
0	0	16 ns / 32-bit word
0	1	8 ns / 32-bit word
1	0	1 us / 32-bit word
1	1	reserved

This feature is used for test purposes only.

3.2.2 Module Id. and Firmware Revision Register (read)

```
#define SIS3153USB_MODID_VERSION                    0x1
```

This register reflects the module identification of the SIS3153USB and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	1
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	5
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	3
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

Major revision number	Application/user
0x01	Generic SIS3153USB design (internal 32-bit interface support)
0x16	Generic SIS3153USB design (internal 16-bit interface support)

3.2.3 Serial Number register

```
#define SIS3153USB_SERIAL_NUMBER_REG            0x2
```

This register holds the Serial Number of the module.

BIT	access	Name	Function
31-17 FFFE0000	RO	reserved	
16 00010000	RO	Serial Number Not Valid Flag	0: valid 1: not valid
15-0 0000FFFF	RO	Serial Number	1..65535

Note: The Ethernet MAC address is 00-00-56-15-3n-nn (n-nn is the Serial Number)

3.2.4 LEMO IO control register

```
#define SIS3153USB_LEMO_IO_CTRL_REG            0x3
```

The register is implemented in a J/K fashion also and allows to check the status of the logic level setting of the front panel inputs and outputs. In addition it can be used to control the levels by software. Please note, that the actual control over the status of the inputs and outputs is controlled via the LEMO I/O register

Bit	Write Function	Read Function/value
31	Disable Software Level Control (*)	0
30	reserved	0
29	reserved	0
28	reserved	0
27	reserved	0
26	reserved	0
25	reserved	0
24	reserved	0
23	Clear output 2 latch (*)	Status of input 2 latch
22	Clear output 1 latch (*)	Status of input 1 latch
21	Clear output 2 (*)	Status of input 2
20	Clear output 1 (*)	Status of input 1
19	Set input 2 to NIM level (*)	0
18	Set input 1 to NIM level (*)	0
17	Set output 2 to NIM level (*)	0
16	Set output 1 to NIM level (*)	0
15	Enable Software Level Control	Status Software Level Control
14	reserved	Status of reserved
13	reserved	Status of reserved
12	reserved	Status of reserved
11	reserved	Status of reserved
10	reserved	Status of reserved
9	reserved	Status of reserved
8	reserved	Status of reserved
7	Generate output pulse 2	0
6	Generate output pulse 1	0
5	Set output 2	Status of output 2
4	Set output 1	Status of output 1
3	Set input 2 to TTL level	Status of level input 2 (0=NIM, 1=TTL)
2	Set input 1 to TTL level	Status of level input 1 (0=NIM, 1=TTL)
1	Set output 2 to TTL level	Status of level output 2 (0=NIM, 1=TTL)
0	Set output 1 to TTL level	Status of level output 1 (0=NIM, 1=TTL)

The power up value is 0x00000000 (with the I/Os jumper configured to NIM level)

(*) denotes the power up default setting
Note 1: Enable software control by setting bit 15 to gain software control over the logic levels of the I/Os. By default the level is defined by jumpers JP123 and JP133.

Note 2: for the typical application it will be good enough to set the logic levels to the desired levels in hardware by setting JP123 and JP133 accordingly.

3.2.5 UDP protocol configuration register

```
#define SIS3153_UDP_PROTOCOL_CONFIG      0x4         /* read/write; D32 */
```

This register is used to control the UDP data packets. The setup of the ethernet interface is described in detail in 'SIS3153USB - Ethernet UDP Addendum'.

Bit	31 - 9	8	7 - 5	4	3 - 0
Function	reserved	UDP transmit Data packet format bit	reserved	UDP transmit jumbo Packet enable bit	UDP transmit packet gap bits

UDP transmit packet gap value	Gap time between UDP packets
0	256 ns
1	512 ns
2	1 us
3	2 us
4	4 us
5	8 us
6	10 us
7	12 us
8	14 us
9	16 us
0xA	20 us
0xB	28 us
0xC	32 us
0xD	41 us
0xE	50 us
0xF	57 us

The power up default value reads 0x 00000000

3.2.6 USB VME Master Status/Control register (read/write)

```
#define SIS3153USB_VME_MASTER_CONTROL_STATUS          0x10
```

The control register is in charge of the control of most of the basic properties of the SIS3153 board in write access. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.

Bit	Write Function	Read Function
31	Clear SYSTEM VME BERR TIMER BIT1	0
30	Clear SYSTEM VME BERR TIMER BIT0	0
29	Clear LONG TIMER BIT1	0
28	Clear LONG TIMER BIT0	0
27	no function	0
26	Clear Force Dearbit	0
25	no function	0
24	Disable VME retry	0
23	no function	0
22	Clear VME REQUESTER TYPE BIT	0
21	Clear VME_REQ_LEVEL BIT1	0
20	Clear VME_REQ_LEVEL BIT0	0
19	no function	0
18	no function	0
17	Clear VME_SYSRESET bit	0
16	Clear VME System Controller Enable bit	Status VME System Controller (*2)
15	Set SYSTEM VME BERR TIMER BIT1	Status SYSTEM VME BERR TIMER BIT1
14	Set SYSTEM VME BERR TIMER BIT0	Status SYSTEM VME BERR TIMER BIT0
13	Set LONG TIMER BIT1	Status LONG TIMER BIT1
12	Set LONG TIMER BIT0	Status LONG TIMER BIT0
11	no function	0
10	Set Force Dearbit (*5)	Status Force Dearbit Enable bit
9	no function	0
8	Enable VME retry (*4)	Status VME retry Enable bit
7	no function	0
6	Set VME REQUESTER TYPE BIT	Status VME REQUESTER TYPE BIT
5	Set VME_REQ_LEVEL BIT1	Status VME_REQ_LEVEL BIT1
4	Set VME_REQ_LEVEL BIT0	Status VME_REQ_LEVEL BIT0
3	no function	0
2	no function	0
1	Set VME_SYSRESET bit (*3)	Status VME_SYSRESET bit
0	Set VME System Controller Enable bit (*1)	Status VME System Controller Enable bit

The power up value is 0x0000C100 (or 0x0001C100 with system controller set)

Notes:

(*1) is ored with switch 5 of SW162; Caution: if the jumper is not installed and the VME system controller functionality is enabled by software, the 16 MHz clock is not active during power up. This may result in problems with peculiar VME slave designs that use the VME clock to initialise on board logic.

(*2) is set with switch 5 of SW162 on or if VME System Controller Enable bit is set

(*3) if Switch SW162-7 is ON and VME_SYSRESET bit is set then VME_SYSRESET is issued

(*4) A retry error (error code 0x212) may be caused by older VME backplanes, which do not properly terminate this previously reserved (pin B3 on connector P2) if retry is enabled. Retry can be disabled by setting bit 24. Retry had to be activated by setting bit 8 on the SIS3153, this behaviour is not compatible with SST transfers.

(*5) Setting bit 10 causes the SIS3153 to release busy for 170 ns in between of blockletts during a block transfer. This gives another master the possibility to gain busmastership during the block transfer. The SIS3153 will terminate the block transfer with an arbitration timeout if the other master does not release busmastership within the long timer period. The AS-AS gap of 90 ns will be extended by the 170 ns release period, i.e. the reduction in transfer speed is negligible.

Explanation/function of bit combinations:

SYSTEM VME BERR TIMER BIT1	SYSTEM VME BERR TIMER BIT0	VME Bus Error after
0	0	1,25 µs
0	1	6,25 µs
1	0	12,5 µs
1	1	100 µs (default)

Note: The default value of 1,25 µs will be fine with most of VME slaves on the market, there are peculiar cards which will respond to a VME cycle much slower however also. The bus error code is 0x211.

LONG TIMER BIT1	LONG TIMER BIT0	LONG Timeout after
0	0	1 ms (default)
0	1	10 ms
1	0	50 ms
1	1	200 ms

LONG Timeout: arbitration timeout, no reply from current VME master or VME bus mastership not granted
The arbitration timeout error code is ox214.

VME_REQ_LEVEL BIT1	VME_REQ_LEVEL BIT0	VME Bus Request Level
0	0	BR3 (highest Level, default)
0	1	BR2
1	0	BR1
1	1	BR0

VME REQUESTER TYPE BIT	VME Bus Requester Type
0	Release when Done (default)
1	Release on Request

3.2.7 USB VME Master Cycle Status

```
#define SIS3153USB_VME_MASTER_CYCLE_STATUS          0x11
```

This register contains status information for the last VME Cycle.

D31 D16	D15 D0
VME Cycle Error Register	VME Write Transfer Byte Count Register

VME Cycle Error Codes:

- 0x100 Timeout
- 0x110 USB Protocol Error: invalid parameter
- 0x111 USB Protocol Error: USB write error
- 0x112 USB Protocol Error: USB read error
- 0x113 USB Protocol Error: USB read length error

- 0x211 VME Bus Error
- 0x212 VME_RETRY_ERROR
- 0x214 VME Arbitration Timeout

Note: The 0x100 timeout error occurs if the VME master logic is "dead" for one second. This situation can occur if the VME slave generates DTACK_L in a fashion that violates the VME specification. The timeout error does not occur with properly working VME slave hardware.

3.2.8 USB VME Interrupt Status Register

```
#define SIS3153USB_VME_INTERRUPT_STATUS        0x12
```

This register reflects the status of the VME IRQ lines. It can be used to check on the occurrence of a VME interrupt.

Bit	Function
31	0
..	..
20	0
19	Test: set IRQ
..	Test: IRQ level 2
..	Test: IRQ level 1
16	Test: IRQ level 0
15	
..	..
8	0
7	Status VME IRQ 7 on VME BUS
6	Status VME IRQ 6 on VME BUS
5	Status VME IRQ 5 on VME BUS
4	Status VME IRQ 4 on VME BUS
3	Status VME IRQ 3 on VME BUS
2	Status VME IRQ 2 on VME BUS
1	Status VME IRQ 1 on VME BUS
0	0

Note:
To create an IACK cycle you have to execute a D8 VME read cycle with AM=0x4000 from the address defined by (irq_level<<1)+1.. The read returns the interrupt vector as datum.

Examples:
VME IRQ level = 1 -> address = 3
VME IRQ level = 4 -> address = 9
VME IRQ level = 6 -> address = 0xd

3.3 VME Bus

The Windows driver offers the following calls:

```
int EXPORT sis3153Usb_Vme_Single_Read(HANDLE usbDevice,
                                      ULONG addr,
                                      ULONG am,
                                      ULONG size,
                                      ULONG* data) ;

int EXPORT sis3153Usb_Vme_Dma_Read(HANDLE usbDevice,
                                   ULONG addr,
                                   ULONG am,
                                   ULONG size,
                                   ULONG fifo_mode,
                                   ULONG* dmabufs,
                                   ULONG req_nof_data,
                                   ULONG* got_nof_data) ;
```

Note: req_nof_data and got_nof_data are counted in longwords

```
int EXPORT sis3153Usb_Vme_Single_Write(HANDLE usbDevice,
                                       ULONG addr,
                                       ULONG am,
                                       ULONG size,
                                       ULONG data);

int EXPORT sis3153Usb_Vme_Dma_Write(HANDLE usbDevice,
                                    ULONG addr,
                                    ULONG am,
                                    ULONG size,
                                    ULONG fifo_mode,
                                    ULONG* dmabufs,
                                    ULONG req_nof_data,
                                    ULONG* put_nof_data);
```

Not all combinations of the parameters are possible and allowed.
All supported VME cycles are defined in the include file
..\sis3153usb_vme_win_utils\sis3153usb_calls\ sis3153usb_vme_calls.h.

Examples:

```
int vme_A32D32_read(HANDLE  hXDev,
                    u_int32_t vme_adr,
                    u_int32_t* vme_data ) ;

int vme_A32MBLT64_read(HANDLE  hXDev,
                       u_int32_t vme_adr,
                       u_int32_t* vme_data,
                       u_int32_t req_num_of_lwords,
                       u_int32_t* got_no_of_lwords) ;
```

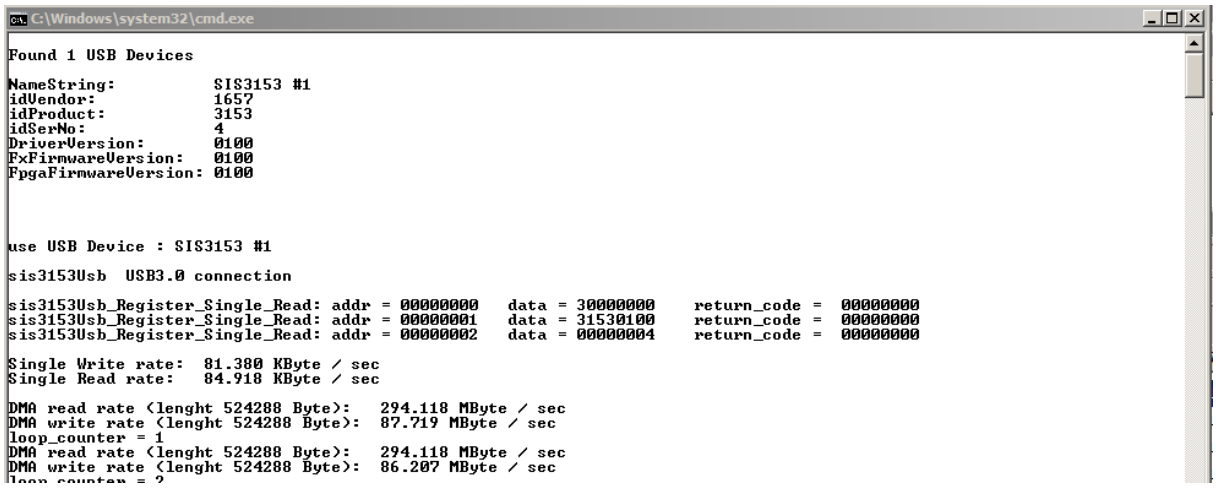
Note: `req_num_of_lwords` and `got_no_of_lwords` are counted in longwords

4 USB – SIS3153 Transfer Data Rate

The following transfer data rates were measured with a Siemens Fujitsu Celsius W420 PC (3.4 GHz i7-3770 CPU) running under Windows 7 Professional.

4.1 USB – SIS3153 Internal Space Data Rate

	appr. continuous Data Rate			
	Single Data Write	DMA Block Write	Single Data Read	DMA Block Read
USB2.0	15 KByte/sec	20 MByte/sec	15 KByte/sec	40 MByte/sec
USB3.0	82 KByte/sec	87 MByte/sec	84 KByte/sec	294 MByte/sec



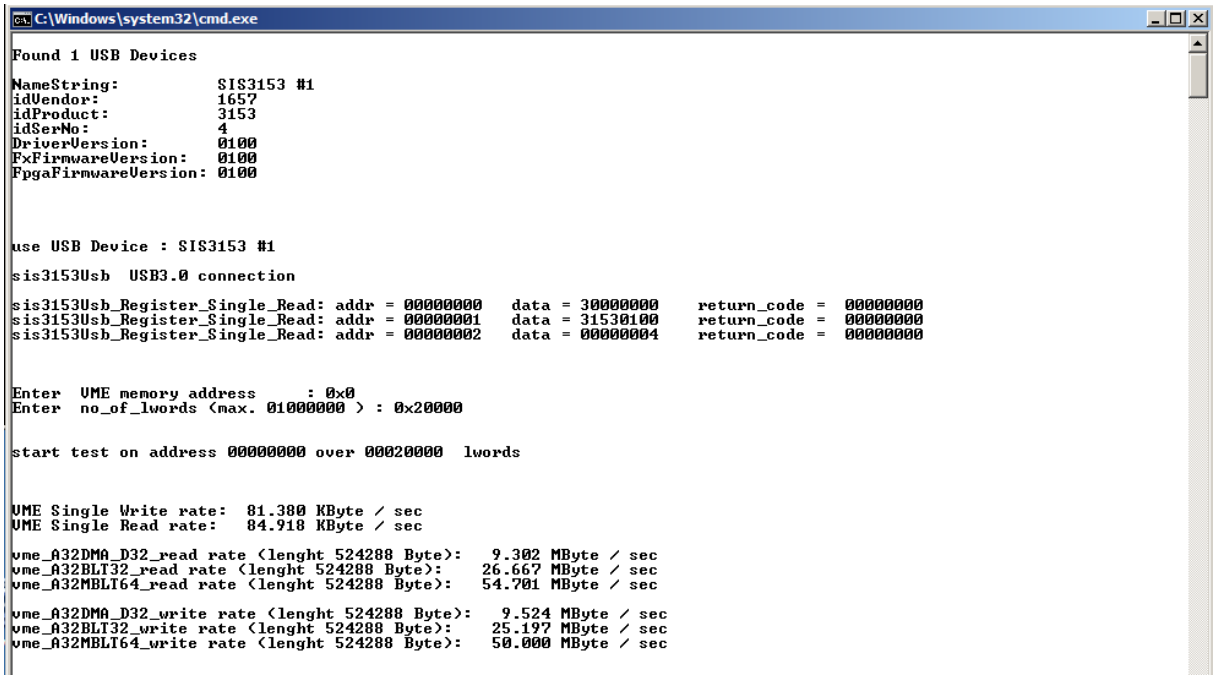
4.2 USB – SIS3153 VME Space Data Rate

4.2.1 VME Data Rate measured with a Chrislin VME Memory

USB2.0	approximate continuous Data Rate	
	Write	Read
A32-D32	15 KByte/sec	15 KByte/sec
A32-DMA-D32	9 MByte/sec	9 MByte/sec
A32-BLT32	19 MByte/sec	25 MByte/sec
A32-MBLT64	19 MByte/sec	39 MByte/sec

USB3.0	approximate continuous Data Rate	
	Write	Read
A32-D32	81 KByte/sec	84 KByte/sec
A32-DMA-D32	9 MByte/sec	9 MByte/sec
A32-BLT32	25 MByte/sec	26 MByte/sec
A32-MBLT64	50 MByte/sec	54 MByte/sec

Screen shot of the test program with USB3.0 connection.



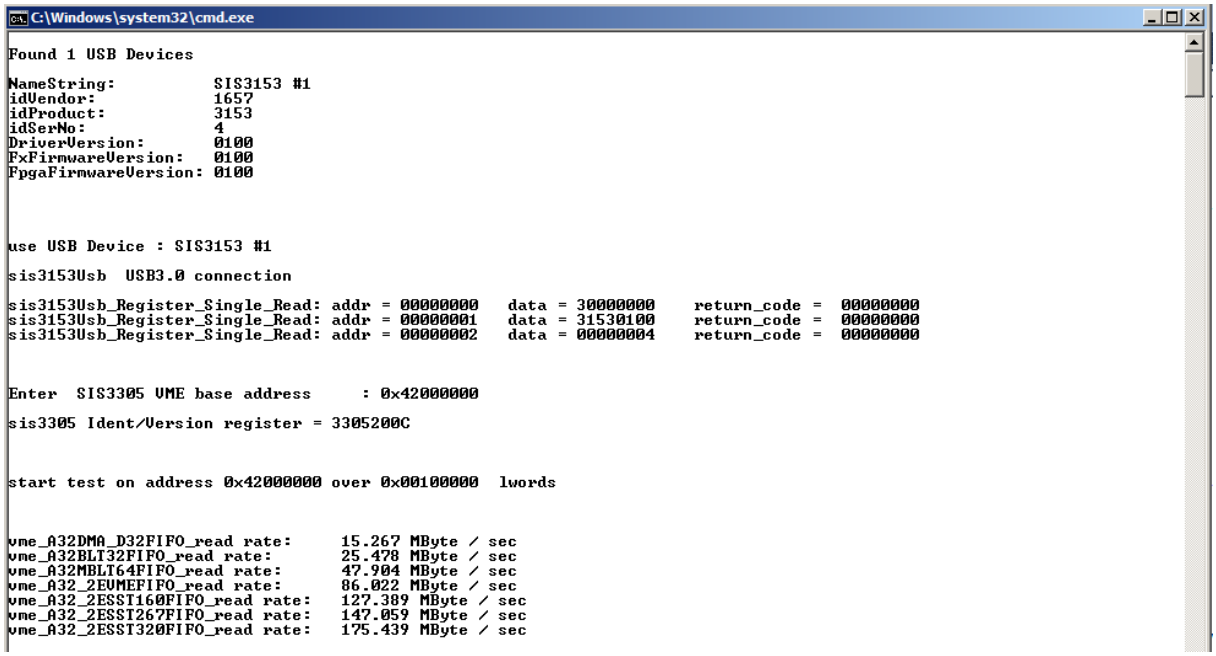
Note: The Chrislin memory is a legacy card, which does not have a state of the art VME slave implementation, but provides means to test standard read/write cycles like A32 D32.

4.2.2 VME Data Rate measured with a SIS3305 ADC

USB2.	approximate continuous Data Rate
	Read
A32-DMA-D32	15 MByte/sec
A32-BLT32	26 MByte/sec
A32-MBLT64	40 MByte/sec
A32-2eVME	40 MByte/sec
A32-2eSST160	40 MByte/sec
A32-2eSST267	40 MByte/sec
A32-2eSST320	40 MByte/sec

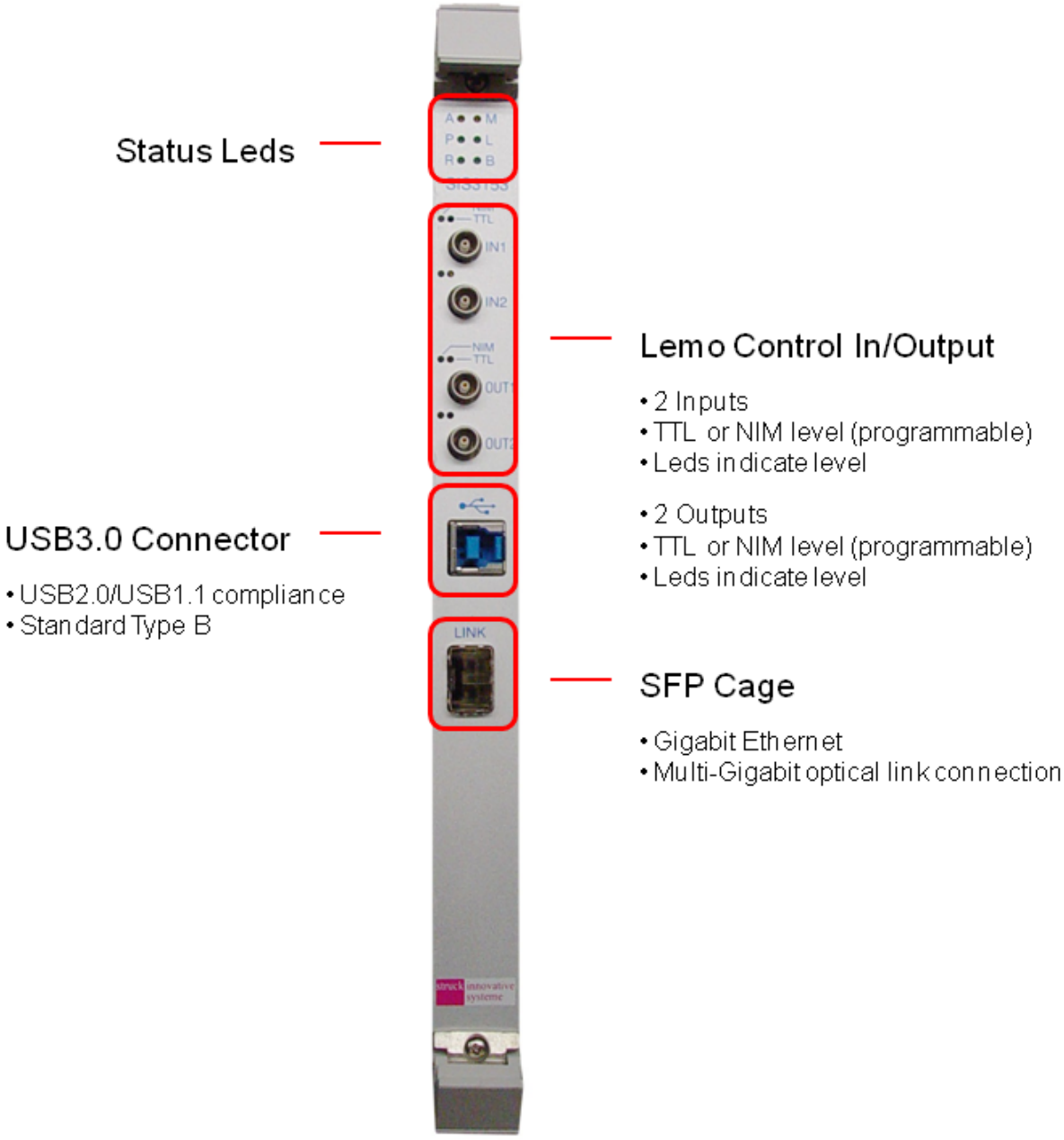
USB3.0	approximate continuous Data Rate
	Read
A32-DMA-D32	15 MByte/sec
A32-BLT32	26 MByte/sec
A32-MBLT64	47 MByte/sec
A32-2eVME	86 MByte/sec
A32-2eSST160	127 MByte/sec
A32-2eSST267	147 MByte/sec
A32-2eSST320	175 MByte/sec

Screen shot of the test program with USB3.0 connection.



5 Front Panel Elements

The SIS3153USB has 14 front panel LEDs, 2 LEMO 00 input, 2 LEMO 00 output connectors, a SFP cage and a type B USB connector.



6 LEDs

6.1 Front Panel LEDs

The six LEDs close to the top of the SIS3153 have the following function.

LED	Color	Description
A	Yellow	To be switched on/off under user program control (see USB Control/Status register (VME access to VME slave port of SIS3153, future option)
M	Yellow	VME master, lit whenever the SIS3153 accesses the VME bus
P	Green	Power, signals presence of +3.3 V supply voltage
L	Green	USB or Ethernet connection status (see below), depends on SW162-3
R	Green	Ready, lit when on board logic is configured (off during power up LED self test)
B	Green	VME Bus Error

During power up self test and FPGA configuration all LEDs except the Ready (R) LED are on. After the initialisation phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. The status of the L LED depends on the status of the USB connection.

Depends on the position of the Switch-3, the Link Led “L” indicates the status of the USB or Ethernet connection.

SW162-3 = Off:
The L LED will flash **N** times approximately every 4 seconds. N indicates USB connection:

N	Function
0	reserved
1	USB1 connection or not connected
2	USB2.0 connection
3	USB3.0 connection

SW162-3 = On:
The Link LED indicates after Power-Up and booting the FPGA the Ethernet Link Status:

- blinking with 4 Hz (every 0.25 sec) indicates no Ethernet Link
- blinking with 0.8 Hz (every 1.25 sec) indicates DHCP request busy
- blinking with **ping** access

Four pairs of green surface mounted LEDs are used to indicate the logic level of the front panel LEMO inputs and outputs.

Lit LED	Description	
NIM	In/output set to NIM level	
	logic state	voltage
	0	0 V
	1	< -0.8 V
TTL	In/output set to TTL level	
	logic state	voltage
	0	< 0.7 V
	1	> 2.4 V

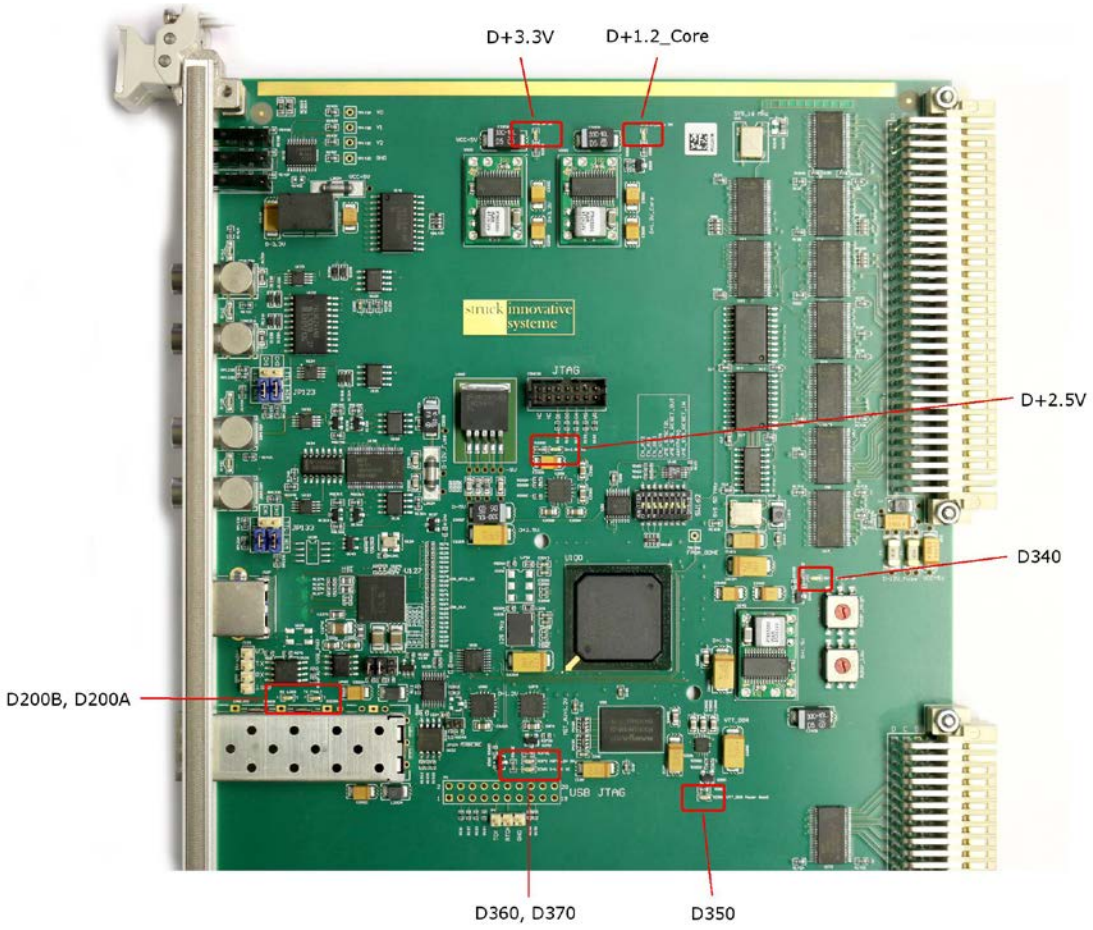
Note 1: the factory default power up logic level is NIM: The input default levels can be set on JP123, the default output levels on JP133. In addition the logic level can be set in the LEMO IO control register

Note 2: the inputs are factory terminated with 50 Ω, the outputs drive a load of 50 Ω

6.2 SMD LEDs

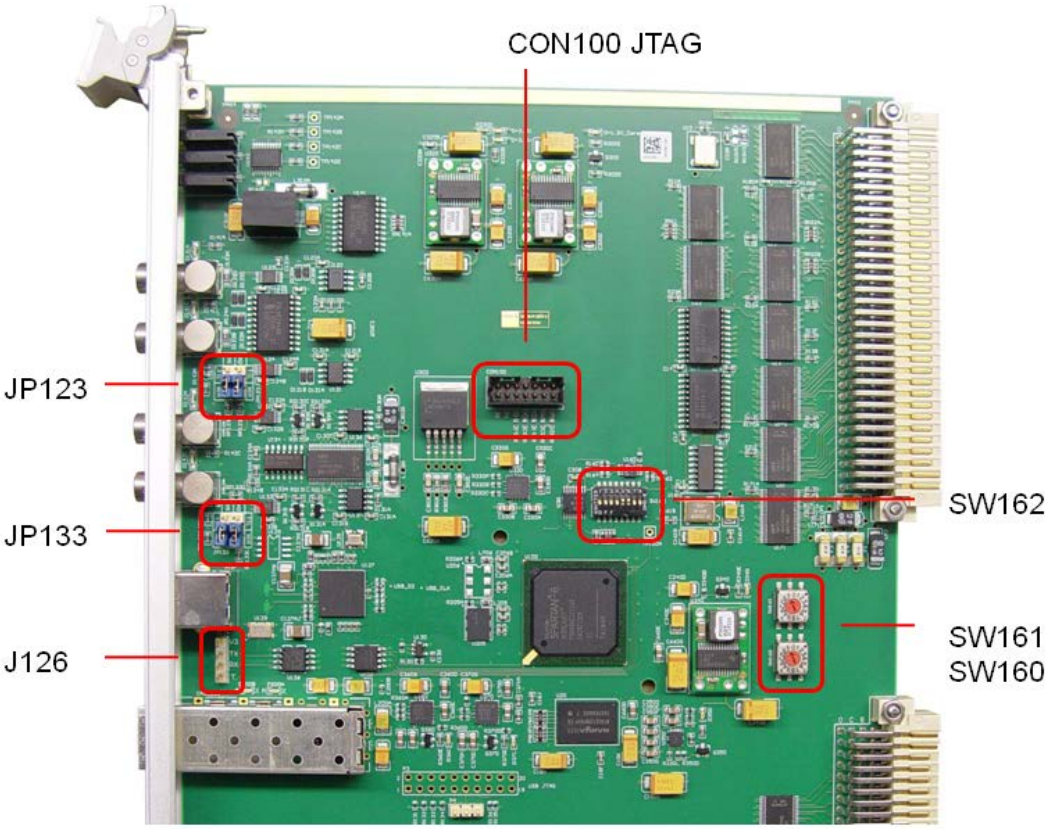
9 red surface mount LEDs are on the SIS3153 to visualize part of the board status.

LED designator	LED comment	Function
D200A	TX FAULT	Signals SFP transmit fault (lit without SFP installed also)
D200B	RX LOS	Signals SFP link loss (lit without SFP installed also)
D+1.2V_Core	D+1.2V_Core	Signals presence of 1.2V Core power
D+2.5V	D+2.5V	Signals presence of 2.5V power
D+3.3V	D+3.3V	Signals presence of 3.3V power
D340	D340	Signals presence of 1.5V power
D350	D350	Signals presence of VTT_VREF power
D360	D+1.2V	Signals presence of 1.2V power
D370	D370	Signals presence of 1.2V MGT power



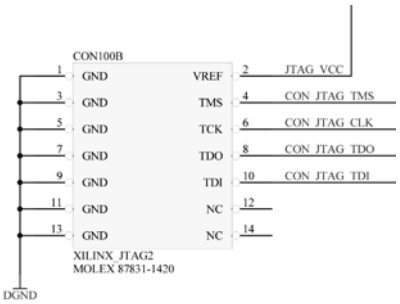
7 SIS3153 Jumpers, Switches and Connectors

The SIS3153 card has three jumper arrays, one DIP switch and two rotary switches.



7.1 CON100 JTAG

The SIS3153's on board logic can load its firmware from a SPI Flashprom or via the JTAG port on connector CON100.
Hardware like the HW-USB-II-G-JTAG in connection with the appropriate software will be required for in field JTAG firmware upgrades.
CON100 is a 2mm (i.e. metric) 14 pin header that allows you to reprogram the firmware of the SIS3153 board with a JTAG programmer. The pinout is shown in the schematic below. It is compatible with the cable that comes with the XILINX HW-USB-II-G-JTAG platform cable.



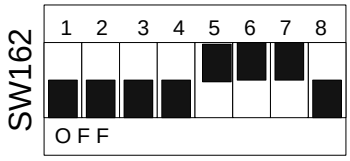
Note: The board has to be powered for reprogramming over JTAG

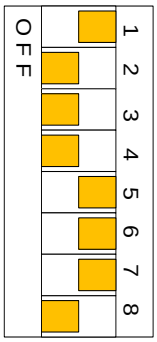
7.2 SW161/SW160 VME Slave Address (future feature)

The two rotary hexadecimal rotary encoders SW161 and SW160 are used to define the VME slave address. The function depends on the setting of switch SW162 also.

7.3 SW162 Dip switch System Controller/Reset Behavior/Slave Addressing

The 8 switches of SW162 are in charge of system controller function, reset behaviour and slave addressing as listed in the table below. Factory default settings are illustrated on the left hand side of the table.



SW162	Off Function	On Function
	**1: Disable A32 slave addressing***	**Enable A32 slave addressing***
	2: *	**
	3: Led L indicates USB activities	**Led L indicates Ethernet activities**
	4: DHCP disable	**DHCP enable (Ethernet)**
	5: System controller disable	**System controller enable**
	6: Disconnect FPGA reset to VME SYSRESET	**Connect FPGA reset to VME SYSRESET**
	7: Watchdog disable	**Watchdog enable**
	8: Disconnect VME SYSRESET from FPGA reset	**Connect VME SYSRESET to FPGA reset**

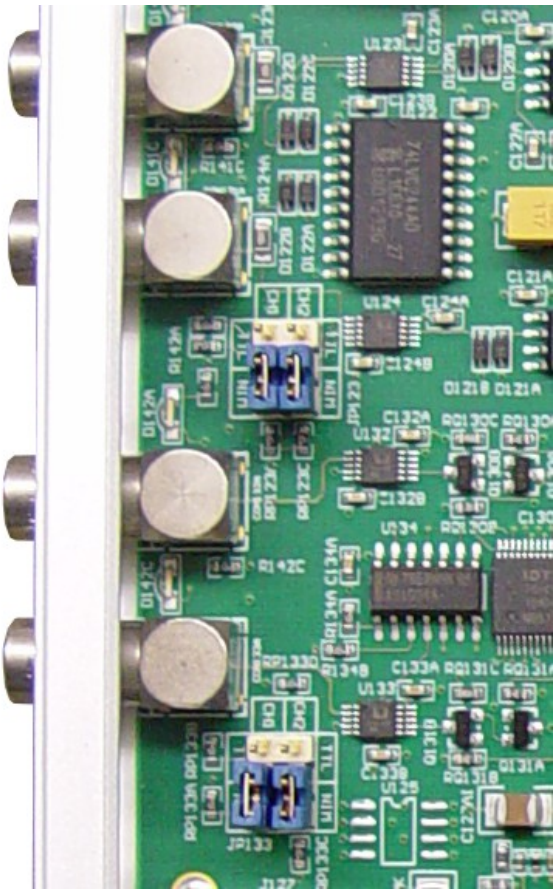
* reserved for future slave use

Note 1: do not set switch 6 and 8 to the on position at the same time (deadlock). The recommended setting is switch 6 on/8 off for a master/system controller and switch 6 off/8 on for non system controller units.

7.4 JP123 LEMO input, JP133 LEMO output logic level

Example:

JP123 both inputs configured for NIM (i.e. at factory default setting)
JP133 both outputs configured for NIM (i.e. at factory default setting)

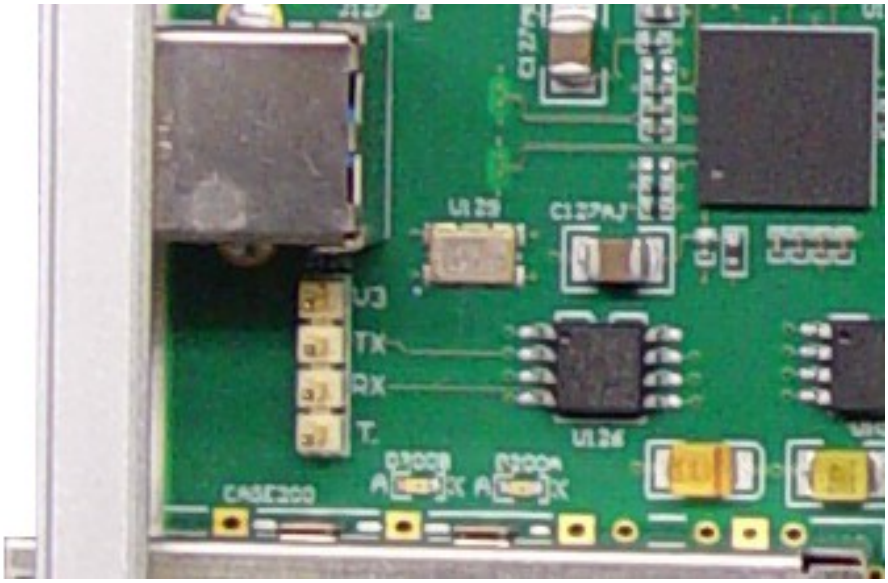


Note: The position for the jumpers for TTL is printed on the silk screen of the PCB.

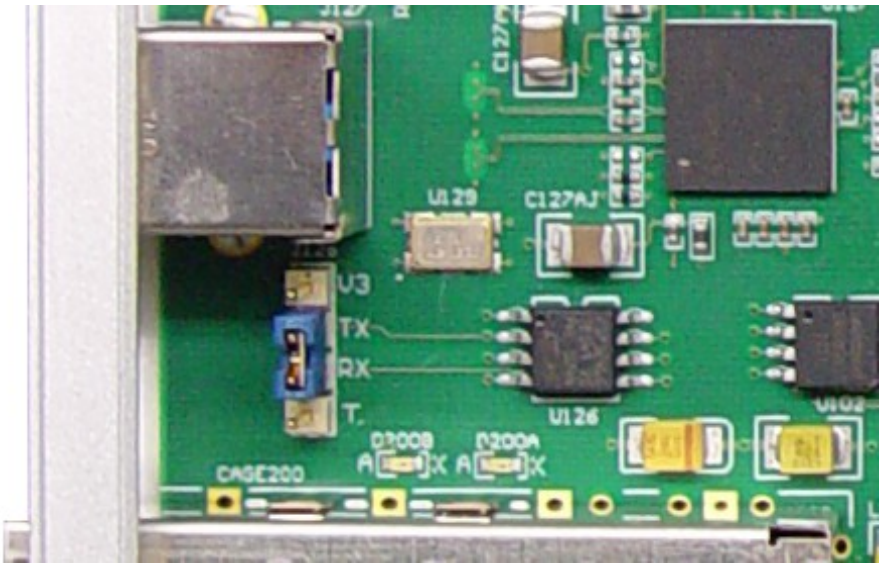
J126 USB Controller FX3 UART interface

The UART interface can be used for debugging of the USB FX3 controller software (used by Struck) and to force the USB FX3 controller to boot with a “Cypress default bootloader”. This is necessary to reload a new FX3 images (Struck bootloader) into the FX3-Flashprom. (SIS3153 V1 / SN001...005 only)

Normal operation (FX3 starts with a Struck bootloader after PowerUp) : open

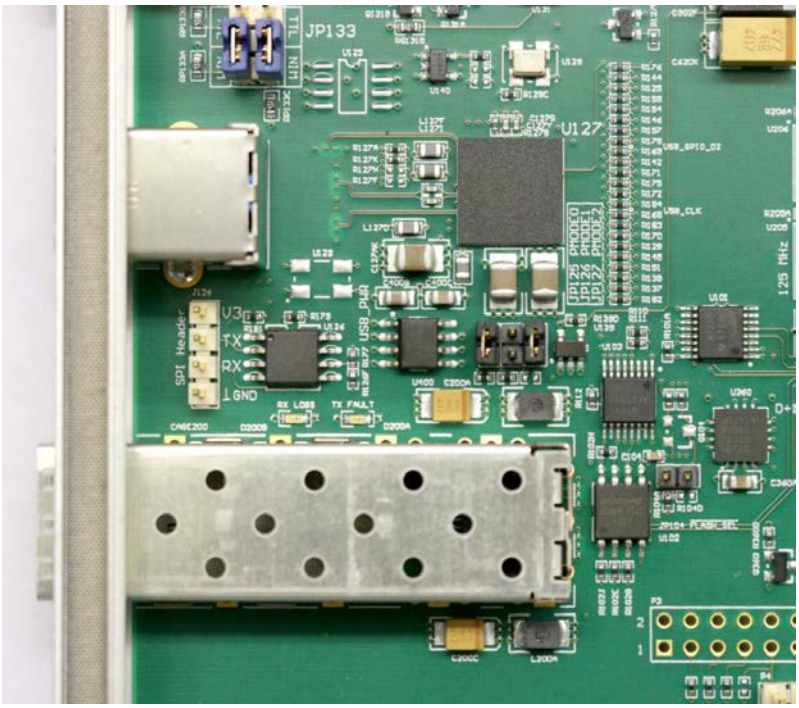


Force the FX3 to start with a “Cypress default bootloader”: Jumper between TX and RX

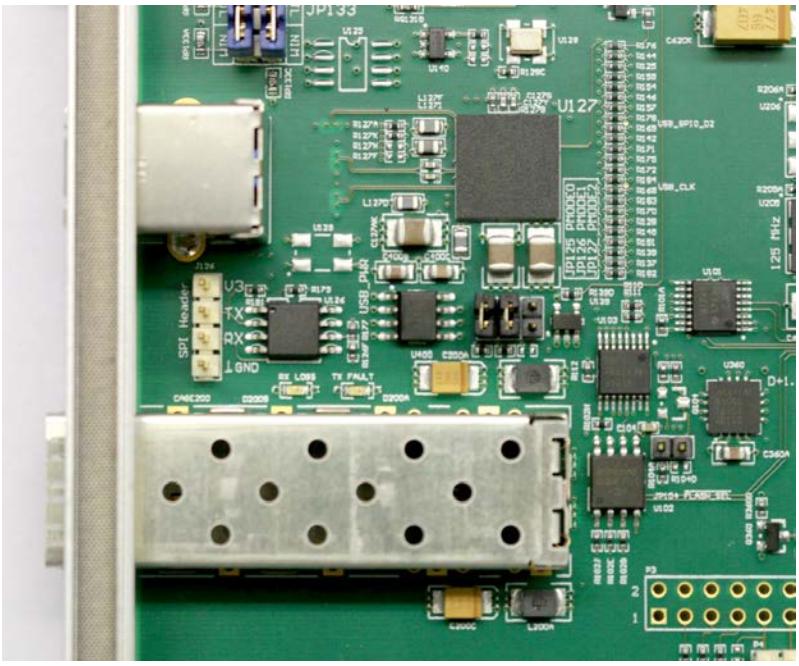


7.5 FX3 Boot mode (SIS3153 V2 / SN006 and above)

Normal operation (FX3 starts with a Struck bootloader after PowerUp)
PMODE0 and PMODE2 are closed



Force the FX3 to start with a “Cypress default bootloader”
PMODE0 and PMODE1 are closed



8 VME master/system controller

8.1 Multi master operation

VME is a multi master system, what allows you to use several SIS3153 modules or a mixture of SIS31xx VME interfaces and other VME master hardware in one crate. The sections below have to be taken into account for successful multi master operation.

8.1.1 System Controller

The SIS3153 can act as VME system controller. The 16 MHz VME system clock is generated by the SMD oscillator U10. and enabled/disabled by switch 5 of switch array SW162.
Make sure not to have more than one system controller on the VME backplane. The system controller has to be the leftmost master in the crate (typically it will reside in slot 1). In the case of the SIS3153 the system controller is enabled/disabled with switch 5 of SW162. SIS3153 system controller functionality can also be enabled/disabled via the "USB VME Master control register. The system controller on/off status is an OR of the control register setting and the jumper and can be read back from the status register. The factory default is system controller enabled (as most SIS3153 cards are used in a single master environment.

Note: A VME diagnosis module like the VDIS or a measurement with a VME bus extender can be used to check, whether a particular CPU or interface generates system clock (with all other interfaces/CPUs unplugged from the VME backplane. Some VME slave modules may use the system clock to initialize on board resources, this mechanism may fail if the system clock is generated by more than one board in the crate. The system clock can also be activated by software if the switch is in off position. In this case the user has to be aware, that no SYSCLOCK will be generated during the power up phase of the crate. A SYSRESET may be required by certain VME slaves for proper initialization of on board circuitry after SIS3153 SYSCLOCK generation was enabled.

8.1.2 Bus grant/bus mastership

- make sure to set the jumpers on the bus grant (BG) daisy chain properly unless your crate has an automatic daisy chain backplane (refer to the VME specification).
- Make sure, that no VME master locks bus mastership. It may be a good idea to use release when done instead of release on request where possible. It may be necessary to use a higher arbitration timeout than the standard value of 1 ms (selected via the USB VME Master control register).
- use different bus request (BR) levels as needed. The bus request level of the SIS3153 is programmed with the USB VME Master control register. The BR level of the SIS3153 defaults to 3 (highest level)

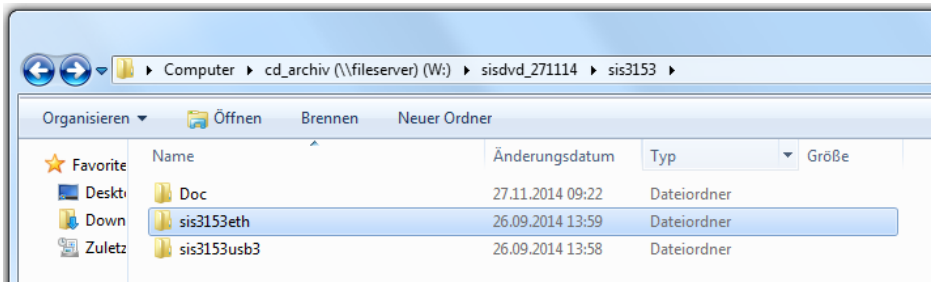
9 Connector types

The VME connectors and the front panel connectors used on the SIS3153 are:

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
90° PCB LEMO	Digitial I/O connectors	LEMO EPL.00.250.NTN
USB connector	USB connector type B	Amphenol GSB3211311 WEU

10 Software

LINUX and Windows are both supported for Ethernet and USB operation. The software can be found on the Struck product DVD as shown in the screenshot below.



Please refer to the software manuals for details.

Note: The documentation PDFs for both operating systems can be found in the Doc directory

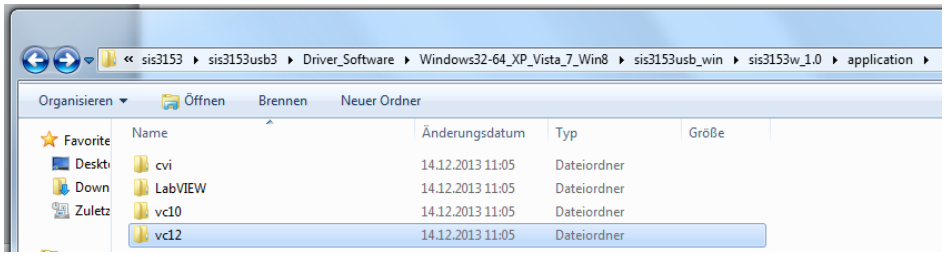
10.1 Windows

10.1.1 Ethernet

A CERN ROOT based GUI including the installer kit for the ROOT version, that was used at the time of generation, is furnished.

10.1.2 USB

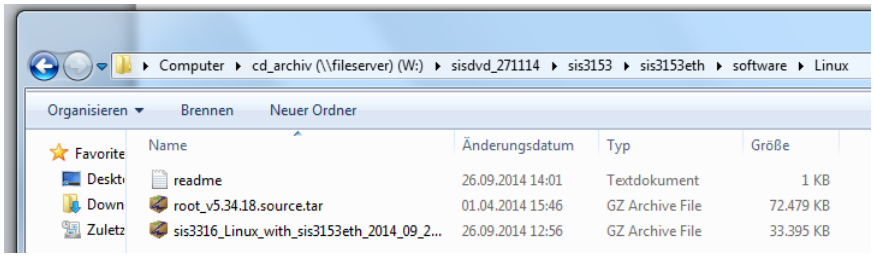
Application examples for Labview, Microsoft Visual C++ and National Instruments CVI can be found in the application directory as shown below.



10.2 LINUX

10.2.1 Ethernet

Like in the Windows case you'll find a root application coming with the ROOT installer kit of the version that was used at time of generation. A ready to run application for the SIS3316 digitizer is furnished also.



10.2.2 USB

In the LINUX case we continue to use the original SIS3150 sisusb driver, which is supporting the SIS3153 starting with release sisusb-1.2-005.

11 Appendix

11.1 Power Consumption

Find below a table listing the currents:

Configuration	+5V	+12V	-12V
USB3 interface	< 1,0 A	0 mA	< 100 mA

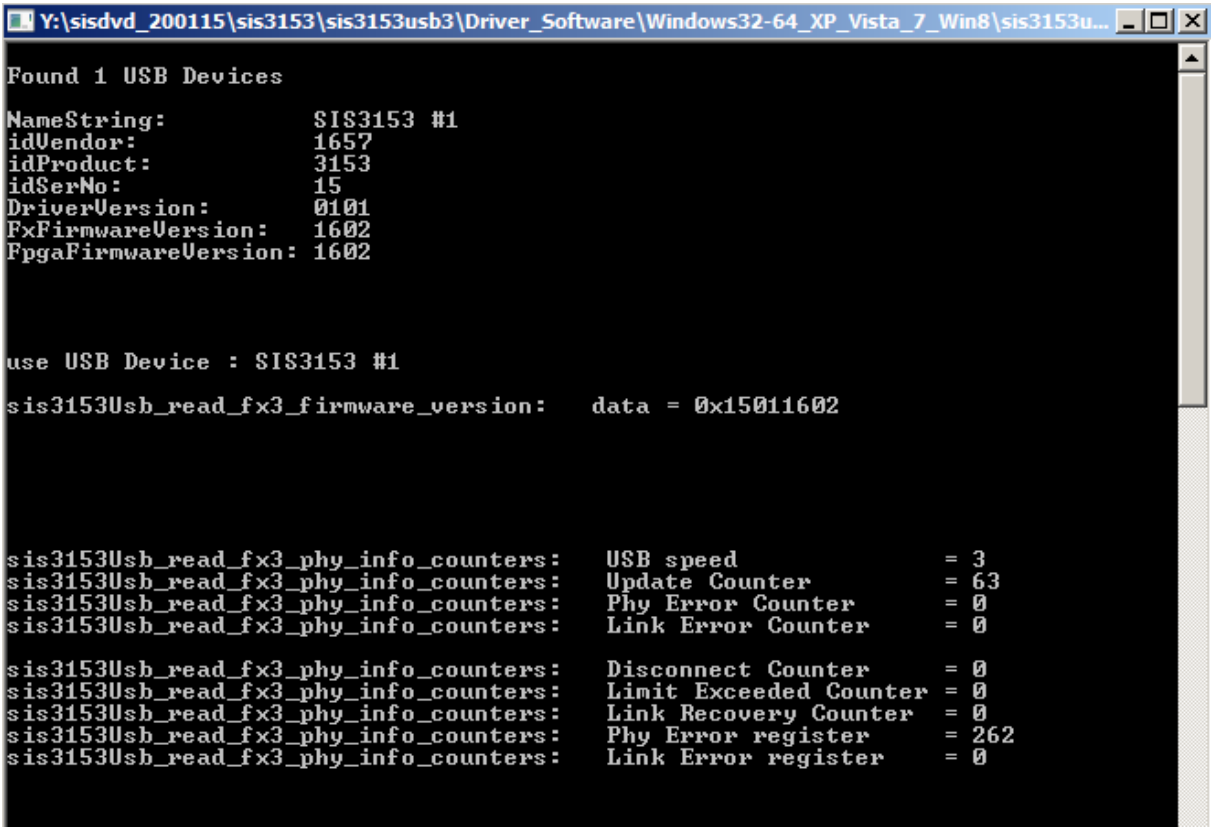
11.2 USB3.0 cable length

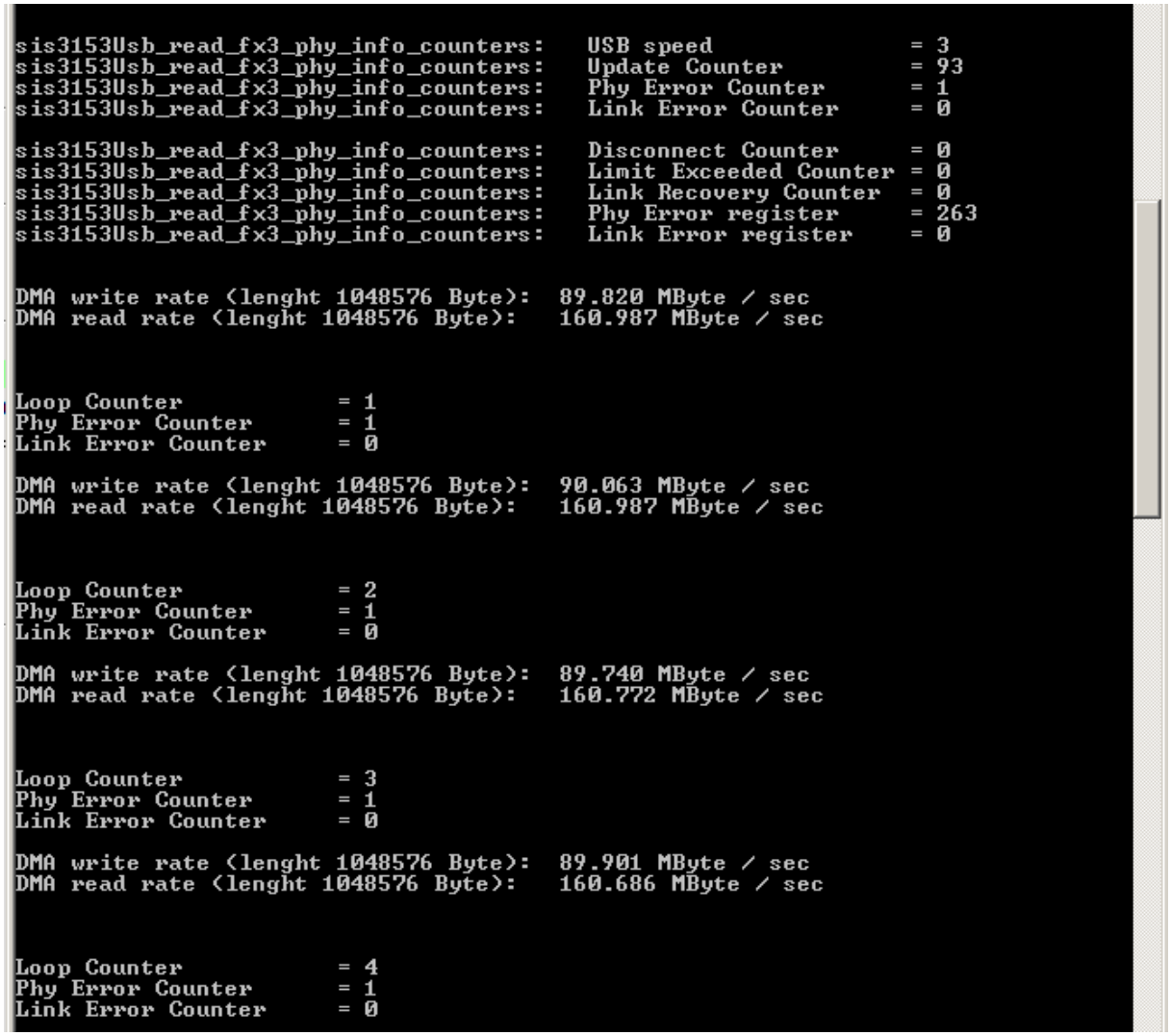
The recommended practical length limit for USB 3.0 cables is three meters.
In reality the maximum cable length for reliable USB3.0 operation may be limited by the hardware of the host computer. USB3.0 ports on the front of tower enclosures are typically connected to the mainboard by cables, while rear USB3.0 ports are attached to the mainboard directly, with the latter resulting in better performance.
By default the SIS3153 ships with 1.8 m cable length. The default cable length results in reliable longterm USB3.0 operation with a MACBook Pro and a Celsius W530 workstation (USB3.0 front port) in our lab.
So far we have not found reliable cables with active redrivers that allow for a safe extension of the possible cable length.
While PHY errors are expected at a certain rate due the given bit error rate, the Windows USB driver may terminate upon the first PHY error occurrence.

Note 1: In case you would like to cover longer distances you can use USB2.0 cables as a fallback solution

Note 2: The flashing frequency of the front panel L LED signals the type of the USB link connection (1 Hz USB, 2 Hz USB2.0 and 3 Hz for USB3.0)

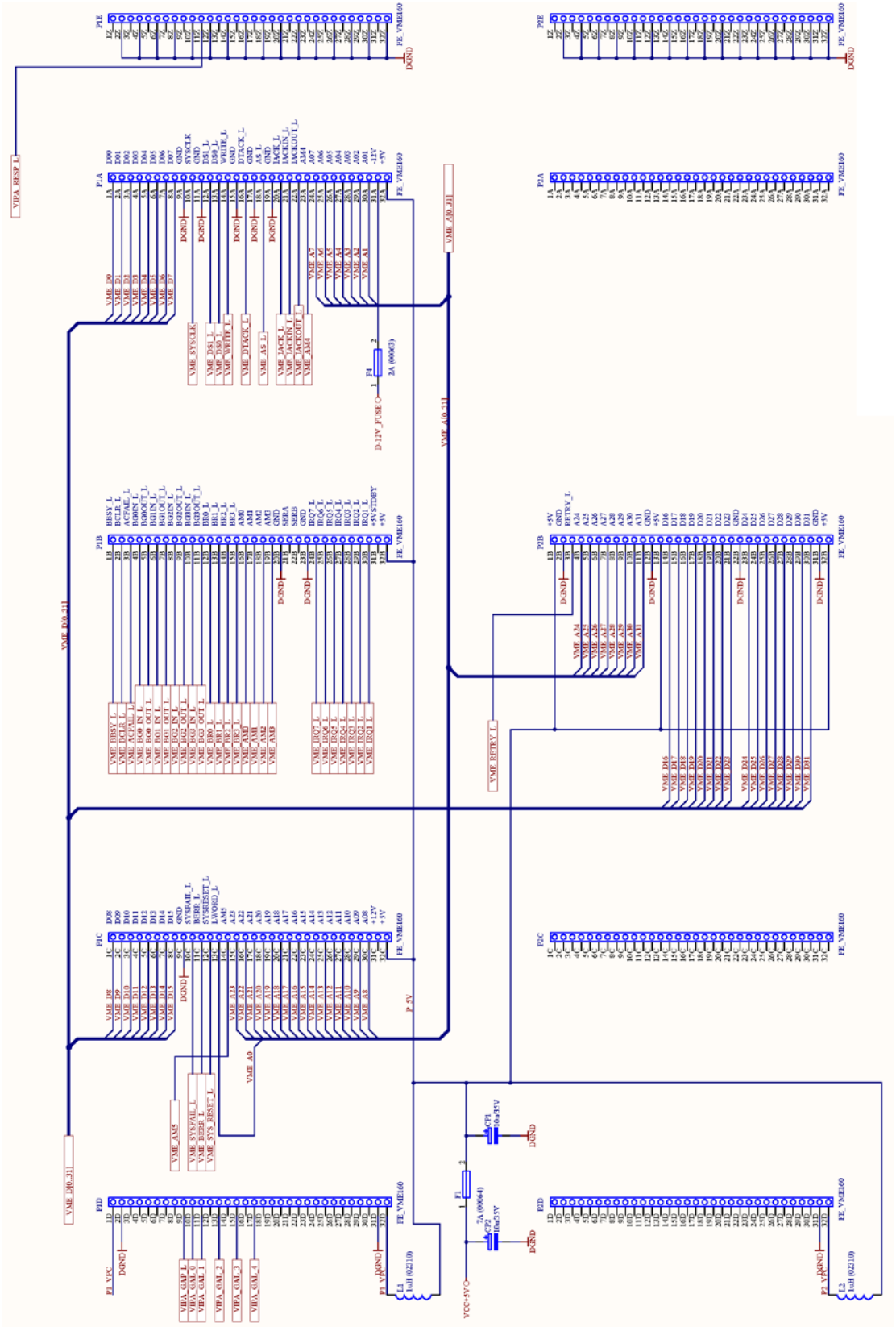
Note 3: The sis3153usb_internal_access_test program can be used to exercise the USB connection. A non excessive PHY error count is ok., while link errors are critical. A screenshot of the output at program start is shown below. The scrrenshot on the next page shows the output after the DMA read/write loop sequence has started.




sis3153Usb_read_fx3_phy_info_counters: USB speed = 3
sis3153Usb_read_fx3_phy_info_counters: Update Counter = 93
sis3153Usb_read_fx3_phy_info_counters: Phy Error Counter = 1
sis3153Usb_read_fx3_phy_info_counters: Link Error Counter = 0
sis3153Usb_read_fx3_phy_info_counters: Disconnect Counter = 0
sis3153Usb_read_fx3_phy_info_counters: Limit Exceeded Counter = 0
sis3153Usb_read_fx3_phy_info_counters: Link Recovery Counter = 0
sis3153Usb_read_fx3_phy_info_counters: Phy Error register = 263
sis3153Usb_read_fx3_phy_info_counters: Link Error register = 0
DMA write rate (lenght 1048576 Byte): 89.820 MByte / sec
DMA read rate (lenght 1048576 Byte): 160.987 MByte / sec
Loop Counter = 1
Phy Error Counter = 1
Link Error Counter = 0
DMA write rate (lenght 1048576 Byte): 90.063 MByte / sec
DMA read rate (lenght 1048576 Byte): 160.987 MByte / sec
Loop Counter = 2
Phy Error Counter = 1
Link Error Counter = 0
DMA write rate (lenght 1048576 Byte): 89.740 MByte / sec
DMA read rate (lenght 1048576 Byte): 160.772 MByte / sec
Loop Counter = 3
Phy Error Counter = 1
Link Error Counter = 0
DMA write rate (lenght 1048576 Byte): 89.901 MByte / sec
DMA read rate (lenght 1048576 Byte): 160.686 MByte / sec
Loop Counter = 4
Phy Error Counter = 1
Link Error Counter = 0

11.3 Schematic of P1 and P2 Connectors

The schematic of the two VME connectors is shown below.



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