ZMI 4100 Series Measurement Board Manual

OMP-0508T

Warnings and Notes

Warning!
Denotes a hazard that could cause injury to personnel and can also cause damage to the equipment.

Note, provides helpful information.

Notices

If equipment has CE Marking it indicates compliance to safety requirements established by the European Union. See page iii for a listing. The directives and standards in compliance are listed in a Declaration of Conformity, which is on file at Zygo Corporation, Middlefield, Connecticut, USA.

Do not dispose of this product as household waste. Use an approved organization that collects and/or recycles waste electrical and electronic equipment. For more information, contact ZYGO Customer Service or your local government office.

Revision Tracking

Revision	*Date*	*Revision*	*Date*
A	April 2005	K	November 2010
B	June 2005	L	December 2010
C	March 2006	M	January 2012
D	August 2007	N	May 2012
E	May 2008	P	January 2015
F	December 2009	Q	December 2016
G	February 2010	R	February 2018
H	April 2010	S	March 2018
J	June 2010	T	September 2022

CE Notice

Marking by the CE symbol indicates compliance of this Zygo instrument to the EMC (electromagnetic compatibility) Directive and the Low Voltage Directive of the European Union. Such marking is indicative that this system meets the following technical standards:

- EN 61326-1:2006 - Electrical equipment for measurement, control and laboratory use - EMC Requirements - Part 1: General requirements
- EN 61000-3-2:2006 - Electromagnetic compatibility (EMC) - Part 3-2: Limits for harmonic current emissions (equipment input current <= 16 A per phase)
- EN 61000-3-3:1995, A1:2001, A2:2005 - Electromagnetic compatibility (EMC) - Part 3-3: Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current <= 16 A per phase and not subject to conditional connection
- EN 61010-1:2001 - Safety requirements for electrical equipment for measurement, control, and laboratory use - Part 1: General requirements

A Declaration of Conformity in accordance with the preceding directives and standards has been made and is on file at Zygo Corporation, Middlefield, Connecticut, USA.

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Chapter 1 Introduction

1.1 Using This Manual

This document describes the functions and features of the ZMI 4100[1] family of measurement boards. The 4100 family is a high-performance evolution of the 4000 family and offers high sensitivity fiber optic receivers using Avalanche Photodiodes (APD) and optional Cyclic Error Correction (CEC) logic.

Unless otherwise specified, the information provided in this document applies equally, yet independently to all ZMI 4100 measurement axes. The ZMI 4100 Measurement Board family is listed in the table below.

Table 1-1 ZMI 4100 Products Covered in This Manual

Product	PCB Assy	Kit	Description
ZMI 4104	8020-0700-03	8020-0103-12 8020-0103-14	4-axis Measurement Board with APD
ZMI 4104C	8020-0700-03	8020-0103-13 8020-0103-15	4-axis Measurement Board with APD and CEC

Where applicable, the differences between boards are highlighted. In register descriptions, all axes are listed. Some of the registers and bits are accessed only through one axis (axis 3). The board type is indicated by the *Config* bits in Status Register 1 and the *System Type* bits in Status Register 0.

(1) U.S. Patent Numbers 6,597,459; 6,975,406; 7,428,685; and 7,542,147; other U.S. and foreign patents pending.

1.2 Assumptions and Standards

The ZMI 4100 Series Measurement Boards are register based VMEbus circuit boards for use with ZYGO motion measuring interferometers. This manual makes the assumption that you are familiar with VMEbus specifications and interferometry principles.

The ZMI Measurement Board is compliant with the following standards:

VME64 (ANSI/VITA 1-1994)

VME64 Extensions (ANSI/VITA 1.1-1997)

VMEbus International Trade Association
7825 E. Gelding Drive, Suite 104
Scottsdale, Arizona USA 85260-3415

telephone: 480-951-8866
fax 480-951-0720
website: www.vita.com
email: info@vita.com

IEEE Standard for Additional Mechanical Specifications for Microcomputers Using the IEEE 1101.1-1991 Equipment Practice (IEEE Std 1101.10-1996)

IEEE Customer Service
445 Hoes Lane, PO Box 1331
Piscataway, New Jersey, USA 08855-1331

telephone: 800-678-4333 (in the US and Canada)
732-981-0060 (outside the US and Canada)
fax: 732-981-9667
website: standards.ieee.org
email: customer.service@ieee.org

1.3 Manual Notations

- ☑ ZMI 4000 refers to any member of the ZMI 4000 family.
- ☑ ZMI 4100 refers to any member of the ZMI 4100 family (ZMI 4104 and 4104C).
- ☑ ZMI 4100C refers to ZMI 4104C.
- ☑ Register names are underlined, and the names of register bits or data fields are in italics.
- ☑ The term “set” refers to a logical 1, or asserted, state. The term “cleared” refers to a logical zero, or unasserted state.
- ☑ Hexadecimal numbers are indicated by a 0x prefix.
- ☑ An * (asterisk) is used to indicate active-low signals. Differential signals are indicated by a + and –suffix or a _P and a _N suffix.
- ☑ The online Adobe Acrobat PDF version of this document includes bookmarks and cross-references that make navigation easier.

1.4 Overview

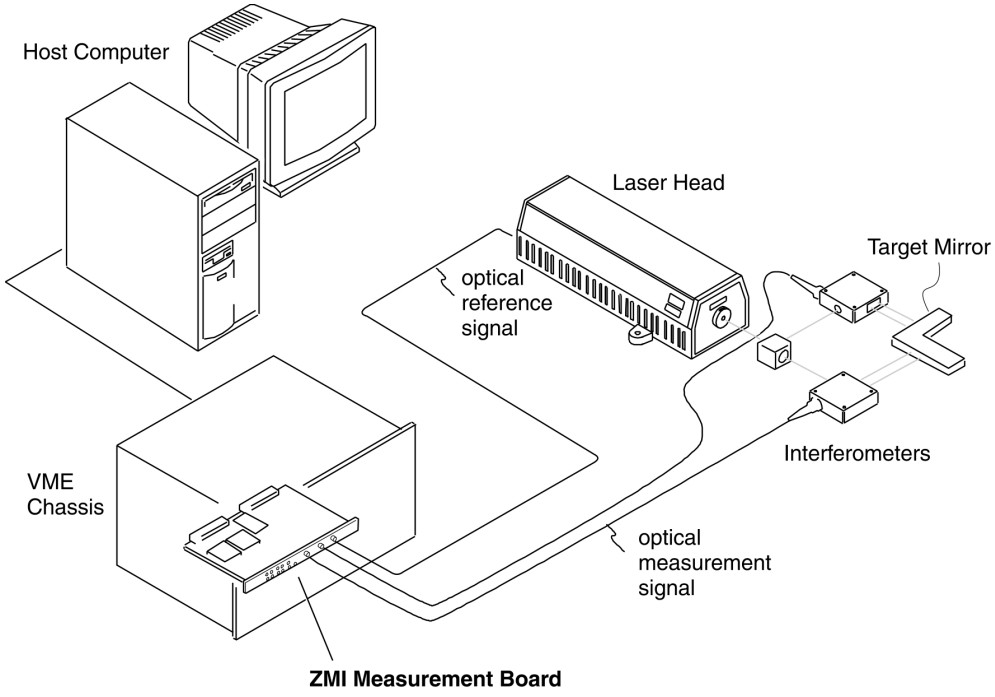
The ZMI 4100 family of products are register based, VME slave cards used with ZYGO motion measuring interferometers. The circuitry converts the interference signal from interferometers to position and velocity data. The Measurement Board complies electrically and mechanically with the VME64x VMEbus specification (ANSI/VITA 1-1994). All 4100 family products are 6U format boards.

This manual describes the installation and use of the ZMI 4100 Series Measurement Boards. A measurement board is a component in a complete ZYGO Motion Interferometer (ZMI) system. Figure 1-1 shows the basic structure of a ZMI system.

The Measurement Board is part of a total VME solution for an interferometry based motion measurement system. Minimally, a displacement measuring interferometer system consists of a laser head, optics, and a measurement board.

The function of the measurement board is to convert a measurement signal from an interferometer and a reference signal from the laser head into measurement data in the form of a 37-bit (or 32-bit) 2's complement word.

Figure 1-1 Basic ZMI System

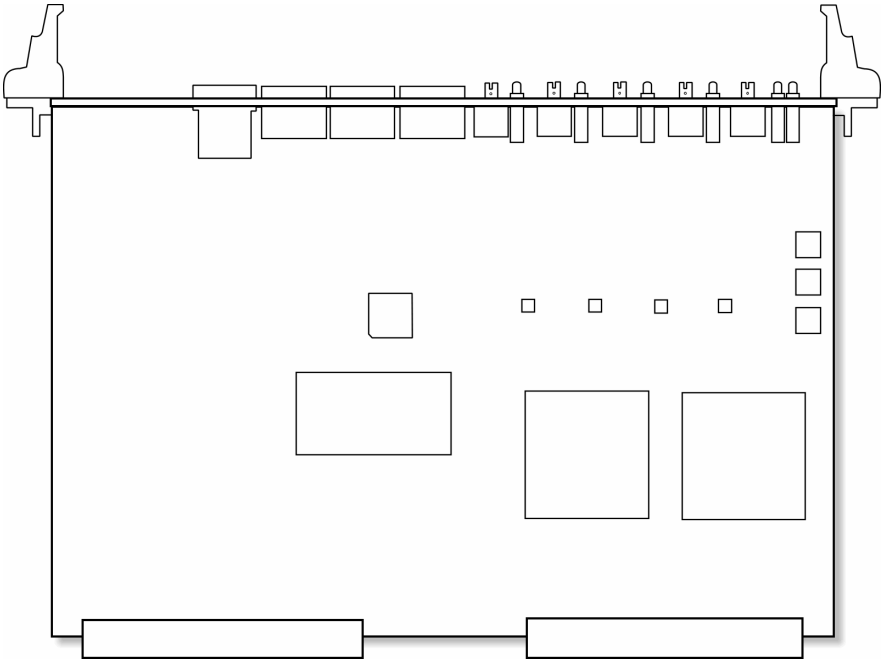


1.5 The ZMI 4100 Series Measurement Board

The ZMI 4100 Series Measurement Board, shown in Figure 1-2, is a multi axis, register based VME slave card used with ZYGO motion measuring interferometers. Its circuitry converts the interference signal from one to four interferometers to position and velocity data. The Measurement Board complies electrically and mechanically with the VME64 and VME64 Extensions specifications. The user must program parameters internal to the ZMI system by writing through the VMEbus interface.

ST fiber optic connectors are provided for measurement and reference inputs. Connectors are provided for one electrical reference input and two electrical reference outputs. The board provides a standard 16 or 32 bit VME interface, a proprietary 32 bit P2 interface, and a P2z interface containing several data, control and status signals.

Figure 1-2 ZMI 4100 Series Measurement Board



The features of the ZMI 4100 Series Measurement Board are:

- Standard 6U board outline with either two or four measurement axes.
- Position resolution of 0.31 nm with a single-pass interferometer, or 0.15 nm with a double-pass interferometer.
- Velocity range of ± 5.1 m/sec with a single-pass interferometer, or ± 2.55 m/sec with a double-pass interferometer.
- Compensated data age uncertainty of ±0.2 ns.
- Dynamic Data Age compensation.
- Input sensitivity of 0.1 μW.
- Two electrical reference outputs.
- A serial position data output for connection to other user interfaces.
- Diagnostic features.

1.5.1 ZMI 4100 Series Measurement System Block Diagram

The front panel has the following inputs:

- One fiber optic input for the reference signal from the laser head.
- One electrical input for the reference tree from another ZMI 4000 or ZMI 4100 board.
- Fiber optic inputs for measurement signals from the interferometers; one for each axis.

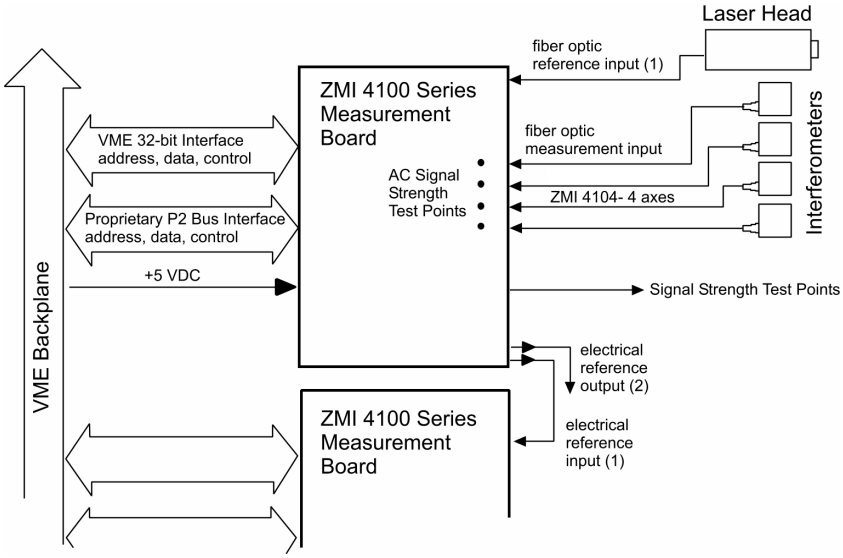
The front panel has the following outputs:

- Two electrical outputs for the reference tree to additional ZMI 4000 or ZMI 4100 boards.
- One signal strength test points connector; one for all axes.

The VMEbus P1 and P2 connectors include the following interfaces:

- Standard 32-bit VMEbus interface. This interface provides access to all measurement, control, status, and diagnostic functions.
- Proprietary high-speed P2bus interface. This interface provides access to all measurement functions, most control and status functions, and some diagnostic functions.
- P2d interface that includes hard-wired signals for reset input, error output, and comparator outputs.
- Serial interface that provides a connection to other user interfaces.

Figure 1-3 ZMI 4100 Series System Block Diagram



1.5.2 VMEbus Interface

The VMEbus interface provides an efficient means to acquire motion data and system status from the ZMI system to a user program running on a VMEbus computer. The VMEbus interface includes the following functions:

- Sampling of position, velocity, time, and error/status data.
- Digital filter coefficient programming.
- Offset register, user velocity limit, sample timer register.
- Programmable interrupts.
- Optical power, calibration data for optical power and data age compensation.

These data and functions are located in discrete registers within the VMEbus address space. Each measurement axis in a ZMI system must be programmed to a unique base address. All motion data can be acquired through a VME read access of the appropriate offset from the board base address.

The Zygo Corporation VME interface provides capability to transfer data using 16-bit or 32-bit word lengths. Typically all motion registers are 32 bits in length. However, the position data resides in 37-bit registers within the ZMI electronics. These registers can be accessed in three 16-bit transfers, or two 32-bit transfers. In addition, these registers can be configured to output any 32 bits of the 37 bits when the register is read.

VME functions include Status registers for indicating errors. Control registers are provided for setting modes of operation and for enabling interrupts. A VME Command and P2 Command register are provided for resetting error conditions and data accumulators.

The Measurement Board can generate VME interrupts on any one of the seven levels. All of the Measurement Board error conditions can be individually enabled to cause interrupts. The interrupt level is selected by a combination of a VME bus write accesses, storing an interrupt level code to an Interrupt Vector register. Interrupts are enabled by various bits in the Interrupt Enable register.

1.5.3 P2 Interface

The P2 connector provides a secondary high speed interface for reading 37-bit (or 32-bit) position data, 32-bit time data, 32-bit velocity data, and error/status data. This interface has a separate addressing and bus control system, permitting reading of data independent of the VMEbus.

The P2 interface provides the following functions:

- Reading and writing of most registers, including external sampling or direct reading of position, velocity, time, and error/status data.
- Programmable, periodic automatic data sampling.
- Reset position accumulator.
- Reset time accumulator.
- Reset P2 interrupts.

1.5.4 On-board Fiber Optic Detectors

The ZMI 4100 Series Measurement Boards include on-board fiber optic detectors. This feature eliminates the need for separate receivers and reduces sensitivity to electrostatic discharge. Each on-board detector connects directly to a fiber optic cable, from either a fiber optic interferometer or a nonfiber optic interferometer with a fiber optic pickup. In both cases, the fiber optic cable directs the light from the interferometer to a photo detector on the measurement board.

An analog test point is used when aligning the interferometer to ensure the best possible alignment. The interferometer alignment is adjusted to maximize the output voltage at the test point. The higher the voltage the greater the detected signal intensity. The specific output voltage varies depending upon the interferometer efficiency, the optical alignment, and other system tolerances. The minimum optical signal must be 0.1 microwatts, as measured at the entrance of a fiber optic pickup.

1.5.5 Data Output Summary

Interface[1]	Location	Rate	Bus Width	Position	Time	Velocity	Status	Config-uration	Diag-nostics
VMEbus	P1, P2	20 Mbyte/sec	32 bit	37 bit	32 bit	32 bit	All	All	All
P2bus	P2	40 Mbyte/sec[1]	32 bit	37 bit	32 bit	32 bit	All	Most	SSI
Serial Interface	P2z	40 Mbit/sec	1 bit/axis (4 axes)	37 bit	No	No	1 bit	No	No

(1) The maximum P2bus rate is 10 M samples/sec for previously latched data, and 6 M samples/sec for data latched by read.

1.6 ZMI 4100 Measurement Board Specifications

Measurement Board Configurations:

Board	Kit P/N	Description
4104	8020-0103-12	4-axis with APD
4104C	8020-0103-13	4-axis with APD and CEC

Previous board versions are designated 8020-0103-0X

Size: 6U VME board, 160 mm x 233 mm

Maximum Number of Boards in a System:
16 (64 axes); there may also be limits due to VME or P2 population

VMEbus:
Type: VME64X
Addressing: A24
Data Transfer: D16 or D32
P1 and P2 connectors: 160-pin DIN

Compliance: UL94V0, CE Mark*
(EN 55011A, EN 50082-1, EN 61010-1, EN 60950-1)
*Tested inside CE Mark compliant chassis

Reference Inputs:
ST fiber optic or HSSDC2 electrical, 20.0 MHz

Reference Outputs (2 per board):
HSSDC2 electrical, 20.0 MHz

Measure Inputs (1 per axis):
ST fiber optic, 20.0 ± 16.1 MHz

Signal Strength Test Points:
SSI, RJ-11 connector
On Board MMCX connectors for each axis

Status Indicators (LEDs):
Green – meas present (1 per axis), ref present,
Amber – meas error (1 per axis), ref error, config.
User LED

Measurement Axis Optical Input Power: A dynamic range of 10:1 is supported within a static range of 70 nW to the maximum value shown below.

APD Temp[1]	Max Optical Power
15 °C	7.0 µW
20 °C	7.9 µW
25 °C	8.5 µW
30 °C	9.0 µW
≥35 °C	9.6 µW

Power Requirement:
+5 VDC +0.25V/-0.125V @ 5 A typical, 7 A max.

Cooling Requirements (typical):
300 linear fpm at 30° C
400 linear fpm at 40° C
600 linear fpm at 50° C

Operating Environment:
Temperature: 15°C to 50°C
Humidity: 0 to 90% (non-condensing)
Pressure: Standard 1 atmosphere (700-800 mmHg), non-vacuum applications

Position Resolution:
λ/2048 (0.31 nm) (single pass interferometer)
λ/4096 (0.15 nm) (double pass interferometer)

Position Range:
± 21.2 m @ λ/2048 (single pass interferometer)
± 10.6 m @ λ/4096 (double pass interferometer)

Position Format: 37 bit - 2's complement

Time Resolution: 25 nanoseconds
Time Range: 107.4 seconds
Time Format: 32 bit - positive integer

Velocity Resolution: 18 to 22 bits
(function of the digital filter gains Kp and Kv)

Velocity Range:
± 5.1 m/sec @ λ/2048 (single pass interferometer)
± 2.55 m/sec @ λ/4096 (double pass interferometer)

Velocity Format: 32 bit - 2's complement
Maximum Acceleration: 100 g
(0.1 g max. during reset)

Cyclic Error Compensation (CEC):
CEC Initialization Time: 4.1 ms
CEC Initialization Velocity: >= 1.2 mm/s
CEC Update Rate: 2.4 kHz
CEC Reduction: 10x reduction of 20 MHz Leakage (CE 0) and -1 Doppler (CE N)

Data Age (P2 output):
1 µs typical for the ZMI 4100
2 µs typical for the ZMI 4100C

Data Age Uncertainty, Uncompensated:
± 6 ns (axes on any one board)
± 30 ns (15 boards, any axis to any axis)

Data Age Uncertainty, Factory Compensated:
± 0.2 ns (axes on any one board)
± 1.0 ns (any axes including maximum of 3 calibrated reference jumpers)

Accuracy[2]: (single pass interferometer)
σ ≤1.0 LSB at 0 m/sec
σ ≤1.2 LSB at ± 2.5 m/sec
σ ≤1.4 LSB at ± 5.1 m/sec

Noise[2]: ± 3 LSB (3σ)
Temperature Coefficient: < 1 LSB per °C
MTBF: 236,700 hours (MIL-HDBK-217 method)

(1) APD temperature as reported by the APD Temp register. This is higher than ambient temperature and depends on air flow provided to board.

(2) 70 nW with 90% modulation into onboard APD receiver, at optimum APD gain, and filter settings of Kp = -6, Kv = -15. Accuracy and noise at minimum optical power is not significantly affected by temperature.

Table 1-2 Part Numbers and Revisions for 4100 Series Measurement Boards

Component →	**Product**	**Firmware**	**+ Software**	**= PROM**
Base P/N →		SPM8020-9276-	SPM8020-9277-	SPM8020-9278-
Versions →	ZMI 4104 ZMI 4104C	-01 -01	-01 -01	-03 -05
Register for version info. →		Firmware Version	Software Version	PROM Version
Register for revision info. →		Firmware Revision	Software Revision	PROM Revision

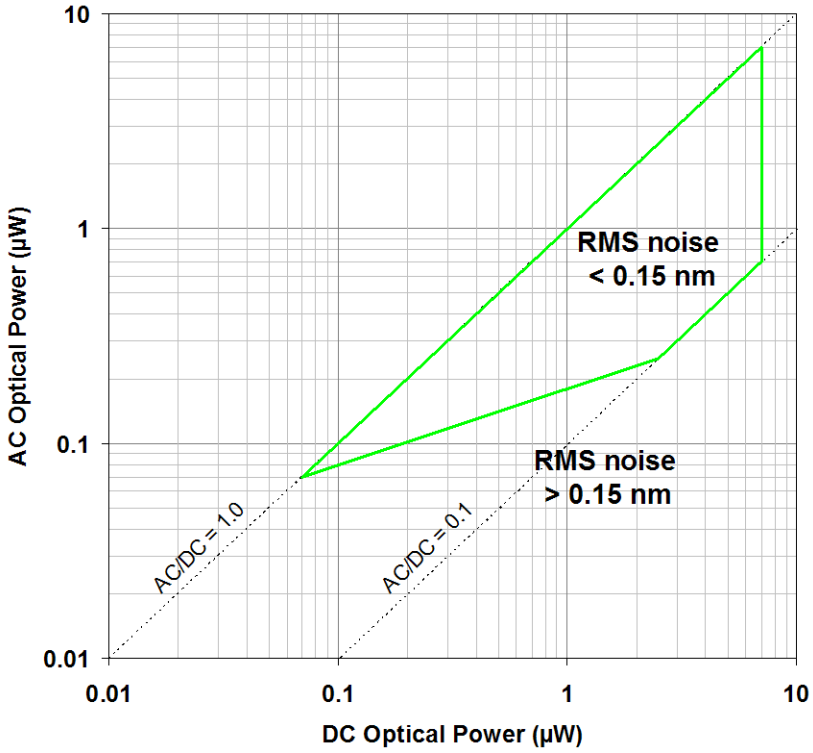
Component →	**Product**	**PCB Assy**	**+ PROM**	**= Kit**
Base P/N →		8020-0700-	SPM8020-9278-	8020-0103-
Versions →	ZMI 4104 ZMI 4104C	-03 -03	-03 -05	-12, -14 -13, -15
Register for version info. →		EEPROM, Status Reg 1 *Config*	PROM Version, Status Reg 0 *System Type*	
Register for revision info. →		EEPROM	PROM Revision	

Firmware is the circuit design in the FPGA (Field Programmable Gate Array), which includes control and signal processing functions. Software is the program that runs in the processor in the FPGA, primarily for control of the APD. Firmware and Software together form the data in the FPGA configuration PROM.

1.6.1 Optical Power Operating Range

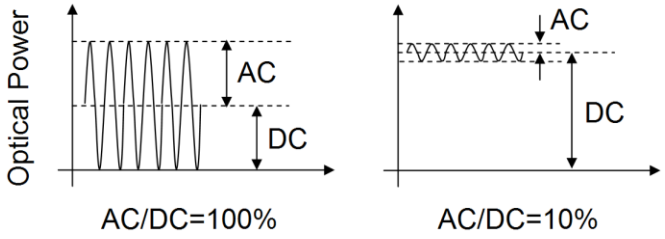
ZMI 4100 measurement boards operate over a wide range of AC and DC optical powers. The graphs in the second figure show how these optical powers are defined. The powers indicated are incident power onto the on-board receiver. Typically, the AC/DC ratio will be high when the target mirror is normal to the measurement beams, so that the interferometer measurement and reference beams have good overlap at the Fiber Optic Pickup (FOP). As the target mirror tilts, measurement-to-reference overlap will decrease. Since unmixed light may enter the FOP, the DC power will decrease less than the AC power, decreasing the AC/DC ratio. AC/DC ratios in the region marked "RMS noise > 0.15 nm" may be used. The board will not operate if the DC optical power limit is exceeded. Also refer to section 2.9 Measurement Performance.

Figure 1-4 Measurement Board Optical Power Operating Range



The specified operating region for the ZMI 4100 is indicated by the green line. AC/DC ratios within this area will have less than 0.15 nm noise (1 σ RMS).

Figure 1-5 AC and DC Optical Powers



AC and DC optical powers are defined so that maximal AC power results in AC/DC = 1.

1.7 Compatibility

The ZMI 4100 Series Measurement Boards are compatible with the ZMI 7702 Laser Heads, 7714 Laser Heads, 7724 Laser Heads, fiber optic cables, fiber optic pickups, and all industry standard interferometers and optics.

The VME interface is compatible with VME64 and VME64x specifications. Due to the larger 160-pin connectors, high power supply current, and the greater forces required to seat or remove boards, a VME64x chassis with 160 pin connectors and insertion/extraction rails is highly recommended. The ZMI 4100 boards are supplied with a VME64x front panel, which is incompatible with some VME subracks.

The ZMI 4100 Series Measurement Boards are *not* compatible with the ZMI 1000 Measurement Board, ZMI 1000A Measurement Board, ZMI 2001 Measurement Board, ZMI 2002 Measurement Board, ZMI 2004 Measurement Board, ZMI 2004A Measurement Board, ZMI 1000 electronics, ZMI 2000 electronics, ZMI PC Measurement Board, ZMI 510 Measurement Board, the ZYGO 2/20 system electronics, the ZMI 764Z Pulse Converter Board, the 7081 Receiver, or the 7701 and 7701a Laser Heads.

The ZMI 4104/4104C is compatible with and interchangeable with the ZMI 4004. The power up default is with CEC disabled. For systems using data age compensation with CEC board types (ZMI 4104C) and standard board types (ZMI 4004) the ZMI 4004 is required to have the extended data age range feature, see appendix D line 16 for applicable version and revision information.

The ZMI 4100 family is compatible with the ZMI 4000 family with the following differences:

- The diagnostic ADC inputs have been rearranged, there are now 24 ADC inputs for the master FPGA, and 8 inputs for the slave FPGA.
- The diagnostic ADCs may be operated by either the user VME interface, or the internal processor interface. The time for an ADC read may be 300 µs maximum.
- The EEPROM data has been rearranged.
- The EEPROM may be operated by either the user VME interface, or the internal processor interface. The time for an EEPROM read may be 600 µs maximum.
- For the ZMI 4100C, the CEC registers are as described for the ZMI 4004CEC. The powerup default setting is with CEC disabled.
- There are additional registers to control the APD. The powerup default setting is with constant APD gain.

The current ZMI 4100 boards are *fully backward compatible* with previous generations (P/N 8020-0103-0X). An adapter cable (P/N 1115-800-056) will be needed for linking the electrical reference cables if this signal is required.

1.8 Mixing ZMI 2400, 4000 and 4100 Series Boards

It's possible to use ZMI 2400 boards with ZMI 4004, ZMI 4104 and ZMI 4104C boards. Data will be latched nearly simultaneously. However, circuit differences among the board types can result in as much as 1 µs of data age difference between the ZMI 2400 boards and the ZMI 4104C boards. This is due primarily to the extended processing time required for cyclic error compensation. Unfortunately, the ZMI 2400 board data age adjustment circuit cannot compensate for this difference because its range is too short. In systems that use ZMI 2400 boards with ZMI 4004/4104 boards only (no ZMI 4104C boards), the ZMI 2400 boards and ZMI 4004/4104 boards will have similar, but not specified data age.

1.8.1 Recommended Configuration for Mixed Board Systems

The ZMI 2400 boards should be located at the end of the ZMI 4000 series board electrical reference daisy chain signal. The first ZMI 4000 board should receive the optical reference signal from the laser head. It should also drive the SCLK1 sample signal on the P2bus. All ZMI 4000 series boards should use SCLK1 for sampling. The last 2400 board should have SCLK1 enabled to receive the SCLK1 falling edge and drive the SCLK0 sample signal. All ZMI 2400 series boards should use SCLK0 for sampling.

Figure 1-6 Configuring ZMI Boards

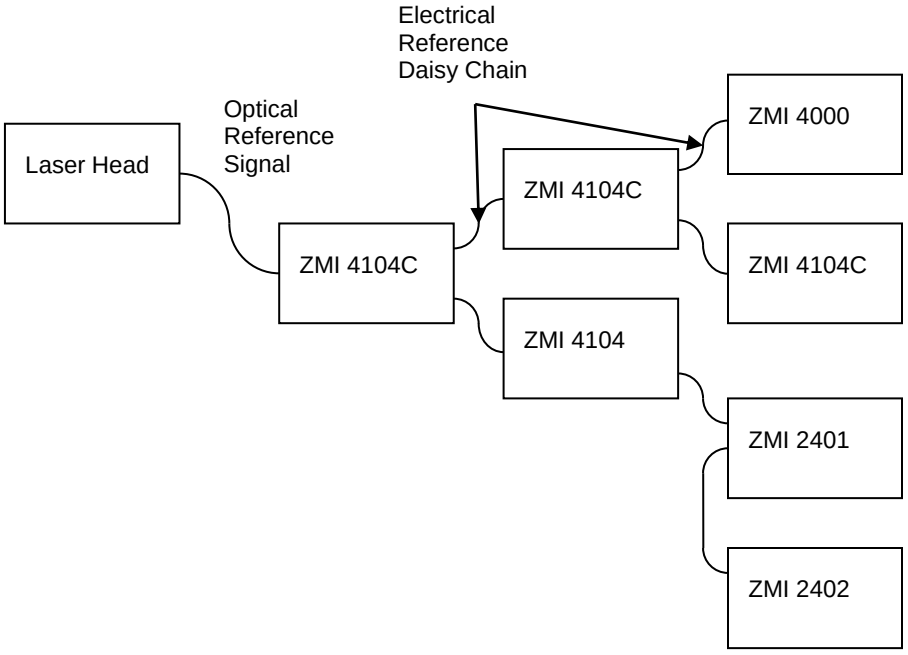
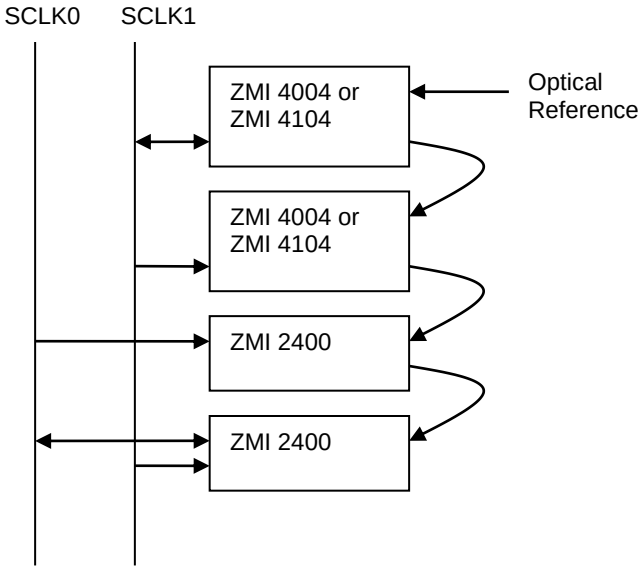


Figure 1-7 SCLK Signals When Mixing ZMI Boards



1.8.2 Data Age Adjustment for Mixed Board Systems

All ZMI 4000 series boards should be included as a set when calculating the data age adjustment values. All ZMI 2400 series boards should be included as a separate set when calculating their data age adjustment values. In this case, the data age between all ZMI 4000 boards will be very low. The data age between all ZMI 2400 boards will also be very low. The sample time of the ZMI 2400 series boards will be approximately 250±50 ns later than the ZMI 4000 series boards due to the resynchronization of SCLK. Please see the data age adjustment section of the appropriate measurement board operating manual.

1.9 Changes from the 4000 to 4100 Series

- Measurement board fiber optic receivers have APD (Avalanche Photodiode) substituted for PIN Diode. This provides approximately 10x increase in sensitivity.
- The four measure signal test points are located on-board, using MMCX connectors, instead of through the front panel using probe jacks.
- Additional FPGA registers to support APD control.
- CEC (Cyclic Error Correction) processing (ZMI 4100C only).
- Microcontroller (μC) implemented within the FPGA, primarily for APD control.

1.10 Safety Summary

The following general safety precautions must be observed for installation and operation of this board. ZYGO assumes no liability for the customer's failure to comply with these requirements.

Warnings!

Ground the Instrument. To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The ground wire on the chassis or enclosure must be reliably connected to an electrical ground at the power outlet.

Use Proper ESD Handling Techniques. Use proper ESD (electrostatic discharge) techniques when handling the board. The board should be stored in a static shield bag and handled only by individuals using a static control grounding devices. Avoid touching connectors on the board; electrostatic discharge can damage components.

Disconnect Power During Installation. Do not install the board with power on. Install the board and connect cables only when power is off and the power cable is disconnected.

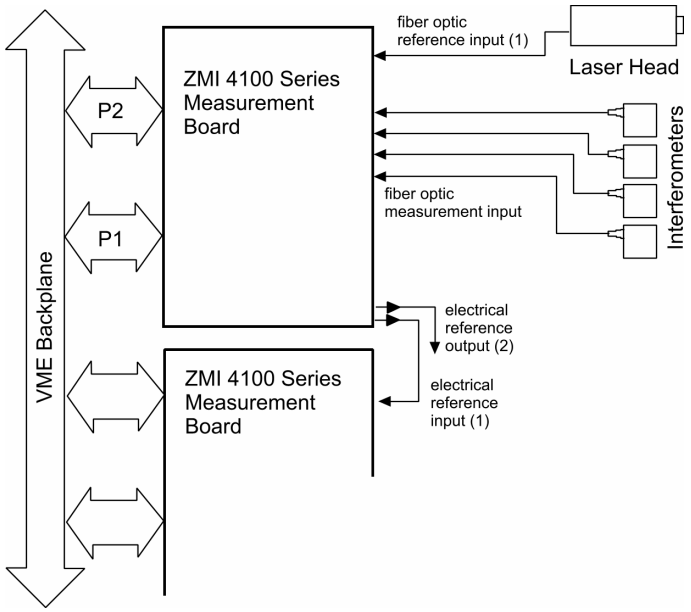
Do Not Modify Equipment. Do not install substitute parts or perform any unauthorized modification of the board.

Chapter 2 Installation

2.1 System Interconnections

General system connections are shown in Figure 2-1. The laser head provides an optical reference signal to the first Measurement Board, which then provides a synchronized electronic reference signal to other Measurement Boards in the system. The reference signal is also used to minimize data age uncertainty. The optical measurement signals are provided directly from the interferometer through a fiber optic connection. Boards are addressed, and position, time, and velocity data is obtained through the VMEbus and/or P2 interface (P1 and P2 connectors).

Figure 2-1 System Interconnections



2.2 Considerations for the VME Backplane

2.2.1 Basic Requirements of the VME Backplane

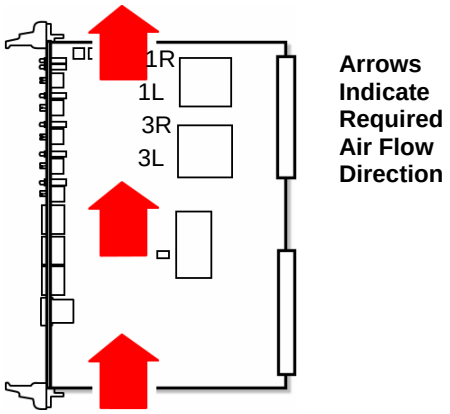
The Measurement Board may be installed in a user-supplied VME backplane. Ensure that the user VME backplane meets the following basic requirements:

- Supplies incoming DC voltage for the board: +5 VDC @7.0A
- Provides sufficient cooling air flow (see Cooling section below).
- Supplies a level of noise and interference immunity.

Proper backplane design is important to provide reliable data transfers among all boards using the backplane. Most commercially available VMEbus backplanes provide good performance for basic VMEbus functions. Systems using the P2bus should incorporate the P2bus signals into the same backplane as the VMEbus, with careful attention to crosstalk prevention and impedance matching. Implementation of the P2bus as a secondary backplane plugged onto the primary backplane, or as a ribbon cable, may result in corrupted VME or P2 data due to crosstalk or ringing. In all applications using the P2bus, adequate signal fidelity and lack of crosstalk on both the VMEbus and P2bus signals should be verified with a high speed oscilloscope.

2.2.2 Cooling

The nominal cooling requirements for the ZMI 4100 are listed in the specifications in chapter 1. These specifications are guidelines only. Due to uncertainties in air flow uniformity and measurement, actual cooling performance must be evaluated in the actual application to ensure sufficient margin for reliable operation under any expected conditions.



The figure shows the approximate locations of the temperature monitors. The Remote monitors (1R and 3R) are at the top left corners of FPGA U46 and U48. The Local monitors (1L and 3L) are in devices U33 and U36.

To verify cooling performance:

1. Determine maximum operating ambient temperature T_{Amax}.
2. Operate system in final configuration, allow system temperature to stabilize and measure ambient temperature T_A.
3. Follow the procedure described for the Diag Temp Monitor Read register to measure board temperature T_B and FPGA temperature T_F for axes 1 and 3.
4. Calculate minimum operating temperature margin for axes 1 or axes 1 and 3:
   $T_{Margin} = \min((75 - T_F), (70 - T_B)) - (T_{Amax} - T_A)$
5. Minimum margin must be 10°C or more.

Sufficient cooling is required to keep the board temperature below 60°C and the FPGA temperature below 65°C (10°C margins). Air flow measurement results are highly variable, depending on sensor type, sensor location, and air turbulence. Air flow is affected by:

- Changes in hardware, cabling, or other conditions.
- Vacant board slots. A vacant slot provides an easier path for air flow around the boards needing cooling.
- Different board types. A board with more components may require more cooling, but may offer greater restriction to air flow and thus receive less cooling.

2.2.3 Noise and Interference

Noise and interference caused by other system components, such as switching power supplies and fans, can degrade the accuracy of the Measurement Board. The possible symptoms are: apparent noise in the position data output, measurement error LED on, or reference error LED on.

It is recommended to check performance when installing the Measurement Board in a user-supplied chassis. To perform the check, install the Measurement Board and the Laser Head, according to their installation instructions. As shown in Figure 2-2, position a fiber optic pickup directly in the Laser Head output beam with no interferometer. In this configuration, and after a system reset, the position data should be stable to ±1 LSB with no error LEDs on. If the data is not stable or there are error LEDs on, noise interference is indicated. Potential noise sources are listed in Table 2-1.

Figure 2-2 Typical System Noise Test

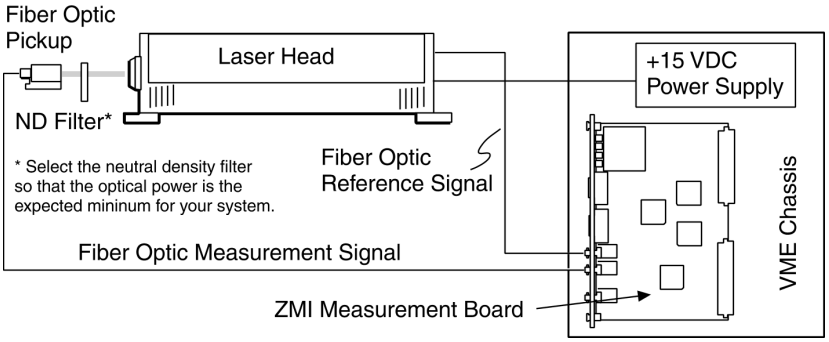
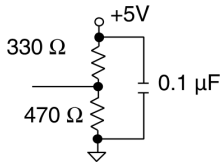


Table 2-1 Possible VME Chassis Noise Sources

Noise Source	Guidelines
Switching Power Supplies	Switching power supplies can cause transients on the power supply conductors at harmonics of the switching frequency. Follow the installation and noise suppression recommendations of the power supply manufacturer.
DC Brushless Fans	DC brushless fans can also cause transients on the power supply conductors. Follow the installation and noise suppression recommendations of the fan manufacturer.
VME Backplane	Use passive termination not active termination. The recommended termination circuit is shown here. 
Improper Component Grounding	Improper grounding of the Measurement Board, laser head, or cables, may cause measurement data noise. Adhere to the recommended grounding guidelines in Table 2-2.

2.2.4 Recommended Grounding

Improper grounding of the Measurement Board, laser head, or cables may introduce noise in the measurement data. Adhere to the recommendations in Table 2-2 to prevent electromagnetic interference from causing measurement problems.

Table 2-2 Recommended Grounding of Components

Component	Recommendation
Measurement Board	The front panel of the board should be in contact with earth ground through its captive screws. The captive screws secure the board to the card cage, which in turn should be connected to earth ground.
Laser Head	The laser head feet and enclosure should be isolated from earth ground. Grounding is provided through the cable.
Cables	All cables should be shielded and connected to earth ground through their connectors and the electronic enclosure panel. The fiber optic cables do not require shielding. Use of ZYGO supplied cables provides for proper grounding and signal noise immunity.

2.3 Installing the Measurement Board

1. Determine beforehand the outputs required and the preferred interface to your control system.

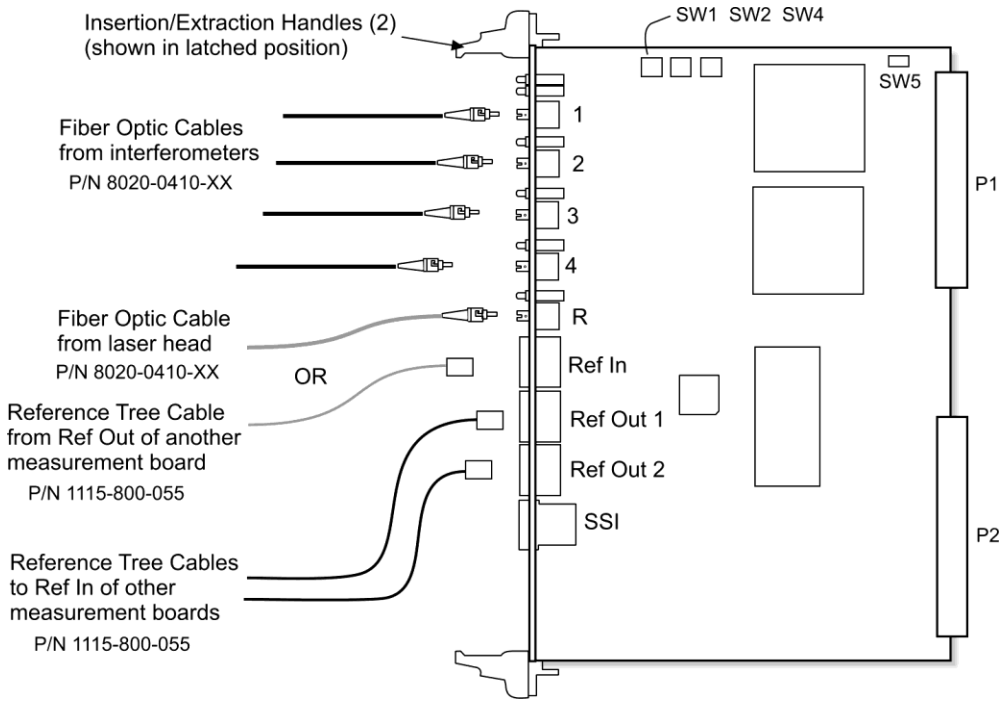
   Warning!
   Use proper handling techniques when touching the Measurement Board to prevent the board from being damaged by electrostatic discharge (ESD). The board should be stored in a static shield bag and handled only by individuals using a static control wrist grounding strap.

2. Wearing a static control wrist strap, remove the board from the static shield bag.
3. Determine the addressing scheme and set SW5, and SW1, SW2, and SW4 as necessary. Refer to Table 2-3.

   Warning!
   Disconnect the VMEbus chassis from power before installing the board and when connecting (or disconnecting) cables.

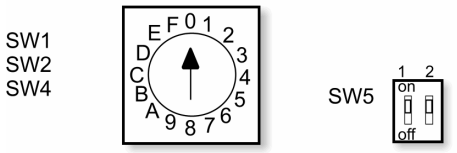
4. Be sure that the captive front panel screws are freely floating in their holes.
5. Push the release buttons on the board's insertion/extraction handles, and swing the handles away from each other.
6. Insert the board into the VME subrack. As the P1 and P2 connectors meet the backplane connectors, pull the insertion/extraction handles toward each other until the board is fully seated and the handles latch.
7. Screw the captive front panel screws into the card cage frame.
8. Connect the cables.

Figure 2-3 Typical Measurement Board Connections



2.3.1 Base Address

Table 2-3 ZMI 4100 Measurement Board Base Address Settings



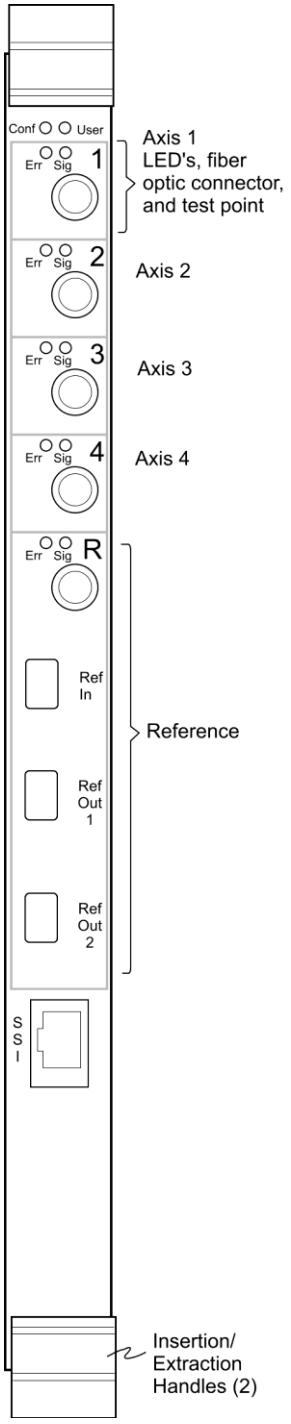
VME64x Geographical Addressing:	*No*	*Yes*
SW5-2	1 (off)	0 (on)
SW1	A(23:20)	A(23:20)
SW2	A(19:16)	0

P2 Addressing Setup:	*Switch*	*Control Register*
SW5-1	1 (off)	0 (on)
SW4	A(11:8)	0
Control Register 17 (3:0)	N/A	A(11:8)

2.4 Board Front Panel

The front panel is compliant to both the VME64x and IEEE 1101.10 specifications. It is grounded to chassis ground through the mounting hardware and the EMI gasket along one edge of the panel. The shields of the front panel electrical connectors are grounded to the front panel, and isolated from circuit ground, for ESD immunity.

Figure 2-4 Measurement Board Front Panel



Conf — Configuration LED (yellow); indicates that the FPGA (Field Programmable Gate Array) devices are in the configuration process.

User — User LED (green) controlled by the *User LED* bit in Control Register 16 of axis 3.

Err (1-4) — Measurement Error LED (yellow); indicates an error in the measurement signal for the applicable axis. When flashing, indicates the board is receiving insufficient cooling air flow.

Sig (1-4) — Measurement Signal LED (green); indicates the measurement signal is present for the axis.

1-4 — ST type fiber optic connectors, 1 for each axis, for the measurement signal from an interferometer.

Err (R) — Reference Error LED (yellow), indicates a reference or system error. For more information see Section 4.2.

The Reference Error LED is the logical OR of the reference error signal for all measurement axes.

Sig (R) — Reference Signal LED (green), indicates the reference signal is present.

R — ST type fiber optic connector for the optical reference signal from the laser head. If the system has multiple measurement boards, connect the optical signal to a board centrally located.

Ref In — Electrical reference signal input connector; it is an HSSDC2 (High Speed Serial Data Connector). In systems with multiple measurement boards it receives an electrical reference signal from another board.

Ref Out 1, 2 — Electrical reference signal output connectors (2). These are HSSDC2 (High Speed Serial Data Connector) connectors. In systems with multiple measurement boards, they link multiple measurement boards to the same reference signal.

SSI — Signal Strength Indicator connector for all the axes on the board. It is a shielded RJ-11 connector.

2.4.1 Measure Fiber Input Connectors

The four measure fiber input connectors are type ST fiber optic connectors, compatible with 400 µm or smaller fiber optic cables. A photodiode is located in the back of the receptacle. It is electrically isolated from the front panel; however, it is connected to signal ground on the board.

2.4.2 Reference Fiber Input Connector

The reference fiber input connectors is a type ST fiber optic connector, compatible with 400 µm or smaller fiber optic cables. Only one measurement board in a system receives the optical signal from the laser head; it should be centrally located in the VME backplane to facilitate reference connections to other measurement boards.

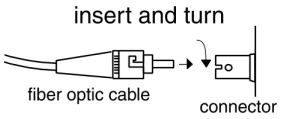
2.4.3 Connecting Fiber Optic Cables

One or more fiber optic cables can be used to connect the interferometer to the measurement board measure fiber input connectors. The Fiber Optic Feed-Thru, P/N 1189-857-076, connects two cables together for extending cable length or for passing through a sheet metal enclosure. The efficiency of each Feed-Thru is typically from 80% to 90%.

Warning!
Protective caps should be installed when the cable is not in use. Dropping an unprotected fiber optic cable could damage the fiber.

Clearance and bending specifications for fiber optic cables and Fiber Optic Feed-Thru dimensional specifications are located in the ZMI Cable Guide, OMP-0333.

1. Remove protective caps from both ends of fiber optic cable.
2. Examine the fiber end to ensure that no contaminants or residue are present.
3. If necessary, clean the fiber end. Clean the fiber end using a lint free wipe dampened with Methanol or Isopropyl alcohol and gently wipe both cable ends.
4. Insert the cable end into the connector. Align the pin to the slot in the cable's collar. Press and turn the cable clockwise to secure the pin into the cable's detent.



2.4.4 Reference Tree Connectors (Ref In and Ref Out)

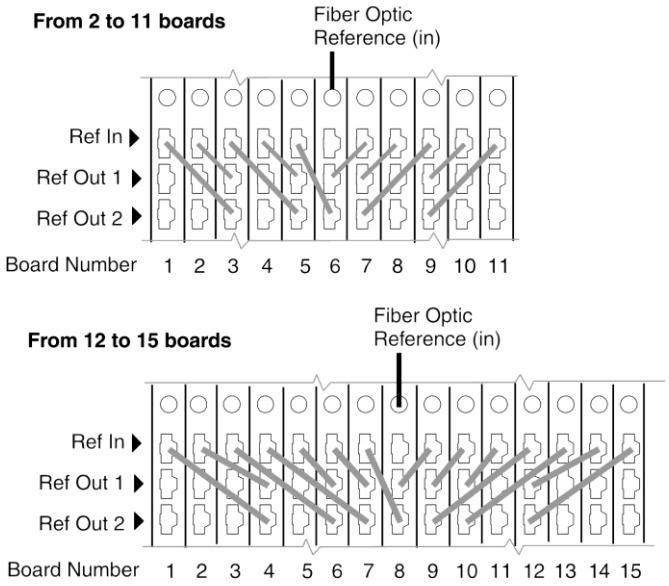
Each measurement board has three electrical reference tree connectors, one for input and two for output. The reference tree connectors are HSSDC2 (High Speed Serial Data Connector) connectors. Sample connection diagrams are shown here.

The HSSDC2 reference cable is 9.8 in. (250 mm) long; it is ZYGO P/N 1115-800-055. Note that the fiber optic reference cable from the laser head should connect to the measurement board in the center of the VME backplane for easy distribution of electrical reference signals.

Previous versions of the Measurement Board used HSSDC connectors.

ZYGO P/N 1115-800-056 is an adapter cable which can be used to connect from HSSDC to HSSDC2.

Figure 2-5 Reference Tree Arrangements

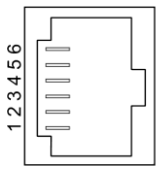


2.4.5 SSI (Signal Strength Indicator) Connector

The Signal Strength Indicator diagnostic connector (SSI DAC) contains the signal strength indicators for all measurement axes. The connector is a shielded, 6-pin, RJ-11 type connector. All signals are filtered by a 1 kΩ series resistor and a 1000 pF capacitor to chassis ground.

The user must supply a mating RJ-11 jack and cable to use the SSI connector. The cable does not need to be shielded. A digital multimeter can be used to measure the DC voltage, which is proportional to the AC signal strength. The maximum SSI DAC voltage is 1.25 V.

Figure 2-6 SSI Connector Pinout



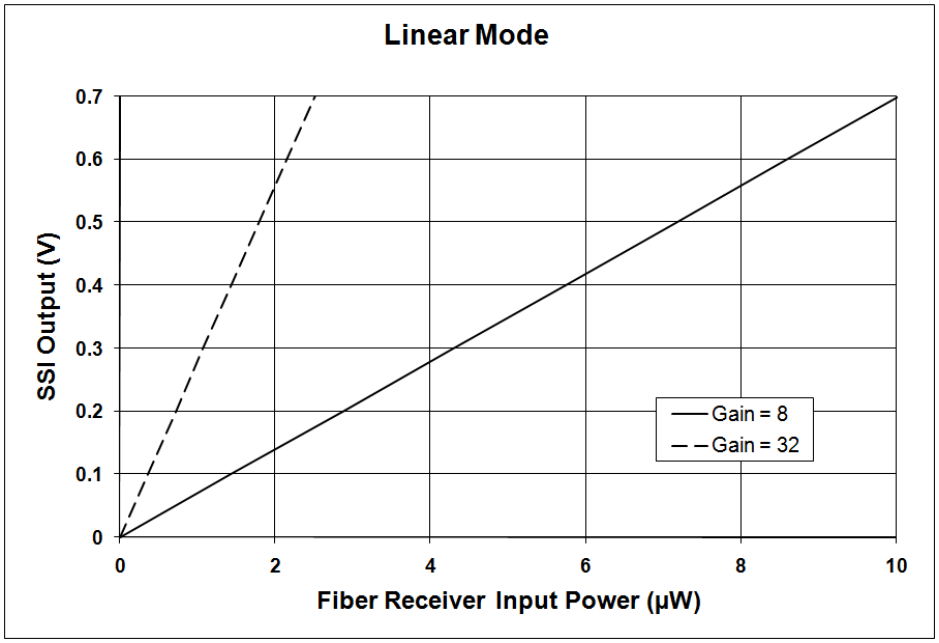
Pin	Signal
1	Reserved
2	SSI_1
3	SSI_2
4	SSI_3
5	SSI_4
6	Return

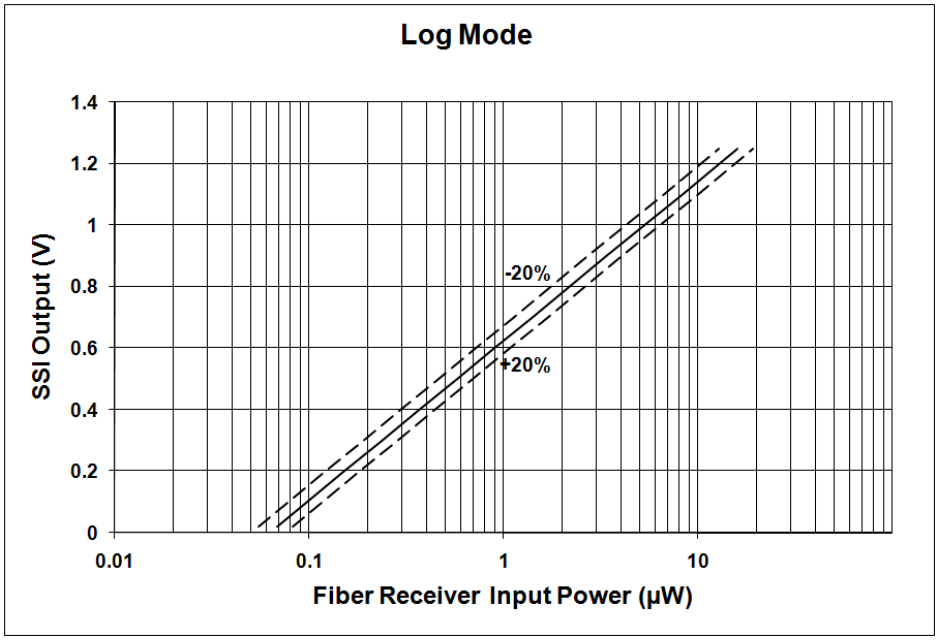
The SSI output has three modes:

Linear	SSI voltage is proportional to the optical AC signal. The proportionality constant is different for each APD gain setting. Component tolerances and APD gain adjustment make this output mode useful only for relative measurements.
x16	SSI voltage is the Linear value multiplied by 16.
Log	SSI voltage is proportional to the logarithm of the optical AC signal. Log mode is factory calibrated to achieve an accuracy of ±20%. In this mode, the output voltage does not depend on the APD gain setting.

The following graphs show the fiber receiver input optical power and the associated SSI voltage for Linear Mode and Log Mode. The Linear Mode graph depicts a typical transfer function characteristic.

Figure 2-7 ZMI 4100 Series Measurement Board SSI Voltage





The following table provides details of the three modes.

Mode	Control Register 2 *DAC x16*	Control Register 5 *SSI DAC Mode*	Equation
Linear	0	0	V_{SSI} = 1.25 x SSI Average/65536
x16	1	0	V_{SSI} = 1.25 x SSI Average/4096
Log	-	1	V_{SSI} = 1.25 x (Optical Power L2 + 4096)/8192

2.4.6 Determining if There is Sufficient Optical Signal

To ensure that there is enough optical signal to satisfy the ZMI 4104 Measurement Board, for the life of the Laser Head, use the appropriate formula below.

Optical Power ≥ 0.1 µW * Power Factor

Where:

Optical Power = $2^{(\text{Opt Power L2} / 1024)}$

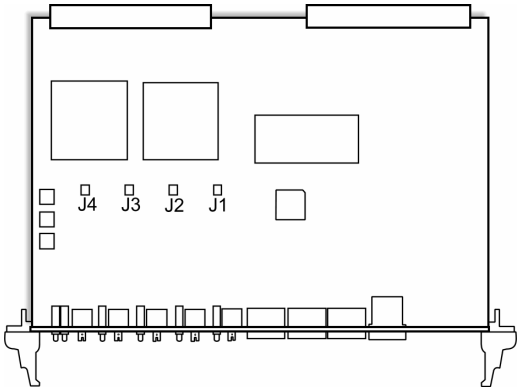
Power Factor = Current laser head optical power / Specified minimum laser head optical power

Laser Head Model	ZYGO P/N	Minimum Power
7702	8070-0102-0X	400 µW
7714	8070-0278-01	1350 µW
7722	8070-0257-02	900 µW

2.5 Test Point Characteristics

The ZMI 4100 contains on-board test points for observing the actual AC signal. The location and assignment of these test points is illustrated below. These connectors are type MMCX receptacles.

Figure 2-8 Location of Test Points



Point	Axis
J4	axis 1
J3	axis 2
J2	axis 3
J1	axis 4

2.6 Diagnostic LED's

The measurement board has two on-board diagnostic LED's.

In addition, each FPGA includes a temperature monitor located near the device. If the board is not receiving sufficient cooling air flow to keep the internal temperature below 85°C, an over-temperature error will occur and the front panel measure error LED's will flash.

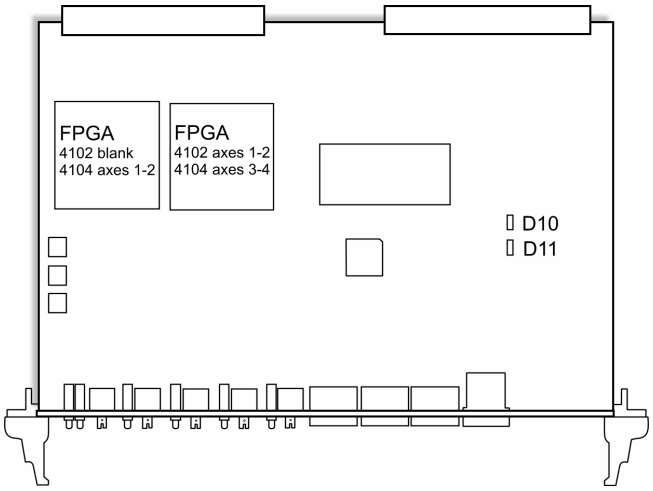
D10 Power okay LED (green) indicates status of LV (analog power) and HV (APD bias) power supplies:
Off = LV invalid.
Flashing = HV invalid, LV ok.
On = HV ok, LV ok.

These power supplies are required for measurement functions.

D11 Digital power okay LED (green) indicates status of +1.2V, +1.8V, +2.5V, +3.3V, +5V power supplies:
Off = power supplies invalid.
On = power supplies ok.

These power supplies are required for all board functions, including VME and P2 interface operation.

Figure 2-9 D10 and D11 Diagnostic LED's



2.7 Backplane and Expansion Connectors

2.7.1 P1 Backplane Connector

The P1 connector is a 160-pin DIN connector with 5 rows of pins. Rows A, B, and C are compatible with the original VMEbus specification and 96-pin backplane connectors. Rows D and Z are specified by the VME64x specification, and are compatible with the VME64 specification. Rows D and Z contain 18 additional ground pins for signal fidelity. Row D also includes 6 Geographic Address pins, GAP* and GA[4:0]*; the use of these signals is optional. The connector pinout for P1 is shown in the following table.

Due to the additional +5V power and ground pins, use of a backplane with the mating 160-pin connector is highly recommended.

Table 2-4 P1 Pin Assignments

P1 Connector					
Pin	**Row Z**	**Row A**	**Row B**	**Row C**	**Row D**
1	reserved	D00	reserved	D08	+5V
2	GND	D01	reserved	D09	GND
3	reserved	D02	reserved	D10	reserved
4	GND	D03	BG0IN*	D11	reserved
5	reserved	D04	BG0OUT*	D12	reserved
6	GND	D05	BG1IN*	D13	reserved
7	reserved	D06	BG1OUT*	D14	reserved
8	GND	D07	BG2IN*	D15	reserved
9	reserved	GND	BG2OUT*	GND	GAP*
10	GND	reserved	BG3IN*	SYSFAIL*	GA0*
11	reserved	GND	BG3OUT*	reserved	GA1*
12	GND	DS1*	reserved	SYSRESET*	reserved
13	reserved	DS0*	reserved	LWORD*	GA2*
14	GND	WRITE*	reserved	AM5	reserved
15	reserved	GND	reserved	A23	GA3*
16	GND	DTACK*	AM0	A22	reserved
17	reserved	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	reserved
19	reserved	GND	AM3	A19	reserved
20	GND	IACK*	GND	A18	reserved
21	reserved	IACKIN*	reserved	A17	reserved
22	GND	IACKOUT*	reserved	A16	reserved
23	reserved	AM4	GND	A15	reserved
24	GND	A07	IRQ7*	A14	reserved
25	reserved	A06	IRQ6*	A13	reserved
26	GND	A05	IRQ5*	A12	reserved
27	reserved	A04	IRQ4*	A11	reserved
28	GND	A03	IRQ3*	A10	reserved
29	reserved	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	reserved
31	reserved	reserved	reserved	reserved	GND
32	GND	+5V	+5V	+5V	+5V

Notes: Pins labeled “reserved” are VMEbus signals that are not used by the ZMI 4100. An * (asterisk) indicates a active-low signal.

2.7.2 P2 Backplane Connector

The P2 connector is a 160-pin DIN connector with 5 rows of pins. Rows A, B, and C are compatible with the original VMEbus specification and 96-pin backplane connectors. Rows A and C are user defined, and are used for the P2bus interface. Rows D and Z are specified by the VME64x specification, and are compatible with the VME64 specification. These rows contain additional ground pins, plus user-defined pins that are used by the measurement board. The connector pinout for P2 is shown in the following table.

Table 2-5 ZMI 4104 P2 Pin Assignments

P2 Connector					
Pin	**Row Z**	**Row A**	**Row B**	**Row C**	**Row D**
1	not used	P2_IOE*	+5V	P2_SCLK2	GND
2	GND	GND	GND	GND	P2D_SERIAL1_P
3	P2Z_SERIAL1_P	P2_A00	reserved	P2_A08	P2D_SERIAL1_N
4	GND	P2_A01	reserved	P2_A09	P2D_SERIAL2_P
5	P2Z_SERIAL1_N	P2_A02	reserved	P2_A10	P2D_SERIAL2_N
6	GND	P2_A03	reserved	P2_A11	GND
7	P2Z_SERIAL2_P	P2_A04	reserved	P2_R/W*	P2D_SERIAL3_P
8	GND	P2_A05	reserved	P2_RESET*	P2D_SERIAL3_N
9	P2Z_SERIAL2_N	P2_A06	reserved	GND	P2D_SERIAL4_P
10	GND	P2_A07	reserved	reserved	P2D_SERIAL4_N
11	P2Z_SERIAL3_P	GND	reserved	GND	GND
12	GND	P2_INT0*	GND	P2_INT1*	P2D _IN1
13	P2Z_SERIAL3_N	P2_INT2*	+5V	P2_INT3*	P2D _OUT1
14	GND	GND	D16	GND	GND
15	P2Z_SERIAL4_P	P2_D16	D17	P2_D24	P2D_ERR1*
16	GND	P2_D17	D18	P2_D25	P2D _ERR2*
17	P2Z_SERIAL4_N	P2_D18	D19	P2_D26	P2D _ERR3*
18	GND	P2_D19	D20	P2_D27	P2D _ERR4*
19	P2Z_REF20_P	P2_D20	D21	P2_D28	P2D _ERRANY*
20	GND	P2_D21	D22	P2_D29	GND
21	P2Z_REF20_N	P2_D22	D23	P2_D30	P2D _RESET1*
22	GND	P2_D23	GND	P2_D31	P2D _RESET2*
23	P2Z_SCLK1_P	P2_D00	D24	P2_D08	P2D _RESET3*
24	GND	P2_D01	D25	P2_D09	P2D _RESET4*
25	P2Z_SCLK1_N	P2_D02	D26	P2_D10	P2D _RESETALL*
26	GND	P2_D03	D27	P2_D11	GND
27	P2Z_SCLK0_P	P2_D04	D28	P2_D12	P2D _COMP1
28	GND	P2_D05	D29	P2_D13	P2D _COMP2
29	P2Z_SCLK0_N	P2_D06	D30	P2_D14	P2D _COMP3
30	GND	P2_D07	D31	P2_D15	P2D _COMP4
31	not used	GND	GND	GND	GND
32	GND	P2_SCLK0	+5V	P2_SCLK1	+5V

Notes: P2_A*xx* is P2 address, P2_D*xx* is P2 data, and D*xx* is VME data. Pins labeled “reserved” are VMEbus signals that are not used by the ZMI 4100. An * (asterisk) indicates a active-low signal.

2.8 Signal Strength Measurement

There are several methods for measuring signal strength summarized in the table below. The SSI Average is the most accurate, however it requires a successful axis reset, which would complicate operation of the APD controller.

The optical powers calculated below are in microwatts based on a photodiode responsivity of 0.44 A/W, known APD gain, typical processing gains, and a mixing efficiency (modulation) of 100%.

Unless specified as “DC”, all optical power values are based on AC optical power.

Optical Power = Optical Power DC * Mixing Efficiency
where ideal Mixing Efficiency =100%.

Register and EEPROM data names containing “L2” are log2(x)*1024, so addition and subtraction are used in calculations instead of multiplication and division.

The processing gain constant (Proc_Gain_L2) may be used to calculate optical power and signal levels more accurately. The processing gain constant is based on “Signal Strength, Nominal Signal” values in EEPROM data described in Section 3.9:

Proc_Gain_L2 = EEPROM(Sig_RMS_L2) - EEPROM(Optical_Power_L2) - EEPROM(APD_Gain_L2)

A typical value for Proc_Gain_L2 is 7200.

In the following equations, APD_Gain = $2^{(APD\_Gain\_L2/1024)}$.

Table 2-7 Signal Strength Measurement

Method	Description
Meas DC	This measures the DC component of the measurement signal using the on-board Diagnostic ADC. The dark value must be subtracted to obtain the signal value. The dark value is stored in EEPROM, and varies with temperature approximately -2.7 mV/°C. Due to the resolution of the Diagnostic ADC (2.075 mV), this value is not accurate at low signal levels. Optical_Power = $(V_D-V_L) * 1e6 / (40950 * 0.44 * APD\_Gain)$ where V_L is the Meas DC voltage (in volts) with light, and V_D is the Meas DC dark voltage.
SSI Max	This measures the maximum of the absolute value of the digitized measurement signal. This has limited accuracy at low signal levels due to ADC offset of up to ±5 mV. For stationary signals, this may be 13% low due to unknown sampling phase of the signal. Optical_Power = SSI_Max * 0.0558 / APD_Gain
Sig RMS	This measures the RMS value of the digitized measurement signal after subtracting the offset given by the SSI Offset register. This is always valid, however it is less accurate at extremely low signal levels (Sig_RMS_L2 less than 7200, or SSI Average less than 460) than optical power calculations based on SSI Average. $Sig\_RMS = 2^{(Sig\_RMS\_L2/1024)}$ Optical_Power = Sig_RMS * 0.00765 / APD_Gain or Optical_Power_L2 = Sig RMS_L2 - APD_Gain_L2 - Proc_Gain_L2 $Optical\_Power = 2^{(Optical\_Power\_L2/1024)}$
SSI Average	This measures the RMS value of the digitized measurement signal in the frequency range of interest. This is always valid for signals at 20 MHz. At other signal frequencies, this is valid only after an axis reset with no fatal errors. The optical power may be calculated based on values stored in EEPROM. Typical values are: Optical_Power = SSI_Average * 0.00218 / APD_Gain
Optical Power	The APD controller uses the Sig RMS L2, APD Gain L2, and Proc_Gain_L2 values to calculate the input optical power. $Optical\_Power = 2^{(Optical\_Power\_L2/1024)}$ The "*Enable Aux Data* bit in Control Register 2 must be enabled to access these values.
Optical Power DC	The APD controller uses the Meas DC and APD Gain L2 values to calculate the input DC optical power. $Optical\_Power\_DC = 2^{(Optical\_Power\_DC\_L2/1024)}$ The "*Enable Aux Data* bit in Control Register 2 must be enabled to access these values.

2.9 Measurement Performance

The measurement "noise" of the ZMI 4100 is directly related to the optical signal power delivered to the receiver. Figure 2-10 shows the typical relationship between optical power and noise for several values of APD gain. The higher gains provide less noise at low optical power, but are limited by saturation at high optical power. Also refer to section 1.6.1 Optical Power Range.

Figure 2-10 Noise versus Optical Power

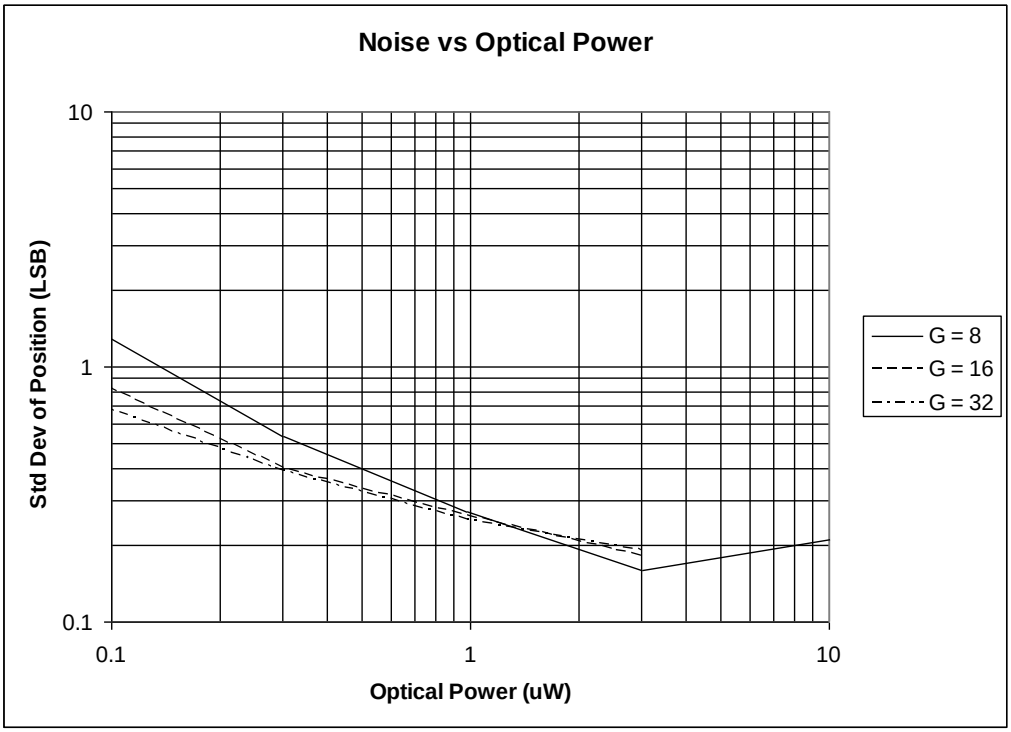
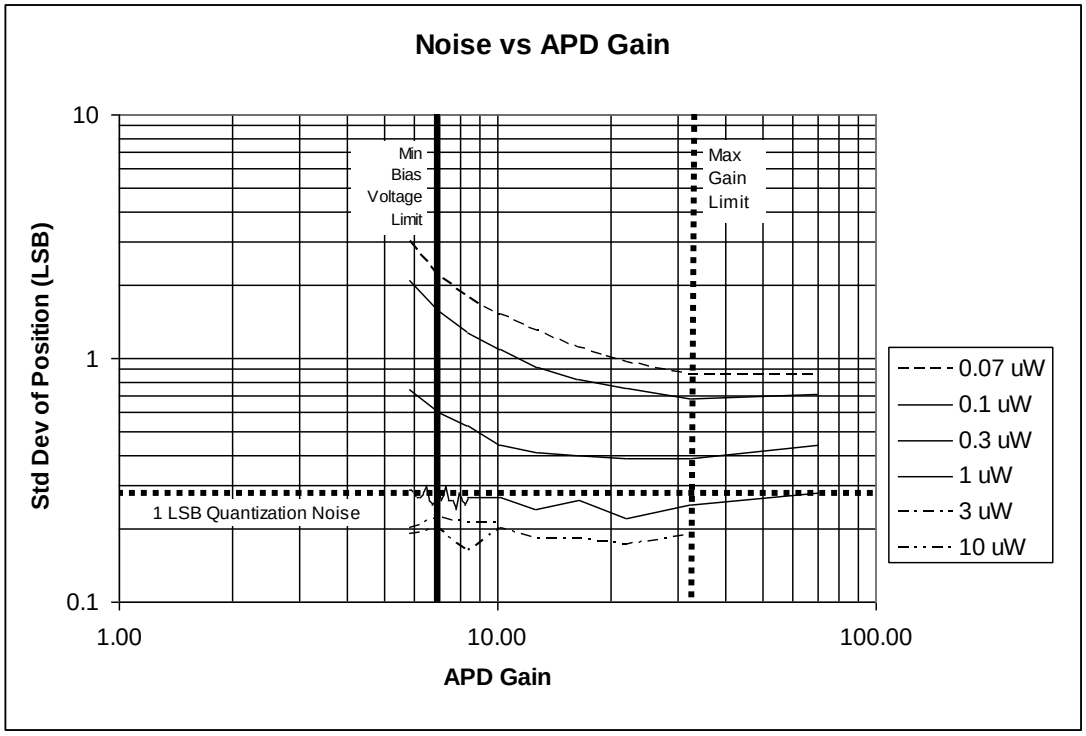


Figure 2-11 shows the typical relationship between APD gain and noise for several optical powers. This figure illustrates three limits:

1. Minimum bias voltage limit. Below the minimum bias voltage, the APD performance degrades significantly. The minimum bias voltage does not vary with temperature, although the gain that it represents does vary with temperature. The ZMI 4100 limits the bias voltage, and provides the actual gain in the APD Gain L2 register.
2. Maximum gain limit. Above the maximum gain limit, the APD excess noise increases. The ZMI 4100 limits the gain, and provides the actual gain in the APD Gain L2 register.
3. Quantization noise limit. With an output quantization of 1 LSB, the quantization noise of the output may be greater than the noise of the measurement. In that case, the *VME Bit Window* (Control Register 2), *P2 Bit Window* (Control Register 4), or Position Extension registers may be used to access up to three fractional bits.

Figure 2-11 Noise versus APD Gain



Chapter 3 Description

3.1 Using the Measurement Board

The measurement board is a register-based VME card that supports four measurement axes. Due to the special functions included in the measurement board, the user must program some parameters using the VMEbus before operating the ZMI.

The board is initialized and all bits in the control registers are cleared when the board receives an active SYSRESET* signal from the VMEbus or when power is turned off and then back on, depending on the *Disable VME SYSRESET* Input* bit in Control Register 16 (bit 2). After the system is reset, the board responds to A24 cycles.

When powered up, the laser head takes a number of minutes to stabilize. The Status Register 0, *Reference Present* bit (bit 1), indicates when the system is ready to make a measurement. It will go high after the laser head stabilizes. The *Reset Axis* bit in the Command Register (bit 6) should be asserted at this point to clear any errors generated during warm-up.

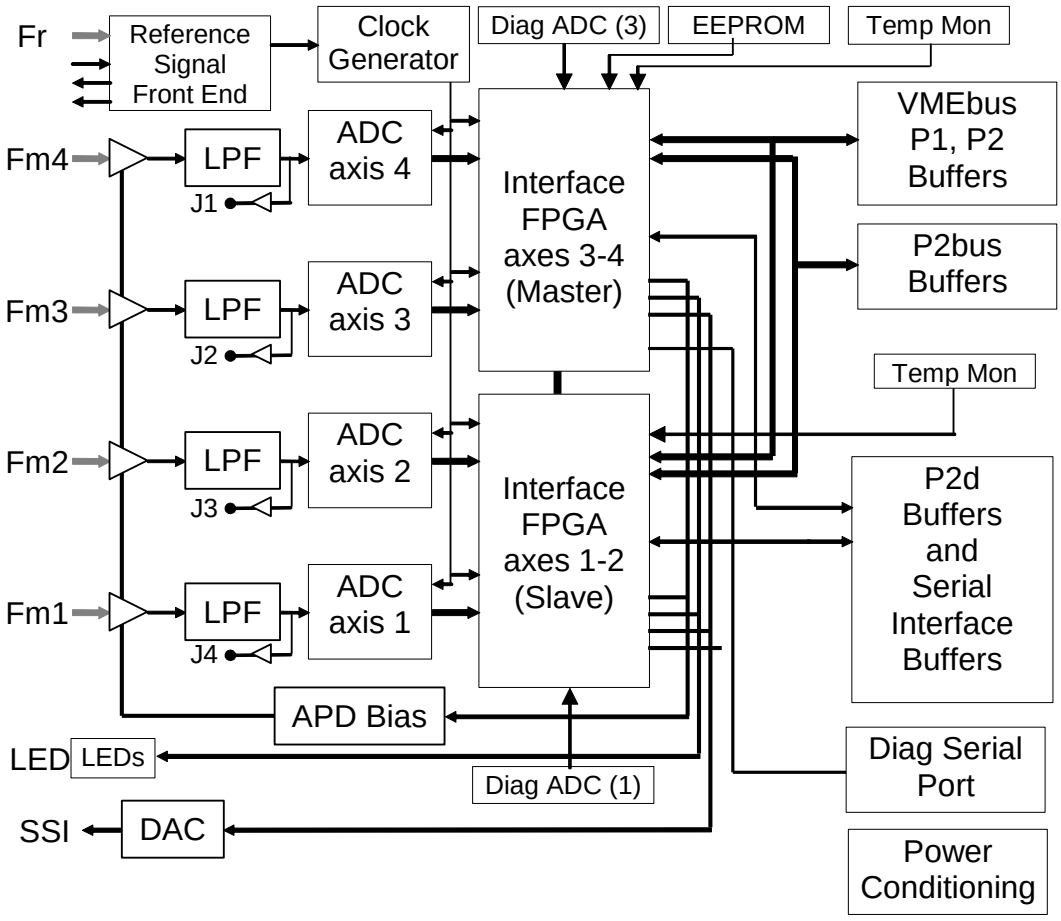
The user *may* program many register functions during warm-up, such as: Kp and Kv filter settings, interrupt vector, P2 interrupt control bits, and Data Age Adjust register bits.

Making measurements with the board consists of accessing the appropriate registers to control interrupts, setting the offset position, sampling and reading the position, velocity, and time. Each register is described in detail in Chapter 4.

Most VME and P2 registers exist for each axis on the board, as shown in Table 4-1. For the ZMI 4104 board, the processing is divided among two FPGA devices, one for axes 1 and 2, and one for axes 3 and 4. Some registers or register bits exist only for axis 3, but represent the entire board. Some registers or register bits exist for axis 1, which also represents axis 2; and for axis 3, which also represents axis 4.

3.2 Board Block Diagram

Figure 3-1 ZMI 4104 Board Block Diagram



3.3 VMEbus Interface

The VMEbus interface is the primary interface to the board. All registers, memory, and diagnostic functions are accessible through the VMEbus interface. All board power is supplied through the P1 and P2 VMEbus connectors.

The following VME64 or VME64x capabilities are implemented:

A24	Only 24-bit addressing is recognized due to the large (14-bit) address space required by this architecture. The base address is set by two rotary switches or by one rotary switches and the VME64x backplane Geographical Address signals as described in Table 3-1.
D16:D32	32-bit or 16-bit data is used, as requested by the bus master.
I(1-7):D08(O):RORA	Interrupts 1-7 are available (specified by a control register), single byte interrupt acknowledge, remove interrupt on write to command register.
+5V	The board requires +5V power.
ESD	The board supports the VME64x ESD (electrostatic discharge) scheme with ESD discharge strips along the board edge.
GA:GAP	The VME64x geographical address capability is optional, controlled by an on-board switch. See Table 3-1.
P1/160:P2/160	The board uses the 160-pin DIN connectors optional in VME64, but required by VME64x. Each connector has 16 additional ground pins and additional power pins, improving signal fidelity. Most of the additional Row Z and Row D user-defined pins are used.
IEL/HDL	The board uses locking injector/ejector handles specified by VME64x and IEEE Std 1101.10 to accommodate the greater forces required by the 160-pin connectors. The front panel retaining screws are no longer required, but remain for compatibility with subracks lacking the retaining hardware.
EMC	The board uses VME64x EMC front panels.

The following capabilities, new to VME64 or VME64x, are *not* implemented:

+3.3V	The board does not require external +3.3V power. The board uses 3.3V bus drivers, and has an on-board regulator to supply their power.
CR/CSR	The configuration ROM and control and status registers s are not implemented. Similar functionality is obtained in other ways.
Lock	Locked cycles are not supported.
KEY	Mechanical keying is not supplied, but may be added by the customer.
D64	The 64-bit data transfer is not supported.
RETRY	Cycle retry is not supported.

3.3.1 VMEbus Addressing

The VMEbus base address is selected in one of two ways:

- If SW5-2 is "1" (off), the base address is manually set by SW1 and SW2. If the backplane has VME64x Geographical Address (GA) capability, the slot number can be read in the Test Status 0 register.
- If SW5-2 is "0" (on), the Geographical Address (GA) capability provided by VME64x is used. With the GA feature, the address switches can be set the same on every board in the system, greatly simplifying configuration. In this mode, the upper four bits of the base address are set with SW1, and the next five bits are set by the GA bits. If the GA bits have bad parity, indicating a backplane without GA capability, the GA is ignored and SW1 and SW2 are used.

Table 3-1 VME Base Address

SW5-2	SW1	SW2	SW4	GA(4:0)	A15	A14	Axis #	Offset
0 (on)	A(23:20)	-	-	A(19:15)	-	0	A(13:12)	A(11:1)
0 (on)	A(23:20)	A(19:16)	-	Bad parity	1	1	A(13:12)	A(11:1)
1 (off)	A(23:20)	A(19:16)	-	-	0	1	A(13:12)	A(11:1)

The board responds only to address modifier codes 0x39 (A24 non-privileged data access) and 0x3D (A24 supervisory data access).

3.3.2 VMEbus Operation

The operation and timing of the VMEbus is specified fully in the VMEbus standards, and is not included here. A number of details require additional explanation, they are listed below.

- The VME SYSFAIL* signal is driven low during FPGA configuration, and returns high when configuration is done. This provides an indication to the processor when all axes on all boards are configured. If an axis is not configured, an attempted VMEbus access will result in a bus error and the board will not propagate the IACKIN* signal to IACKOUT*. There is no status bit indicating the configuration state.
- Previous ZMI products had an on-board jumper to disconnect the VME SYSRESET* signal from the on-board powerup reset signal. This product provides that capability through the *Disable VME SYSRESET* Input* bit in Control Register 16.
- The VME SYSRESET* signal, when enabled, resets all logic functions, registers, and data for all axes. It does not reset the FPGA configuration.
- The ZMI 4100 Measurement Board does not use the Bus Grant (BG0IN* - BG3IN* and BG0OUT* - BG3OUT*) signals. Each Bus Grant input is directly connected to the corresponding output to allow use in a multi-master system.
- The LI/O* pin (P1-D29) is tied low to allow use of backplanes with an electronic automatic daisy-chain.

3.3.3 VMEbus Interrupts

The VMEbus interrupts are enabled by the VME Interrupt Enable register. The VME Interrupt Vector register controls the operation of the VMEbus interrupts as described below.

- *VME Interrupt Enable*. If this bit is set in VME Interrupt Enable 1 register, the interrupt will be asserted on the VMEbus.
- *VME Interrupt Level*. The VME interrupt level is specified by the these bits (VIL0-2). If the bits are all zero, no interrupt occurs.
- *VME Interrupt Vector*. This specifies the 8-bit value that the VME Master will read during a VMEbus IACK (Interrupt Acknowledge) cycle after the interrupt occurs.

3.4 P2bus Interface

The P2bus is a proprietary high speed 32 bit bus capable of 10 MHz 32-bit transfer rates under certain conditions. All signals use TTL logic levels. For best results, the P2 backplane should have bussing and termination similar to that provided for the VME backplane.

Due to the limited 12 bit address space, the diagnostic registers, diagnostic data RAM, and dynamic data age RAM are not accessible through the P2 bus. Board initialization should be done via the VMEbus so that complete powerup diagnostics and initialization may be performed.

3.4.1 P2bus Addressing

The P2bus enable and base address, are set by bits in Control Register 17. These bits must be set in both axis 1 (for axes 1 and 2) and axis 3 (for axes 3 and 4). These bits may be changed only by a VMEbus master. Access from the P2bus may read theses bits, but can not change them.

The P2bus base address is selected in one of two ways as shown in Table 3-2. If SW5-1 is “0” (on), the P2 base address is set by the *P2 Address P2A8* to *P2A11* bits of Control Register 17. Note that this register must be initialized on both axes 1 and 3.

To prevent possible bus contention if the P2 address has not been set, the P2 bus is non-functional after powerup until the *P2 IO Enable* bit in Control Register 17 is set to a “1”. This bit should not be set until after the base address has been set on all axes on all boards. This bit can only be changed by a VMEbus master. The powerup state of this bit depends on the setting of SW5-1, as shown in Table 3-2.

The P2 interface *only* supports 32-bit access. Only even (P2_A00 = 0) P2 addresses may be used. When reading or writing a 16-bit register, the register with the even address is in bits 31-16, and the register with the next higher (odd) address is in bits 15-0. For example, Control Register 0 and Control Register 1 must always be read or written as a single 32-bit register at address offset 0x08.

Table 3-2 P2 Base Address

SW5-1	SW4	P2 Address register	Axis #	Offset	Powerup Default	
					State	*P2 IO Enable*
0 (on)	-	P2_A(11:8)	P2_A(7:6)	P2_A(5:0)	Disabled	0
1 (off)	P2_A(11:8)	-	P2_A(7:6)	P2_A(5:0)	Enabled	1

3.4.2 P2bus Signals

Refer to following table for a summary of the P2 signals. An asterisk(*) following a signal name indicates an active low signal. P2 pin assignments are listed in Chapter 2.

Table 3-3 P2 Bus Signal Descriptions

P2 pins	Signal	Description
P2_D00 to P2_D31	tri-state I/O	P2 data bus. P2_D31 is the most significant bit and P2_D0 is the least significant bit.
P2_A0 to P2_A11	inputs	The address bus for the P2 interface. A11 is the most significant bit and A0 is the least significant bit. The base address is set as described in a previous section.
P2_RW*	input	Read/Write, high for read, low for write.
P2_RESET*	input	P2 reset signal. The action of this signal is described in the next section.
P2_INT0* to P2_INT3*	outputs	P2 interrupt lines. The configuration of these signals is described in "P2bus Interrupts" in this chapter.
P2_SCLK0 P2_SCLK1	input/ output	Sample Clock 0 and 1. These are used to sample multiple axes at the same instant while minimizing the data age uncertainty between the samples. The VME, P2, Serial, and High Speed Position outputs may select which SCLK causes sampling to occur. These signals are driven by the first board in the reference tree and received by all other boards. These signals are not intended to be driven by user hardware. SCLK can cause one sample at a time using the External Sample bits in the SCLK Command Register or produce periodic sampling as specified by the Sample Timer register.
P2_SCLK2	input	Sample Clock 2. This signal may be driven by user hardware into the first board in the reference tree when an externally generated sample signal is required. This signal must have a minimum width of 100 ns. The input is synchronized to the 20 MHz reference clock, then output to all boards as SCLK0 or SCLK1 as specified by the SCLK2 Resync Drive bit in Control Register 17. The SCLK2 input polarity and enable is controlled by the SCLK2 Resync Mode bits in Control Register 17.
P2_IOE*	input	I/O Enable, active-low during a read or write cycle. The address lines and the P2_RW* signals must be stable when this line goes low, as shown in the timing diagrams.
P2Z_REF20P/N	outputs	Differential output of 20MHz Reference Clock. Enabled when either the SCLK0 or SCLK1 bus outputs are enabled.
P2Z_SCLK0P/N, P2Z_SCLK1P/N	outputs	Differential output of SCLK0 and SCLK1. Enabled when either the SCLK0 or SCLK1 bus outputs are enabled.

3.4.3 P2bus Reset

The Measurement Board uses the P2_RESET* signal to perform a position reset, quick position reset, time reset, and/or error latch reset. This is not a global reset like the VMEbus SYSRESET* signal. Bits in Control Register 4 select which reset operations occur when the P2_RESET* signal is activated. The combination of all five resets is the same as an axis reset. The power-on default condition is that no reset operation is selected. If the *P2d Reset All* bit in Control Register 3 is set, the P2d bus RESETALL* signal is ORed with the P2_RESET* signal, and both function in an identical manner.

3.4.4 P2bus Timing

P2bus Read Cycle Timing

An interface board can read data values from the ZMI measurement boards through the P2bus. The latch mode for measurement data is determined by the *P2 Latch Mode* bit in Control Register 4. The data can be latched either by the SCLK0 or SCLK1 signal (default, *P2 Latch Mode* = 0), or by the falling edge of P2_IOE* (*P2 Latch Mode* = 1) during the read operation. Data latching by SCLK0 or SCLK1 allows faster data access during the read operation.

The P2bus read timing diagram, when reading data from a Measurement Board with previously latched data, is shown in the following figure and Table 3-4.

Figure 3-2 P2bus Read

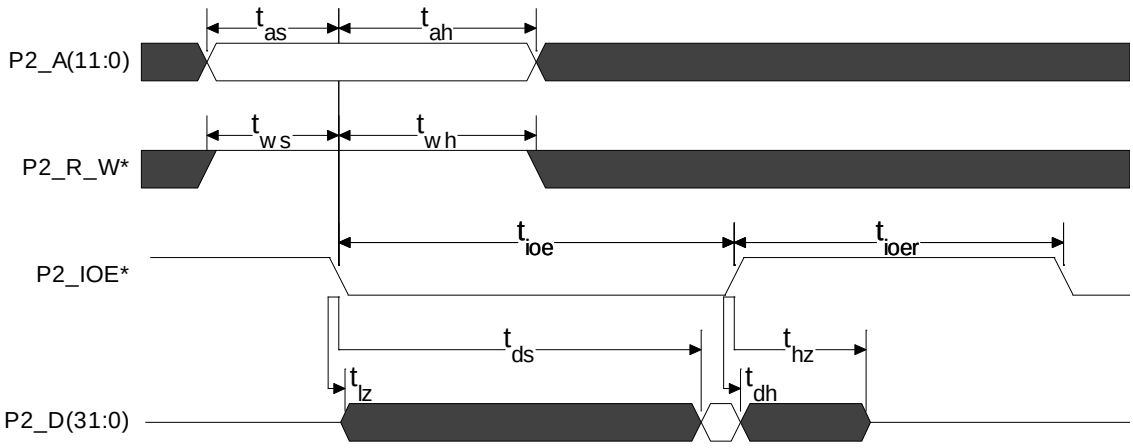


Table 3-4 P2bus Read

Time	P2 Master	P2 Slave		Description
t_{as}	20 ns	10 ns	min	Address Setup time
t_{ah}	30 ns	20 ns	min	Address Hold time
t_{ws}	20 ns	10 ns	min	Write Setup time
t_{wh}	30 ns	20 ns	min	Write Hold time
$t_{ioe\ (P2)}$	50 ns	40 ns	min	P2_IOE* read recovery time, P2_IOE* latched data
$t_{ioe\ (SCLK)}$	40 ns	30 ns	min	P2_IOE* read recovery time, SCLK latched data
t_{ds}	80 ns	60 ns	max	Data setup from P2_IOE* low, P2_IOE* latched data
t_{ds}	55 ns	35 ns	max	Data setup from P2_IOE* low, SCLK latched data
t_{dh}	0 ns	0 ns	min	Data hold from P2_IOE* high
t_{lz}	0 ns	0 ns	min	P2_IOE* low to active output
t_{hz}	20 ns	20 ns	max	P2_IOE* high to high Z output

The standard timing restricts the transfer rate to approximately 6 MHz The maximum theoretical P2bus 32-bit data transfer rate for SCLK latched data is 10.0 MHz. The design of the P2 bus master and sampling time requirements may additionally limit the maximum system transfer rate. For additional information, contact ZYGO applications engineering.

P2bus Write Cycle Timing

The timing for the P2bus write cycle is shown in the following figure and Table 3-5.

Figure 3-3 P2bus Write

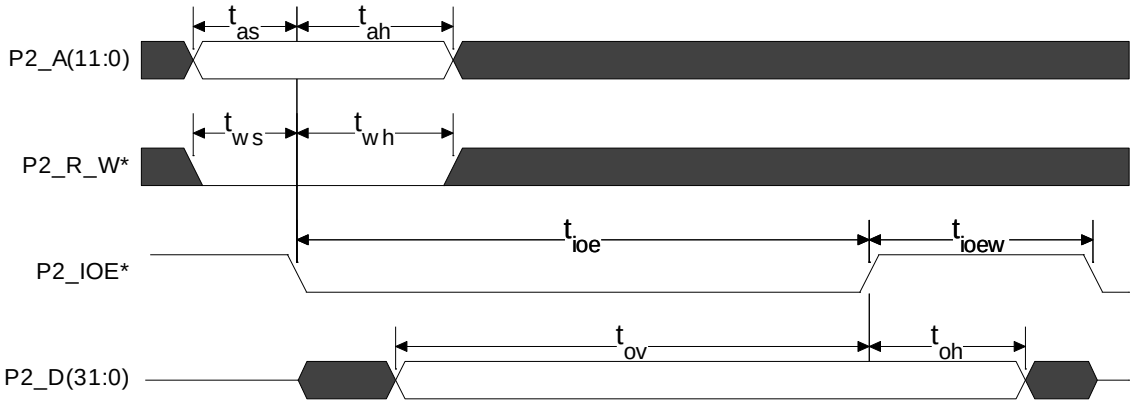


Table 3-5 P2bus Write

Time	P2 Master	P2 Slave		Parameter
t_{as}	20 ns	10 ns	Min	Address Setup time
t_{ws}	20 ns	10 ns	Min	Write Setup time
t_{ioew}	120 ns	110 ns	Min	P2_IOE* write recovery time
t_{ah}	30 ns	20 ns	Min	Address Hold time
t_{wh}	30 ns	20 ns	Min	Write Hold time
t_{ov}	90 ns	80 ns	Min	Data Valid before end of P2_IOE*
t_{oh}	30 ns	20 ns	Min	Data hold from IOE high

Position Sampling with SCLK

The following figure shows timing for P2 read of position, time, or velocity data that has previously been latched by SCLK. This timing information applies to any number of P2 cycles per SCLK and an SCLK period of 150 ns or greater. For additional information, contact ZYGO applications engineering.

Figure 3-4 Position Sampling with SCLK

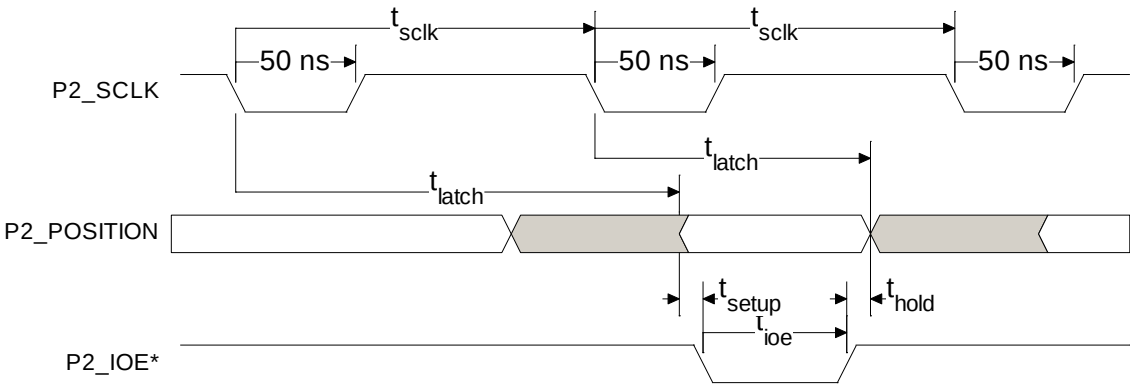


Table 3-6 Position Sampling with SCLK

Time	Slave		Parameter
t_{latch}	115 ns	Min	Time from falling edge of SCLK until internal position latch.
t_{latch}	185 ns	Max	Time from falling edge of SCLK until internal position latch
t_{setup}	0 ns	Min	Position setup time for read after SCLK latching
t_{hold}	0 ns	Min	Position hold time for read before next SCLK latching

3.4.5 P2bus Interrupts

Error conditions are latched in the P2 Error Status register. All error conditions can generate interrupts. The user writes a 1 into the desired bits of the P2 Interrupt Enable register to determine which errors generate interrupts on the P2 interface. The power-on default condition is all mask bits set to no interrupts.

To clear interrupts, the user writes a 1 into the desired bits of the P2 Error Clear register.

The P2 interrupt level is set by the *P2 Int Level* bits (*PIL0* and *PIL1*) in Control Register 4 as shown in the following table.

Table 3-7 P2 Interrupt Levels

Interrupt Level	PIL1	PIL0
INT0	0	0
INT1	0	1
INT2	1	0
INT3	1	1

The P2 interrupts drivers are open-collector active-low with enables controlled by the *P2 Int Driver* bit (*PID0*) in Control Register 4 as shown in the following table.

Table 3-8 P2 Interrupt Drivers

Interrupt Driver	PID0
None	0
Open Collector Active Low	1

The open collector active-low choice is used since it allows multiple boards to share interrupts, prevents driver damage from incorrect setup, and a board may be missing without causing an interrupt. For use with the open-collector driver, the interrupt signals should have a 330Ω pull-up resistor on the backplane or on the bus master.

3.5 P2d Interface

The P2d interface contains the following signals. The pin connections are part of P2 as shown in Chapter 2.

Table 3-9 P2d Interface Signals

Signal	Description
P2d_ERR1* P2d_ERR2* P2d_ERR3* P2d_ERR4*	One error output for each applicable axis. The error output goes low if any measurement error occurs, as indicated by bits in the error status register. If the *Error Output Source* bit in Control Register 0 is zero, the measurement error bits in the VME Error Status register are used, otherwise the measurement error bits in the P2 Error Status register are used.
P2d_ERRANY*	One combined error output, which is the OR of the individual axis error outputs.
P2d_RESET1* P2d_RESET2* P2d_RESET3* P2d_RESET4*	One reset input for each applicable axis. The action of these signals is described later in this chapter.
P2d_RESETALL*	One reset input for all axes. The action of this signal is described later in this chapter.
P2d_COMP1 P2d_COMP2 P2d_COMP3 P2d_COMP4	One comparator output for each applicable axis. The comparators are described later in this chapter.
P2d_IN1	One user input. This bit may be read as the *User P2d In* bit of Status Register 1, VME Position Errs, VME Sample Position Errs, or P2 Sample Position Errs registers for any axis.
P2d_OUT1	One user output. This bit is controlled by the *User P2d Out* bit of Control Register 16 for axis 3 This bit may be read back by the *User P2d Out* bit of the VME Position Errs, VME Sample Position Errs, or P2 Sample Position Errs registers for the same axis. Reading or writing this bit on other axes has no relation to the external hardware.

3.6 Serial Interface

The serial interface provides a separate output for each axis. The data for each axis is separately transmitted on a differential pair over P2 on the P2d and P2z pins. The serial data is transmitted LSB first at 40 Mbits/sec, and includes the bits shown in Table 3-10. The error check bits are a Hamming code that allows correction of any single bit error and detection of any double bit error. The bit order is shown in Table 3-12. The error flag bit is sampled at the same time the position data is sampled. This is described in detail in Section 4.2.

For possible customer use, the SCLK0, SCLK1 and 20 MHz reference clocks are also available as differential signals on the P2z connector. These three outputs are enabled if either the SCLK0 or SCLK1 bus outputs are enabled.

The data packet includes either 32 or 37 bits of data as selected by the *Serial Data Size* bit in Control Register 15 (0 = 32 bits, 1 = 37 bits). All axes in a system, and the interface that they

connect to, must use the same serial size. For both 32-bit and 37-bit modes, the bit window is specified by the *P2 Bit Window* bits in Control Register 4. The data is sampled by either SCLK0 or SCLK1 as specified by the *SCLK Serial Sample In* bit in Control Register 15 of axis 1 and axis 3.

All four P2Z serial output drivers are enabled by the *Serial Output Enable P2Z* bit in Control Register 15 of axis 3. All four P2D serial output drivers are enabled by the *Serial Output Enable P2D* bit in Control Register 15 of axis 3. Data transmission is enabled by the *Serial Data Enable* bit in Control Register 2 of the specified axis. The time from the falling edge of SCLK to the falling edge of the serial output start bit is approximately 230 ns at the P2 connector. This delay is constant for any axis, but depends on SCLK timing (+/- 25 ns), and the setting of the SCLK Delay and the trigger delay enable settings in Control Register 16 and Control Register 17.

Table 3-10 Serial Interface Data

32 bit Data	37 bit Data	Description
1	1	Start bit
32	37	Data bits
1	1	Error flag bit
15	20	Error Check bits
1	1	Stop bits
50	60	Total

The maximum output rate for the serial interface is limited by the following considerations:

- The period must be a multiple of 50 ns.
- The maximum output rate from the ZMI 4100.
- The maximum input rate of the serial interface that is receiving the data.
- The throughput of the system using the serial interface data.

Table 3-11 Serial Interface Maximum Output Rates

	ZMI 4100	ZMI 4100 with ZYGO PMC Card
32-bit	769 kHz (1.30 us period)	714 kHz (1.40 us period)
37-bit	588 kHz (1.70 us period)	588 kHz (1.70 us period)

Table 3-12 ZMI Serial Bus Transfer Format

37 bit Position Words

BIT #	*P/D*	
59	Stop	
58	P(4)t	
57	Pos<36>	
56	P(4)8	
55	Pos<35>	
54	Pos<34>	
53	Pos<33>	
52	P(4)4	
51	Pos<32>	
50	P(4)2	
49	P(4)1	
48	P(3)t	(16,11)
47	Zmi_err	
46	Pos<31>	
45	Pos<30>	
44	Pos<29>	
43	Pos<28>	
42	Pos<27>	
41	Pos<26>	
40	P(3)8	
39	Pos<25>	
38	Pos<24>	
37	Pos<23>	
36	P3(4)	
35	Pos<22>	
34	P(3)2	
33	P(3)1	
32	P(2)t	(16,11)
31	Pos<21>	
30	Pos<20>	
29	Pos<19>	
28	Pos<18>	
27	Pos<17>	
26	Pos<16>	
25	Pos<15>	
24	P2(8)	
23	Pos<14>	
22	Pos<13>	
21	Pos<12>	
20	P(2)4	
19	Pos<11>	
18	P(2)2	
17	P(2)1	
16	P(1)t	(16,11)
15	Pos<10>	
14	Pos<9>	
13	Pos<8>	
12	Pos<7>	
11	Pos<6>	
10	Pos<5>	
9	Pos<4>	
8	P(1)8	
7	Pos<3>	
6	Pos<2>	
5	Pos<1>	
4	P(1)4	
3	Pos<0>	
2	P(1)2	
1	P(1)1	
0	Start	

32 bit Position Words

BIT #	*P/D*	
49	Stop	
48	P(3)t	(16,11)
47	Zmi_err	
46	Pos<31>	
45	Pos<30>	
44	Pos<29>	
43	Pos<28>	
42	Pos<27>	
41	Pos<26>	
40	P(3)8	
39	Pos<25>	
38	Pos<24>	
37	Pos<23>	
36	P3(4)	
35	Pos<22>	
34	P(3)2	
33	P(3)1	
32	P(2)t	(16,11)
31	Pos<21>	
30	Pos<20>	
29	Pos<19>	
28	Pos<18>	
27	Pos<17>	
26	Pos<16>	
25	Pos<15>	
24	P2(8)	
23	Pos<14>	
22	Pos<13>	
21	Pos<12>	
20	P(2)4	
19	Pos<11>	
18	P(2)2	
17	P(2)1	
16	P(1)t	(16,11)
15	Pos<10>	
14	Pos<9>	
13	Pos<8>	
12	Pos<7>	
11	Pos<6>	
10	Pos<5>	
9	Pos<4>	
8	P(1)8	
7	Pos<3>	
6	Pos<2>	
5	Pos<1>	
4	P(1)4	
3	Pos<0>	
2	P(1)2	
1	P(1)1	
0	Start	

3.7 SSI Interface

A front panel connector allows measuring a DC voltage that is proportional to the AC signal strength. Signals for all four axes are provided on a single connector. The pin connections for the SSI connector are shown in Chapter 2.

If the *Enable SSI DAC Test Mode* bit in the Test Control 0 register is set, the value in the SSI DAC Test register is used to set the DC output voltage level. This mode may be used for diagnostics, or to allow the host software to output any desired quantity as an analog value.

For better observation of low signal levels, set the *SSI DAC x16* bit in Control Register 2. This multiplies the SSI DAC voltage by 16, up to the maximum output of 1.25 V. Note that this mode of output does not indicate actual optical power because it does not consider APD gain. Optionally, the *SSI DAC Mode* bit in Control Register 5 can be set, this results in the SSI voltage proportional to the logarithm of the optical signal power.

3.8 Operation

3.8.1 Powerup

At powerup, the FPGA devices are configured from a serial PROM. During configuration, the VMEbus SYSFAIL* signal is asserted, and the front panel Config LED is lit. After configuration, the SYSFAIL* signal is deasserted, and the front panel Config LED is turned off. The time from backplane powerup to deassertion of SYSFAIL* is less than five seconds.

The VMEbus SYSRESET* signal resets all axes and internal FPGA control register contents and states, but does not cause SYSFAIL* to be asserted or FPGA reconfiguration. The *Disable VME SYSRESET** bit in Control Register 16 of axis 1 and axis 3 prevents SYSRESET* from affecting board operation in any way.

3.8.2 Reset

The Axis Reset resets only the data processing and error conditions, and does not affect axis configuration. An axis reset is identical to the combined effect of the Position Reset, Time Reset, P2 Error Reset, and VME Error reset. Note that due to minor timing differences, simultaneous multi-axis reset commands may result in some axes actually being reset one reference clock period (50 ns) later than other axes. Axis reset resets the measurement function and all errors.

The position reset operation reinitializes the position measurement function and normally sets the position register to zero. If the *Preset Enable* bit in Control Register 3 is 1, the position reset loads the value specified by the Preset Pos registers. Position reset resets the measurement function, but does not reset errors.

The time reset results in immediately setting the time register to zero.

The error reset resets all errors in the corresponding error register.

The over temperature error, which causes the front panel Measure Error LED's (Err 1-4) to flash, is reset as described in the description of the Diag Temp Monitor Control register.

Resets may be performed in several ways:

- Write a 1 to the desired *Reset* bits in the VME Command Register.
- Write a 1 to the desired *Reset* bits in the P2 Command Register.
- Write a 1 to the desired *P2 Reset ... Enable* bits in Control Register 4. Then assert P2_RESET*. If the P2d_RESETALL bit of Control Register 3 is a 1, P2d_RESETALL* will perform the same action. In this mode, P2d_RESETALL* is an active low level signal.
- Write a 1 to the desired *P2d Reset ... Enable* bits in Control Register 3. Then assert P2d_RESET* for the desired axes. If the P2d_RESETALL bit of Control Register 3 is a 0, P2d_RESETALL* will perform the same action. In this mode, the operation of P2d_RESETALL* is controlled by the reset mode bit in Control Register 3 described below.
- Write a 1 to the *SCLK Reset Enable* bit in Control Register 3, and select the desired SCLK source with the *SCLK Reset Select* bit in Control Register 3. This causes a simultaneous quick position reset, time reset, P2 error reset, and VME error reset to occur on the first SCLK after an axis reset. The SCLK reset does not produce an interrupt or set the External Sample bits in the error registers.

  For this to work simultaneously in all axes, a certain sequence must be followed:

  1) Before performing the axis reset, the SCLK timer must be disabled by writing a zero to the *SCLK Timer Enable* bit in Control Register 16.
  2) Perform the axis reset by any of the above methods.
  3) Perform an external sample by writing a one to the desired *External Sample* bit in the SCLK Command register.
  4) Then enable the SCLK sampling as desired.

The P2d_RESETn* and P2d_RESETALL* inputs may operate in one of four modes, specified by the *Reset Mode* bits (*RM0-1*) in Control Register 3, shown below. Each input is independently debounced and processed.

Table 3-13 Reset Modes

RM1	RM0	Description
0	0	Disabled (default)
0	1	Rising Edge
1	0	Falling Edge
1	1	Low Level

Normally, the ZMI 4100 position reset or axis reset requires that the velocity is less than 0.1 m/sec (single pass interferometer) for a position reset or axis reset to operate properly.

The ZMI 4100 may optionally be reset at any velocity within the normal operating range. This function is enabled by the *Enable Reset Finds Velocity* bit in Control Register 3, and modified by the *RFV Mode* bit in Control Register 2. When a position reset or axis reset occurs, the firmware searches the normal operating frequency range for the maximum signal strength. The following table summarizes the capabilities of the axis reset function.

Table 3-14 Axis Reset Function

Enable Reset Finds Velocity	RFV Mode	Max Velocity * (2 pass)	Max Acceleration * (2 pass)	Search Time	Total Time **
0	-	0.1 m/s	-	-	0.12 ms
1	0 = normal	Full range	0.1 g	2.39 ms	2.49 ms
1	1 = fast	Full range	10 g	0.30 ms	0.40 ms

* During reset

** Total time is from *Reset Axis* command until *Reset Complete* status. This includes 100 µs settling time for position and SSI Average. This does not include additional delay determined by *Reset Time* setting in Control Register 3.

When an axis is reset, the signal amplitude is measured. If there is no signal, a reset failure is indicated by the *Reset Failure* error bit. When this happens, the SSI will operate normally, but position, velocity, and absolute phase measurements are disabled.

After reset, the digital filter requires a short time interval to stabilize to the actual position value. The time interval required is depends on the values selected for *KV* and *KP* in Control Register 1. The time delay from 2 µs to 256 µs is specified by the *Reset Time (RT0-2)* bits in Control Register 3. At the end of the reset time delay, the Quick Reset function sets the position value to zero or to the Preset Position value specified by the Preset Pos registers, and the *Reset Complete* bit in the VME Error Status and P2 Error Status registers is set. Typical settling time for the digital filter, shown in section 3-12, may be used as a guide for selecting the reset time setting.

If desired, the Quick Reset operation may be performed at any time in a manner similar to the other reset functions. Note that the use of quick reset could result in a later position overflow if the position where the quick reset is performed is a great distance from the position where the axis reset was performed.

If the *SCLK Reset Enable* bit in Control Register 3 is set, a Quick Reset is performed when the first SCLK (as specified by the *SCLK Reset Select* bit in Control Register 3) signal occurs after the position reset is complete. This function allows precisely synchronizing the reset operation of all axes.

3.8.3 Measurement

The position and time measurements are separately latched by the VMEbus interface and by the P2bus interface.

3.8.4 Sampling

The position, time, and velocity data may be sampled by several methods as shown in Figure 3-5 and Table 3-15.

The following figure shows the interface to the P2 SCLK signals that control external sampling. This arrangement allows sampling of the data to be either common or separate. For common sampling, the design ensures that a single SCLK sample signal will result in simultaneous sampling of all data. Separate sampling may be required where the P2bus is performing high speed data transfers, and the VMEbus is performing diagnostics.

If the VME Position data is sampled by SCLK0 or SCLK1, the *VME External Sample* interrupt must be cleared before taking the next sample. The *VME External Sample Flag* bit in Status Register 0 is automatically cleared when the VME Position register is read.

Figure 3-5 Sampling

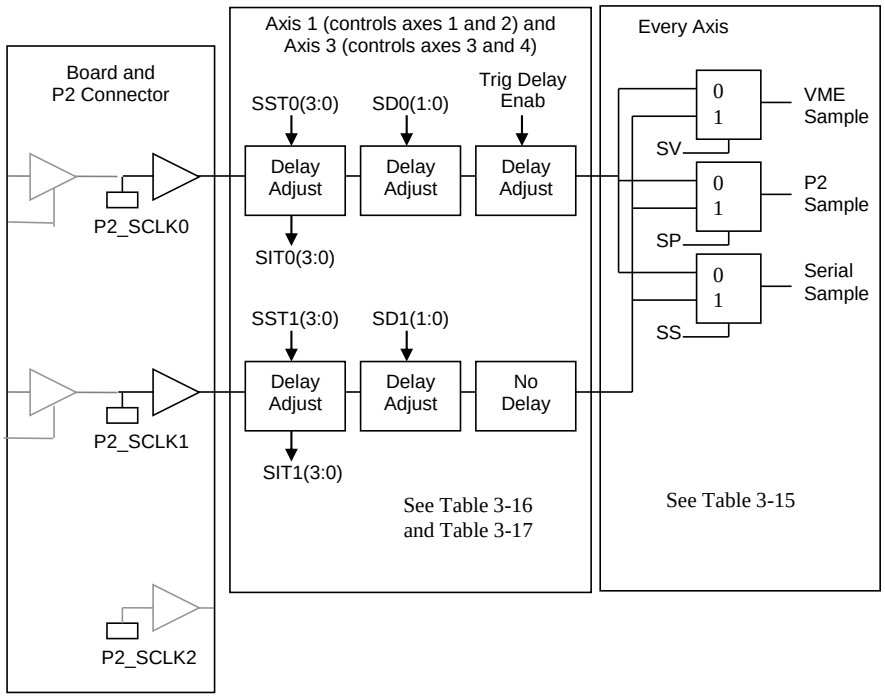


Table 3-15 Sampling

Operation	VME Sample Position	VME Position	VME Time, Velocity, Absolute Phase	P2 Position, Time, Velocity, Absolute Phase	Serial Position
VME Sample Position Read	Yes	-	Yes	-	-
VME Position Read	-	-	-	-	-
Sample VME Position command	-	Yes	Yes	-	-
P2 Position Read	-	-	-	PL=1	
SCLK0 Falling Edge	-	SV=0	SV=0	PL=0, SP=0	SS=0
SCLK1 Falling Edge	-	SV=1	SV=1	PL=0, SP=1	SS=1

Note: conditions to enable sampling are indicated by the following abbreviations:

SS = *SCLK Serial Sample In* bit in Control Register 15 of axes 1 and 3.

SV = *SCLK VME Sample In* bit in Control Register 2.

SP = *SCLK P2 Sample In* bit in Control Register 4.

PL = *P2 Latch Mode* bit in Control Register 4.

The SCLK signals may be driven by any measurement board, but for simplicity only driving from the first board in the reference tree is documented and supported. Driving of SCLK is described in the next section. The proper timing of the SCLK signals is important to achieve simultaneous sampling of all axes in a multi-axis system. The SCLK timing depends on the SCLK delay through the P2bus backplane, the delay of the reference clock as it passes through the reference tree to each board, and the setting of the coarse and fine SCLK timing adjustments.

The timing of the SCLK inputs are independently adjustable as shown in Table 3-16, and are set for both axis 1 and axis 3 to control all axes. The coarse adjustment has a range of 150 ns and a resolution of 50 ns. The fine timing has a range of 50 ns and a resolution of 8.3 ns (50 ns/6). The coarse and fine timing adjustments depend on the board location in the reference tree, and are shown in Table 3-17. The hardware has a diagnostic register that measures the timing of the falling edge of the incoming SCLK signal. The adjustment of the SCLK timing may be verified by comparing the value read with the range of values shown in Table 3-17.

Table 3-16 SCLK Timing Adjustments

Signal	Coarse Timing	Fine Timing	Diagnostic
SCLK0	*SD00-01* Control Reg 16	*SST00-03* Control Reg 16	*SIT00-03* Test Status 1 Diag Reg
SCLK1	*SD10-11* Control Reg 17	*SST10-13* Control Reg 17	*SIT10-13* Test Status 1 Diag Reg

The setting for Coarse Timing, the setting for Fine Timing, and the typical timing diagnostic values, are shown in Table 3-17.

Figure 3-6 Reference Signal Propagation

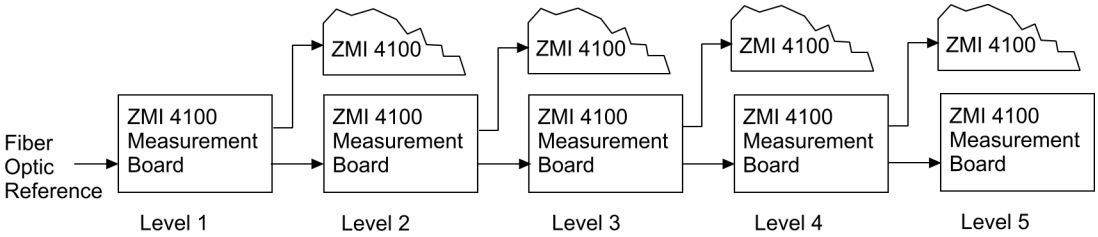


Table 3-17 Reference Propagation and SCLK Timing

Level	1	2	3	4	5
Boards at this level	1	2	4	8	16
Total boards	1	3	7	15	31
Ref In	Fiber	Electrical	Electrical	Electrical	Electrical
Ref Out	Electrical	Electrical	Electrical	Electrical	Electrical
Drives SCLK0-1	yes	no	no	no	no
Receives SCLK0-1	yes	yes	yes	yes	yes
Coarse Timing	0	0	0	0	0
Fine Timing	3	3	3	2	2
Diagnostic	1±1	1±1	0, 1, or 5	0, 1, or 5	0, 1, or 5

The *trigger delay enable* bit in Control Register 16 adds a delay to the path for external sample inputs. This delay is approximately the same as the propagation delay through the board, so that the data sampled represents the position at the time that the sample signal occurred.

3.8.5 SCLK Driving

The SCLK signals may be driven by several sources as shown in following figure and table. Note that the desired SCLK output enables should be setup before the other bits controlling the output. Axis 3 is the only axis on the board capable of driving SCLK. Each SCLK signal should only be driven by one board, otherwise improper operation and damage to the drivers may result.

Figure 3-7 SCLK Driving

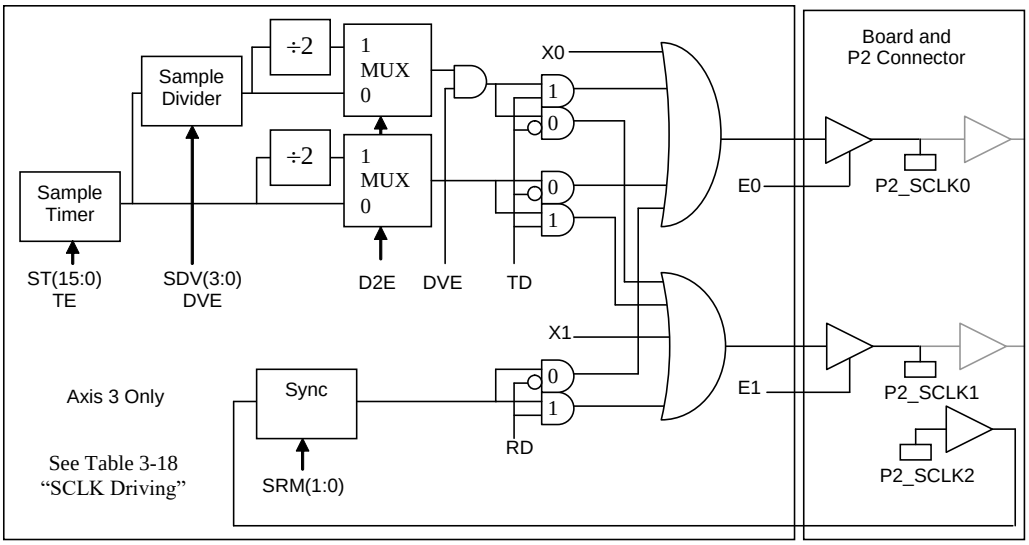


Table 3-18 SCLK Driving

Source	Setup	SCLK0 (E0 = 1)	SCLK1 (E1 = 1)
SCLK Command Register		X0 = 1	X1 = 1
SCLK Timer	TE=1	TD = 0	TD = 1
SCLK Divider	TE=1, DVE = 1	TD = 1	TD = 0
SCLK2 Resynchronized	RM > 0	RD = 0	RD = 1

Note: conditions to enable SCLK driving are indicated by the following abbreviations. These registers are on Axis 3.

X0 = *External Sample (SCLK0)* in SCLK Command Register.
X1 = *External Sample (SCLK1)* in SCLK Command Register.
E1 = *SCLK1 Out Enable* in Control Register 17.
E0 = *SCLK0 Out Enable* in Control Register 16.
TE = *SCLK Timer Enable* in Control Register 16.
TD = *SCLK Timer Drive* in Control Register 17.
SRM = *SCLK2 Resync Mode* in Control Register 17.
RD = *SCLK2 Resync Drive* in Control Register 17.

Note: The period of SCLK is determined by the following registers. These registers are on Axis 3.

D2E = *SCLK Divide-by-2 Enable* in Control Register 16.
DVE = *SCLK Divider Enable* in Control Register 16.
ST = Sample Timer Register
SDV = *SCLK Divider* in Control Register 15.

3.8.6 Data Read

The VME Position or VME Sample Position may be read as a 37-bit value or as a 32-bit value The *VME Bit Window* bits (*VBW2-0*) in Control Register 2 determine the bits being read, as shown in Table 3-19.

- For a 37-bit read, the upper bits are read from the corresponding VME Position Ext register or VME Sample Position Ext register. The VME 32-bit overflow error should not be enabled when all 37 bits are used. In addition, three fractional bits (1F to 3F) are available in the extension register that may allow increased resolution or reduced noise in some applications.
- For a 32-bit read, only the bits shown in the "VME Pos (31:0)" column of Table 3-18 are read. The VME 32-bit overflow error may be used to indicate an error if the value exceeds the range of the selected 32 bits. The sign bit is the MSB of the window, so sign reversal will occur when the data value overflows the 32-bit window.

The P2 Position may be read as a 37-bit value or as a 32-bit value The *P2 Bit Window* bits (*PBW2-0*) in Control Register 4 determine the bits being read, as shown in Table 3-20.

- For a 37-bit read, the upper bits are read from the corresponding P2 Position Ext register. The P2 32-bit overflow error should not be enabled when all 37 bits are used. In addition, three fractional bits (1F to 3F) are available in the extension register that may allow increased resolution or reduced noise in some applications.
- For a 32-bit read, only the bits shown in the "P2 Pos (31:0)" column of Table 3-19 are read. The P2 32-bit overflow error may be used to indicate an error if the value exceeds the range of the selected 32 bits. The sign bit is the MSB of the window, so sign reversal will occur when the data value overflows the 32-bit window.

Table 3-19 VME Bit Window

VBW(2:0)	* MSB	VME Pos Ext (7:0)	VME Pos (31:0)	VME Pos Ext (10:8)	Scale Factor
0 0 0	36	*, Pos (36:32)	Pos (31:0)	Pos (1F, 2F, 3F)	1
0 0 1	36	*, Pos (36:33)	Pos (32:1)	Pos (0, 1F, 2F)	2
0 1 0	36	*, Pos (36:34)	Pos (33:2)	Pos (1, 0, 1F)	4
0 1 1	36	*, Pos (36:35)	Pos (34:3)	Pos (2:0)	8
1 0 0	36	*, Pos (36)	Pos (35:4)	Pos (3:1)	16
1 0 1	36	*	Pos (36:5)	Pos (4:2)	32
1 1 0	35	*, Pos (35:31)	Pos (30:0, 1F)	Pos (2F:3F), 0	0.5
1 1 1	33	*, Pos (33:29)	Pos (28:0, 1F:3F)	0, 0, 0	0.125

Table 3-20 P2 Bit Window

PBW(2:0)	* MSB	P2 Pos Ext (7:0)	P2 Pos (31:0)	P2 Pos Ext (10:8)	Scale Factor
0 0 0	36	*, Pos (36:32)	Pos (31:0)	Pos (1F, 2F, 3F)	1
0 0 1	36	*, Pos (36:33)	Pos (32:1)	Pos (0, 1F, 2F)	2
0 1 0	36	*, Pos (36:34)	Pos (33:2)	Pos (1, 0, 1F)	4
0 1 1	36	*, Pos (36:35)	Pos (34:3)	Pos (2:0)	8
1 0 0	36	*, Pos (36)	Pos (35:4)	Pos (3:1)	16
1 0 1	36	*	Pos (36:5)	Pos (4:2)	32
1 1 0	35	*, Pos (35:31)	Pos (30:0, 1F)	Pos (2F:3F), 0	0.5
1 1 1	33	*, Pos (33:29)	Pos (28:0, 1F:3F)	0, 0, 0	0.125

Notes for Tables 3-19 and 3-20:

* Sign is extended by replicating MSB (most significant bit) in remaining bit positions.

For bit window setting “110”, bit 36 is ignored without any overflow checking. For bit window setting “111”, bits 34, 35, and 36 are ignored without any overflow checking.

3.8.7 Errors

A number of errors and other conditions are detected by the hardware. These conditions appear in three 32-bit VME registers and three 32-bit P2 registers. All the bits are the same in all registers, with only a few exceptions where noted. The registers are listed as a 16-bit "Register 0" and a 16-bit "Register 1".

- The P2 registers do not have the *VME 32 Bit Overflow* bit or the *VME External Sample (SCLK)* bit.
- The VME registers do not have the *P2 External Sample (SCLK)* bit.

An error sets the corresponding bit in the VME Error Status register and the P2 Error Status register. If desired, the error may be used to signal an interrupt by setting the corresponding bit in the VME Interrupt Enable register or the P2 Interrupt Enable register. The error interrupt also requires setting the VME Interrupt Vector register or the *P2 Int Driver* and *P2 Int Level* bits in Control Register 4. The error bits may be individually cleared by writing the corresponding bit to the VME Error Clear register or the P2 Error Clear register. The error bits may all be cleared by performing one of the reset functions described earlier in this section.

The errors and other conditions and their meanings are described in Section 4.2.

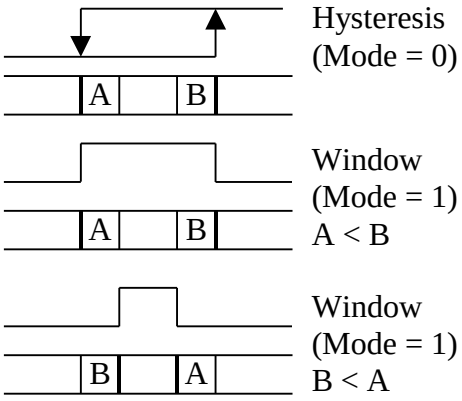
3.8.8 Comparators

Each axis has two 37-bit comparators. The *Compare Mode* bit in Control Register 2 allows selecting threshold or window operation.

When the *Compare Mode* bit is zero, the comparators function as a threshold comparator with hysteresis. A position greater than comparator B makes the comparator output go high. A position less than comparator A makes the comparator output go low. The hysteresis is equal to B-A+1. If comparator B is less than comparator A, the value in comparator B controls the output.

When the *Compare Mode* bit is one, the comparators function as a window comparator. When A < B, if the position is greater than comparator B, or less than comparator A, the output is low. When B < A, if the position is greater than or equal to A, or less than or equal to B, the output is low.

Figure 3-8 Comparator Operation



The state of the comparator (including hysteresis, and before output polarity choices) can be read in the *Comparator State* bit of Status Register 1. If the comparator is in hysteresis mode, and the position is between A and B, the state can be set to high or low using the *Comparator Preset 1* or *Comparator Preset 0* bits in the VME Command Register or the P2 Command Register.

The comparator can be used to cause a VME or P2 interrupt if the *Compare* bit in the VME Interrupt Enable or the P2 Interrupt Enable register is one. The interrupt is set when the comparator output is equal to the *Comparator Interrupt Polarity* bit in Control Register 2.

The comparator output goes to the P2d. The output buffers are enabled by the *Comparator Out Enable* bit in Control Register 2. The power-up default is disabled. The output polarity is controlled by the *Compare Out Pol* bit in Control Register 2. If the output polarity is one, the output on the P2d bus is inverted relative to the above description.

3.8.9 Position Output

The position output processing is shown in Figure 3-9. The position (P_{DF}) from the digital filter goes through the Quick Reset function.

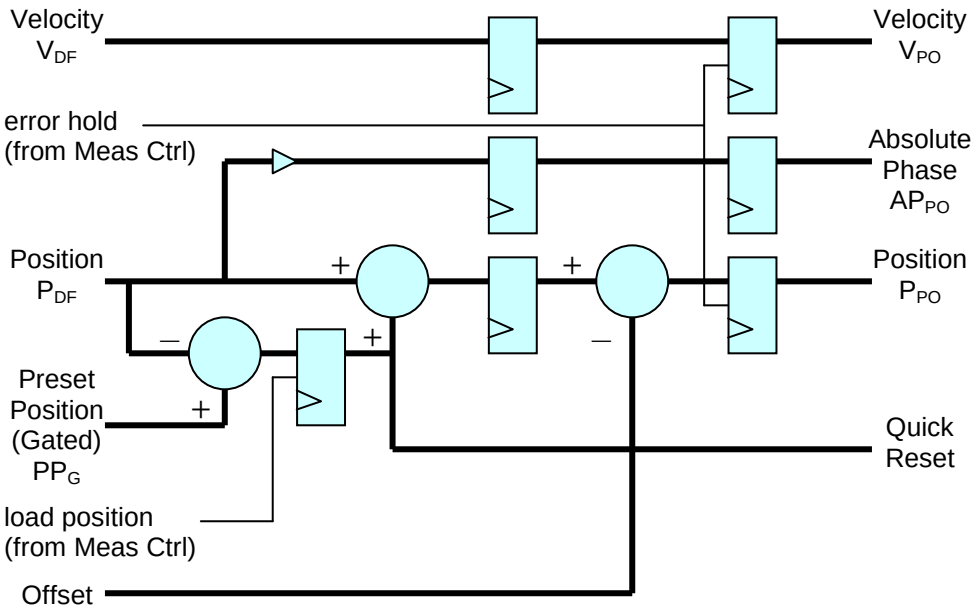
a) If *Preset Enable* in Control Register 3 is not set, the initial position value is subtracted from the position value so that the first position value (P_{PO}) is zero.

b) If *Preset Enable* in Control Register 3 is set, the Preset Position value minus the initial position value is added to the position value so that the first position value (P_{PO}) is equal to the Preset Position value.

c) If the *Disable Quick Reset* bit in Control Register 1 is set, the lower 13 bits of the quick reset register is always zero, so the lower 13 bits of the Position value contain the Absolute Phase value. The *Preset Enable* bit functions as described above.

In all cases, the Offset value is subtracted from the Position value.

Figure 3-9 Position Output



3.8.10 APD Controller Software Errors

The APD Controller uses bit 8 in VME Error Status 2 to indicate a Software Error. The upper 4 bits of Software Error ID Register identify the Software Error Type, the lower 12 bits identify the Software Error ID.

A Software Error is posted by any one of the following four conditions:

1. Exception Error.
    a. Unaligned access exceptions
    b. Timeout from the IOPB bus.
    c. Attempt to execute an illegal opcode.
    d. Timeout on the DOPB bus.
    e. Divide by zero exceptions from the hardware divide.
2. Stack Overflow.
3. Switch Default error - running into a Switch Default statement that should not have been executed.
4. Comm. Error (Rx Overflow).

All of the above conditions cause a Fatal Error except for the Divide by Zero Exception and Comm. Error. If the Software Error ID is not a Divide by Zero Exception or Comm. Error then the APD Controller does the following:

a. Shut down High Voltage Supply.
b. Set fatal error on all axes.
c. The APD Controller moves to a Fatal Error State.

Description of Software Errors

Exception Error Type

The following lists the Error ID and Exception Error Type:

0x00	No Software Error
0x01	Exception Error
0x02	Stack Overflow
0x03	Switch Default Error
0x04	Comm. Error

Exception Error ID

The following shows the ID number and definition for each of the possible Exception Errors:

0x00	No Exception Error
0x01	Unaligned access exception
0x02	Timeout from the IOPB bus exception
0x03	Illegal op code execution exception
0x04	Timeout on the DOPB bus exception
0x05	Divide by zero exception (from a hardware divide)

Stack Overflow ID

There is no Error ID for Stack Overflow

Switch Default Error ID

Currently there are 14 switch defaults that are covered by Error handling, each of those defaults having a unique Error ID.

Comm. Error ID

There is currently only one error ID for Comm. Error:

0x01	Receive Overflow

3.9 EEPROM Address Map

This section provides detailed information about the EEPROM. The EEPROM is divided into logical sections as shown below. Each section includes a version number for the data format, and the size of the section. The offsets and sizes are given in bytes, although the EEPROM address is a 16-bit word address.

Table 3-21 EEPROM Sections

Offset Words	Size Words	Section
0	50	Board Data.
50	100	Axis 1 data
150	100	Axis 2 data
250	100	Axis 3 data
350	100	Axis 4 data
450	100	Factory data
550	1	Checksum (all data above)
	552	Total used
	472	Not used
	1024	Total device

The details of the Board Data section are given in Table 3-22. The details of each of the four identical axis data sections is given in Table 3-23.

Notes for Tables 3-22 and 3-23

1. ASCII fields are left-justified, filled with blanks at the right (higher address) end.
2. Optional feature availability is represented by setting of individual bits in the word. First word contains bits 31 (MSB) to 16 (LSB), second word contains bits 15 (MSB) to 0 (LSB).

Bit	Option
0	APD
1	CEC
2-31	Reserved

3. Delay and data age values are in Data Age units (32.55 ps).
4. Measured voltage value, in ADC units.
5. Voltage output value, in DAC units.
6. APD Gain L2 is in the same units as APD Gain L2 register.
7. Optical Power L2 is in the same units as Opt Power L2 register.
8. APD Temperature values are degrees C * 256.
9. Version 3 applies to early revisions of product that had incorrect gain and voltage data for Nominal and Maximum signal. Version 4 has correct data. Both versions have the same data structure.

Table 3-22 EEPROM Board Data

Note: all voltages are value from Diag ADC register.

Offset Words	Size Words	Note	Description
0	1		Board Data format version
1	1		Size of Board Data block = 50
2	1		Day of manufacture (1-31)
3	1		Month of manufacture (1-12)
4	1		Year of manufacture (2005-…)
5	2		Board Assy Number (8020; 0700)
7	1		Board Configuration (01 or 02)
8	1	1	Board Revision (original) (ASCII)
9	1	1	Board Revision (reworked) (ASCII)
10	5	1	Board Serial number (ASCII)
15	1		Number of axes
16	2	2	Optional features
18	1		Vendor code
19	1	3	Ref Out Delay 1
20	1	3	Ref Out Delay 2
21	1		PCB test temp (deg C) (axis 1)
22	1	4	Ref DC (dark)
23	1	4	Ref SSI (dark)
24	2		Reserved
26	1	4	VCXO_CTRL (with ref)
27	1	4	+HV analog PS
28	1	4	+HV analog PS test
29	1	4	+15V analog PS
30	1	4	+10V analog PS
31	1	4	+5V analog PS
32	1	4	+3.3V analog PS
33	1		Reserved
34	1	4	+1.25 DAC Ref
35	1	4	-5V analog PS
36	1	4	-12V analog PS
37	1	4	-15V analog PS
38	1	4	+5V VME PS
39	1	4	+3.3V digital PS
40	1	4	+2.5V digital PS
41	1	4	+1.8V digital PS
42	1		Reserved
43	1	4	+1.2V digital PS
44	6		Reserved
50	50		Total

Table 3-23 EEPROM Axis Data

Offset Words	Size words	Note	Description
			Axis data
0	1	9	Axis Data format version = 3 or 4
1	1		Size of Axis Data block = 100
2	1	4	Meas DC Dark (50V bias)
3	1	8	APD temp for Meas DC Dark
4	1		Reserved
			– Signal Strength, Minimum Signal
5	1	7	Optical Power L2 of minimum signal
6	1	6	APD gain L2 with minimum signal
7	1	8	APD temp with minimum signal
8	1	5	APD bias with minimum signal
9	1		SSI reading with minimum signal
10	1		Sig RMS L2 reading with minimum signal
11	1		Reserved
			– Signal Strength, Nominal Signal
12	1	7	Optical Power L2 of nominal signal
13	1	6	APD gain L2 with nominal signal
14	1	8	APD temp with nominal signal
15	1	5	APD bias with nominal signal
16	1		SSI reading with nominal signal
17	1		Sig RMS L2 reading with nominal signal
18	1		Reserved
			– Signal Strength, Maximum Signal
19	1	7	Optical Power L2 of maximum signal
20	1	6	APD gain L2 with maximum signal
21	1	8	APD temp with maximum signal
22	1	5	APD bias with maximum signal
23	1		SSI reading with maximum signal
24	1		Sig RMS L2 reading with maximum signal
25	1		Reserved
			Axis data - Data Age
26	1	3	Meas Data Age factory cal
27	1		Size of Dynamic Data Age RAM (or zero)
28	64		Dynamic Data Age RAM
92	8		Reserved
100	100		Total

The EEPROM fiber power values are measured at the input to the board. Typically Fiber Power = 0.382 * FOP power.

3.10 Reference Tree Function

The optical reference input from the laser head is an ST fiber optic connector. The electrical reference input and two output from the measurement board are HSSDC2 type connectors.

The electrical reference connector tree cable includes two pairs of wires. The first pair is used for the reference signal. The second pair is used to send identification data between boards so that the correct connection of the reference tree can be verified by the system software.

The identification (ID) data is shown in following table. The ID data is sent through the reference output and received by the reference input, where it appears in the Reference ID diagnostic register for axis 3. To avoid disturbing the reference signal, the identification data is sent only once when requested by the *Send Reference ID* bit in the Test Command 1 Register for axis 3.

The *RID Invalid* bit in the Reference ID register indicates if the data was received incorrectly. The *RID Invalid* bit is set by the *Clear Ref ID* bit in the Test Command 1 register so it also indicates if no data was received. This bit is used for diagnostic purposes only, and does not affect any other board functions or error indications.

To use the reference ID function:

1) Write a '1' to the *Clear Ref ID* bit of the Test Command 1 register on axis 3 of every board in the system.
2) Write a '1' to the *Send Ref ID* bit of the Test Command 1 register on axis 3 of every board in the system.
3) Wait 100 us for all reference ID transmissions to be complete.
4) Read the Reference ID register on axis 3 of every board in the system, and verify that all are correct.

Table 3-24 Reference Identification

Reference In Reference ID Register	Reference Out 1	Reference Out 2
Axis 3 *RID(9:0)*	VME Base Address(23:14)	VME Base Address(23:14)
Axis 3 *RID(10)*	Axis 3 User P2d Out bit	Axis 3 User P2d Out bit
Axis 3 *RID(11)*	0	1

3.11 Data Age

3.11.1 Definition/Explanation of Data Age

To accurately control the precision motion it is necessary to provide not only position data but also time data; when the measured object is at that exact location. *Data age* is defined as the difference in the time between when the user object is measured and when the user control system gets the position information. *Data age uncertainty* is defined as the maximum variation in the data age in a multi-axis system, due primarily to process variations in the electronics and differences in optical and electrical path lengths.

On a single axis measurement, the data age is approximately 1 μs for the ZMI 4100. The data age must be known so that servo loops using the ZMI 4100 as a sensor can be properly compensated. The exact value of data age for a single axis measurement is usually not important, as long as it is constant.

On a multiple axis dynamic measurements, data age uncertainty must be minimized. The system is intended to measure the position of an object moving as fast as 5.1 m/s with a resolution of 0.3 nm. At this velocity, a time delay in the measurement signal path of 0.1 ns corresponds to a position error of 0.5 nm, which is greater than the system resolution. In a multi-axis system, the data age uncertainty is specified with respect to the first axis in the reference tree.

Multiple boards are synchronized in two ways. The phase meters are synchronized by the 20 MHz reference passed through the reference tree. The measurement output is synchronized by the SCLK0 signal on the P2 bus.

Data age compensation is achieved through internal Measurement Board circuitry that adjusts the data age for a position value.

(*Future*) The ZMI 4104 also provides velocity dependent data age compensation. This compensates for group delay variations in the analog portion of the on-board circuitry. Nominal values are preloaded into on-board RAM that can reduce the velocity dependent error from approximately ±0.3 ns to ±0.1 ns.

3.11.2 Data Age Compensation

Some high precision, high speed applications require the user to minimize data age uncertainty. To determine if data age compensation should be enabled, the user should calculate if data age uncertainty exceeds the error budget. This error is calculated by V * T = error. Typical uncompensated data age uncertainty for a maximum of 15 boards is approximately 30 nanoseconds.

The data age of the ZMI 4000 CEC and 4100 C is approximately 1 μs longer than the data age of the standard ZMI 4000 and 4100. This requires the extended data age range capability in the ZMI 4000 firmware for compatibility. The ZMI 4100 and ZMI 4100 C have the extended data age range. See Appendix D, line 16, for applicable version and revision information.

When applying the equation for setting the data age (as shown in the ZMI 4104 manual), the "Meas Data Age factory cal" value read from EEPROM must be interpreted as a 16-bit signed value (-32768 to 32767). The value written to the Data Age register must be calculated as a 16-bit unsigned value. The standard data age register range is 0 to 8191, the extended data age register range is 0 to 40959.

3.11.3 Compensation Algorithm

The ZMI 4100 data age uncertainty can be reduced by the data age compensation feature. The user reads factory stored data from the onboard EEPROM, then computes a compensation value using the algorithm below. The user then writes this value to the Data Age Adjust register.

The data age adjust value has a range of 1333 ns and a resolution of 32.552 ps. The power-on default value is 0 ns.

Data age uncertainty compensation value algorithm

1. Read the measurement channel delays, $M_{Board, Axis}$, for each axis of each board from the EEPROM on each board. This value is in Data Age Units (0.032552 ns). These are 16-bit signed values with a possible range of -32768 to 32767.
2. Read the reference tree delays, $R_{Board, Output}$, for each reference output of each board from the EEPROM on each board. This value is in Data Age Units (0.032552 ns).
3. Obtain the reference cable delays, C_{Board}, in nanoseconds, for each reference cable. Preferably number the cables to match the board numbers as shown in the figure. These delays are written on a label on each cable. If calibrated cables are not used, use a reference cable delay of 1.25 ns, this will result in an uncertainty of ±150 ps per cable.
4. Optionally, obtain the fiber optic cable delays $F_{Board, Axis}$, in nanoseconds, for each fiber optic cable connected to the measurement input of each board.
   This delay may also include the length of the air path in the interferometer divided by the velocity of light (0.3 m/ns). For a single pass interferometer, the air path is the distance from the end of the fiber optic to the moving reflector in the interferometer. For a double pass interferometer, the air path is the distance from the end of the fiber optic to the beamsplitter in the interferometer, plus twice the distance from the beamsplitter to the moving reflector.

   The approximate fiber optic cable delay may be calculated as: $F = L * n / c$

   Where F = fiber optic delay in ns; L = length of fiber in meters; n = index of refraction of fiber (which is 1.46); and c = velocity of light in vacuum (which is 0.3 m/ns). This equation has some uncertainty due to the length tolerance of the fiber optic cable and the fiber inside the jacket may be slightly longer than the cable.
5. Compute the total delay D Board, Axis for each axis of each board. This value is in Data Age Units (0.032552 ns). The following example is for four boards with their references connected, as shown in Figure 3-6.

   $K_{DA} = 0.032552$

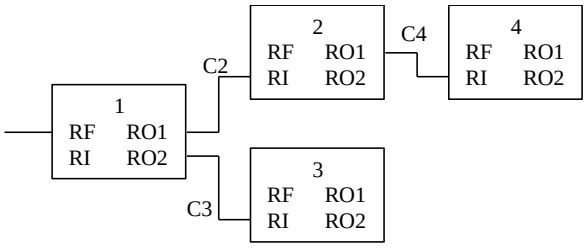
For Axis = 1 to 4

$$D_{1,Axis} = -M_{1,Axis} + F_{1,Axis} / K_{DA}$$
$$D_{2,Axis} = -M_{2,Axis} + F_{2,Axis} / K_{DA} - R_{1,1} - C_2 / K_{DA}$$
$$D_{3,Axis} = -M_{3,Axis} + F_{3,Axis} / K_{DA} - R_{1,2} - C_3 / K_{DA}$$
$$D_{4,Axis} = -M_{4,Axis} + F_{4,Axis} / K_{DA} - R_{1,1} - C_2 / K_{DA} - R_{2,1} - C_4 / K_{DA}$$

End

6. Determine the maximum total delay from all computed $D_{Board, Axis}$ values.
7. Subtract the delay of each axis $D_{Board, Axis}$ from the maximum and round the result to an unsigned integer and verify that the value is within the allowable range. The standard data age range is 0 to 8181, the extended data age range is 0 to 40959. See the table in Appendix D line 16 for applicable version and revision information.

   $DA_{Board, Axis} = Round(Max(D) - D_{Board, Axis})$
8. Load the data age values into the corresponding Data Age Adjust registers.



3.11.4 In-System Data Age Compensation

It is possible to determine the correct data age adjustment in an assembled system by reading the value of the Absolute Phase Register. This reduces the accumulation of uncertainties that occurs when using the factory calibrated delays of the numerous parts of the system.

This requires a program that will read the Absolute Phase value a number of times (typically 100) and compute an average phase. The absolute phase register samples the phase value when the position value is updated, see the register descriptions for more information. Note that special methods must be used for this average, since the data represents an angle (for example, the average of 6 and 8190 is 2, not 4098).

To calculate the Data Age values based on in-system measurements, perform the following steps:

1. Setup the system with a null interferometer. This consists of a variable neutral density (ND) filter and a Fiber Optic Pickup (FOP).
2. Initialize all axes. Set all data age registers to zero (the default value).
3. Connect the fiber optic cable for the axis to be measured to the null interferometer. This test may be arranged to include or exclude the fiber optic cables from the measurement board to the interferometer. Adjust the light level to obtain an SSI Average value between 15000 and 30000. A lower value may be used, but will be less accurate due to noise.
4. Reset the axis and measure the phase P using the test program and the Absolute Phase Register.
5. Calculate the Measurement Data Age for the axis.

   $M_{Board, Axis} = P * (0.048828 / 0.032552)$
6. Repeat steps 3, 4, and 5 for each axis.
7. Compute the total delay $D_{Board, Axis}$ for each axis of each board. This value is in Data Age Units (0.032552 ns). If fiber optic cable delays, $F_{Board, Axis}$, were not included in the calibration, they may be added here (See previous section). The following example is for four boards with their references connected as shown in Figure 3-4.

   $K_{DA} = 0.032552$

   For Axis = 1 to 4

   $D_{1,Axis} = -M_{1,Axis} + F_{1,Axis} / K_{DA}$

   $D_{2,Axis} = -M_{2,Axis} + F_{2,Axis} / K_{DA}$

   $D_{3,Axis} = -M_{3,Axis} + F_{3,Axis} / K_{DA}$

   $D_{4,Axis} = -M_{4,Axis} + F_{4,Axis} / K_{DA}$

   End
8. Determine the maximum total delay from all computed $D_{Board, Axis}$ values.

9. Subtract the delay of each axis $D_{Board, Axis}$ from the maximum and round the result to an integer.

   $DA_{Board, Axis} = Int (Max(D) - D_{Board, Axis} + 0.5)$

10. If the difference between the in-system calculated value and the factory calibrated value is greater than ±768 (±25 ns), add or subtract a multiple of 1536 (50 ns) to the delay values $D_{Board, Axis}$ as required, and repeat steps 8 and 9. This is due to the 2π ambiguity of phase measurements.

11. Load the data age values into the corresponding Data Age Adjust registers.

3.12 Digital Filtering

3.12.1 Purpose of the Digital Filter

A digital filter circuit on the Measurement Board is designed to remove noise from the measurement data. The Measurement Board uses a second order digital filter, with two programmable gains, Kp and Kv, to permit a wide range of low pass filter cutoff frequencies, from 15 kHz to 2.7 MHz.

3.12.2 Selecting Kv and Kp Values

The user should determine the desired measurement bandwidth for their particular application. The proper Kp and Kv values should be selected according to the performance attributes shown in the filter performance tables (settling time, overshoot, following error, bandwidth, and gain peaking) and graphs (magnitude, phase, and group delay vs. frequency).

For a closed loop control system, the filter bandwidth may be set to approximately 10 times the control loop bandwidth. For a given bandwidth there may be several reasonable choices that differ primarily in gain peaking and group delay response.

For open loop measurements, the filter bandwidth may be set to slightly higher than the required measurement bandwidth. For a given bandwidth there may be several reasonable choices that differ primarily in overshoot and settling time.

3.12.3 Filter Performance Tables

The following tables provide digital filter performance information for all Kp and Kv gain combinations. The first *row*, labeled Kp, contains actual Kp gain values. The user programs the Kp register with a number from the cells under the Kp values. The first *column*, labeled Kv, contains the actual Kv gain values. The user programs the Kv Register with a number from the cells to the right of the Kv values.

Blank areas are not recommended and will result in improper operation of digital filter. Shaded areas are not recommended, and will produce poor settling time, overshoot, or gain peaking.

Velocity in µm/s is: (1-pass) 0.002946705 * (value in velocity register)
(2-pass) 0.001473352 * (value in velocity register)

Table 3-25 Time Response at 1g Ramp Acceleration

Settling Time to 1 LSB with 1g Ramp Acceleration (µsec)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.0	0.0						
-9	1	0.0	0.0	0.0					
-11	2	0.0	0.0	0.0	0.0				
-13	3			0.0	0.0	0.0			
-15	4				0.0	0.0	0.0		
-17	5					51.3	26.0	15.9	
-19	6						241.1	112.7	48.7
-21	7							756.4	348.4

Overshoot with 1g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.1	0.1						
-9	1	0.1	0.1	0.1					
-11	2	0.2	0.1	0.1	0.1				
-13	3			0.1	0.1	0.1			
-15	4				0.1	0.1	0.1		
-17	5					0.1	0.1	0.2	
-19	6						0.1	0.1	0.5
-21	7							0.1	0.1

Following Error with 1g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	-0.1	-0.1						
-9	1	-0.1	0.0	0.0					
-11	2	0.0	0.0	0.0	0.0				
-13	3			0.1	0.1	0.1			
-15	4				0.6	0.6	0.6		
-17	5					2.5	2.5	2.5	
-19	6						10.3	10.3	10.3
-21	7							41.5	41.5

Table 3-26 Time Response at 10g Ramp Acceleration

Settling Time to 1 LSB with 10g Ramp Acceleration (µsec)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.0	0.0						
-9	1	0.0	0.0	0.0					
-11	2	0.0	0.0	0.0	0.0				
-13	3			7.1	3.7	2.6			
-15	4				48.2	22.9	10.7		
-17	5					165.7	76.1	45.8	
-19	6						469.5	213.9	119.3
-21	7							1213.5	548.6

Overshoot with 10g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.1	0.1						
-9	1	0.1	0.1	0.1					
-11	2	0.1	0.1	0.1	0.1				
-13	3			0.1	0.1	0.1			
-15	4				0.1	0.1	0.3		
-17	5					0.1	0.1	1.2	
-19	6						0.1	0.1	4.6
-21	7							0.1	0.1

Following Error with 10g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.0	0.0						
-9	1	0.0	0.0	0.0					
-11	2	0.3	0.3	0.3	0.3				
-13	3			1.6	1.6	1.6			
-15	4				6.4	6.4	6.4		
-17	5					25.9	25.9	25.9	
-19	6						103.9	103.9	103.9
-21	7							415.9	415.9

Table 3-27 Time Response at 100g Ramp Acceleration

Settling Time to 1 LSB with 100g Ramp Acceleration (µsec)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.0	0.0						
-9	1	0.0	0.0	0.0					
-11	2	19.5	9.1	4.4	2.2				
-13	3			35.5	16.4	6.3			
-15	4				104.6	47.9	28.0		
-17	5					279.4	126.4	64.4	
-19	6						697.1	314.2	186.6
-21	7							1668.8	750.1

Overshoot with 100g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.2	0.1						
-9	1	0.2	0.1	0.1					
-11	2	0.2	0.1	0.1	0.3				
-13	3			0.1	0.1	0.8			
-15	4				0.1	0.1	2.9		
-17	5					0.1	0.1	11.4	
-19	6						0.1	0.1	45.1
-21	7							0.1	0.1

Following Error with 100g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.2	0.2						
-9	1	1.0	1.0	1.0					
-11	2	4.0	4.0	4.0	4.0				
-13	3			16.2	16.2	16.2			
-15	4				64.9	64.9	64.9		
-17	5					259.9	259.9	259.9	
-19	6						1039.9	1039.9	1039.9
-21	7							4159.4	4159.9

Table 3-28 Time Response at 1000g Ramp Acceleration

Settling Time to 1 LSB with 1000g Ramp Acceleration (µsec)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.6	0.3						
-9	1	7.4	3.3	1.3					
-11	2	48.4	23.3	10.4	6.2				
-13	3			64.2	28.9	15.2			
-15	4				162.4	73.1	43.3		
-17	5					394.0	176.9	100.2	
-19	6						925.8	414.9	213.2
-21	7							2117.2	951.2

Overshoot with 1000g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	0.2	0.2						
-9	1	0.2	0.1	0.5					
-11	2	0.2	0.1	0.1	1.9				
-13	3			0.1	0.1	7.3			
-15	4				0.1	0.1	28.5		
-17	5					0.1	0.1	113.1	
-19	6						0.1	0.1	450.9
-21	7							0.1	0.1

Following Error with 1000g Ramp Acceleration (LSB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	2.5	2.5						
-9	1	10.1	10.1	10.1					
-11	2	40.6	40.6	40.6	40.6				
-13	3			162.4	162.4	162.4			
-15	4				649.9	649.9	649.9		
-17	5					2599.9	2599.9	2599.9	
-19	6						10398.5	10400.0	10400.0
-21	7							41131.7	41597.9

Table 3-29 Digital Filter Frequency Response

-3dB Bandwidth of Digital Filter (kHz)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	2920.0	1585.4						
-9	1	2886.0	1397.3	697.0					
-11	2	2902.9	1332.5	562.5	317.9				
-13	3			514.1	246.5	152.1			
-15	4				226.4	118.2	75.0		
-17	5					108.9	58.1	38.1	
-19	6						51.9	28.9	18.2
-21	7							27.4	15.2

Gain Peaking of Digital Filter (dB)

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	3.9	3.9						
-9	1	3.0	1.0	2.7					
-11	2	2.8	0.3	0.8	2.4				
-13	3			0.2	0.8	2.2			
-15	4				0.2	0.7	2.1		
-17	5					0.2	0.7	2.1	
-19	6						0.2	0.7	2.0
-21	7							0.2	0.7

These plots of digital filter response do not include the effect of the DFT frequency response. The total magnitude response is the dB sum of the DFT response listed below, and the filter response.

Frequency MHZ	Amplitude dB
0.0	0
0.8	-1
1.1	-2
1.4	-3
2.4	-10
3.3	-20
4.3	-40
4.8	-60
5.0	-80

Table 3-30 Velocity Accuracy and Resolution

Velocity RMS Error in µm/sec

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	75	24						
-9	1	165	52	21					
-11	2	336	116	36	4.7				
-13	3			85	24	8.1			
-15	4				68	18	3.4		
-17	5					44	15	3.1	
-19	6						21	9.3	9.5
-21	7							10	4.4

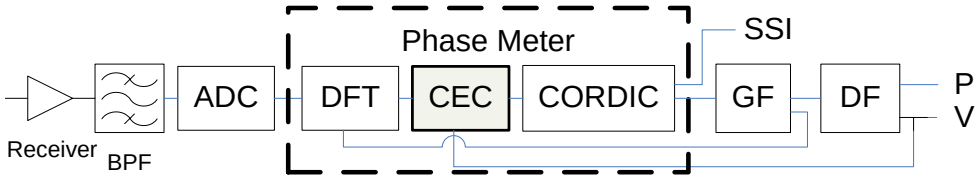
Velocity Resolution, Bits

	Kp	-2	-3	-4	-5	-6	-7	-8	-9
Kv		0	1	2	3	4	5	6	7
-7	0	17	19						
-9	1	16	18	19					
-11	2	15	17	18	21				
-13	3			17	19	21			
-15	4				18	19	22		
-17	5					18	20	22	
-19	6						19	20	20
-21	7							20	22

3.13 Signal Processing

A block diagram of the signal processing of the ZMI 4104 CEC measurement board is shown in the following figure.

Figure 3-10 ZMI 4104 Signal Processing with CEC

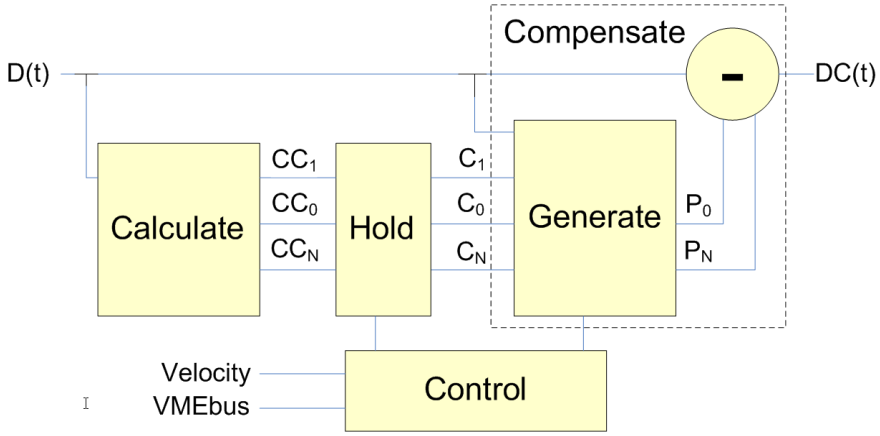


The ZMI 4104 processing consists of the following components:

- **Receiver** (Fiber Optic Receiver). This receives the optical signal from a fiber optic cable and converts it to an electrical signal.
- **BPF** (Bandpass Filter). This filters out frequencies outside of the frequency range of interest. This also eliminates aliasing of noise at frequencies above the Nyquist frequency.
- **ADC** (Analog to Digital Converter). This converts the analog signal to a digital representation of the signal. The ADC operates at a 120 MHz sample rate.
- **DFT** (Discrete Fourier Transform). This calculates a Fourier Transform of the signal at one specific frequency. Feedback from the Glitch Filter determines the frequency corresponding to the current velocity of motion. The output of the DFT is a complex value (i.e. a value with a real and an imaginary part) which represents the signal at the selected frequency. The DFT operates at a 10 MHz rate.
- **CEC** (Cyclic Error Compensation). This calculates coefficients representing cyclic errors of the measurement signal, generates compensating signals similar to the cyclic errors, and subtracts the compensating signals from the complex DFT value. This block is not in the standard ZMI 4104.
- **CORDIC** (Coordinate Rotation by Digital Computer). This converts the complex output from the CEC to separate magnitude and phase values. The magnitude output is averaged and used for the Signal Strength Indicator (SSI). The phase output goes to the Glitch Filter (GF).
- **GF** (Glitch Filter). This calculates position and velocity based on phase values from the CORDIC. The Glitch Filter also reduces the occurrence of glitches due to noise at low signal levels.
- **DF** (Digital Filter). This filters the position information from the glitch filter, and provides position and velocity outputs for the user interfaces (VME, P2, Serial).

The following figure shows a simplified block diagram of the Cyclic Error Compensation (CEC) signal processing. The CEC input D(t) is a complex value from the DFT which represents the measurement signal and its cyclic errors.

Figure 3-11 ZMI 4104 CEC Signal Processing



The CEC processing consists of the following components:

- **Calculate** (Calculation). This calculates three coefficients (CC_1, CC_0, and CC_N) that describe the signal and its cyclic errors.
- **Hold** (Holding Registers). This controls the use of the three calculated coefficients (CC_1, CC_0, and CC_N), or substitutes user-provided coefficients (UC_1, UC_0, and UC_N).
- **Generate** (Compensation Signal Generation). This generates signals P_0 and P_N that are approximately equal to the cyclic error portions of the measurement signal.
- **-** (Subtract). This subtracts the compensation signals, and outputs a compensated signal DC(t) to the CORDIC.
- **Control**. This controls the operation of the cyclic error compensation.

3.14 CEC Operation

The following table summarizes the frequencies of four common cyclic errors, and the frequencies of the position disturbances that they cause. The CEC function calculates and subtracts the cyclic errors 0 and N. The calculation is performed while motion occurs, and the coefficients are stored and used to correct for the cyclic errors when motion is at a velocity below a predefined threshold.

Table 3-31 Cyclic Errors

Cyclic Error	Signal Frequency	Frequency Offset	Cyclic Error Frequency
N or -1	$f_R - f_D$	$- f_D$	$2f_D$
0	f_R	0	f_D
1 (Doppler)	$f_R + f_D$	f_D	0
2	$f_R + 2f_D$	$2f_D$	f_D
3	$f_R + 3f_D$	$3f_D$	$2f_D$

f_R = Reference Frequency, f_D = Doppler Frequency

The CEC function has four distinct modes of operation. The transition between modes is automatically controlled by the hardware. Compensation is enabled by setting the *Enab Comp 0* and *Enab Comp N* bits in the CE Control register. The powerup default is with compensation disabled.

- **Startup.** After axis reset, the CEC compensation is disabled until motion occurs and the coefficients are calculated. The entire startup motion must be at a velocity greater than the value specified by the CE Min Vel register and less than the value specified by the CE Max Vel register.
    - The first time after axis reset, coefficients are available, compensation is enabled and *CE Init Complete* bit in the CE Status register is set after 4.1 ms of motion.
    - If the velocity decreases below the CE Min Vel threshold, the coefficients are immediately held.
    - If the velocity again increases above the CE Min Vel threshold, the C0 and C1 coefficient updates begin after 2.1 ms, and the CN coefficient updates begin after 3.7 ms.

  If the *Enab User Startup* bit in the CE Control register is set, the user-defined coefficients are used until the *CE Init Complete* bit in the CE Status register is set.

- **Low velocity**. At low or zero velocity, the cyclic error coefficients are held from the most recent calculated values. The *Hold C1*, *Hold C0*, and *Hold CN* bits in the CE Status register indicate the coefficients are being held. The CE Age register indicates how long the coefficients have been held.

  The CE Min Vel register determines the threshold between low velocity and medium velocity. The default setting for the CE Min Vel register is 96, which represents a 7.3 kHz Doppler shift, or a velocity of approximately 1.2 mm/s (double pass).

  The CE Min Vel register should not be set to a value smaller than 24, which represents a 1.8 kHz Doppler shift, this may cause improper operation of the CEC function.

- **Medium velocity**. At medium velocities, the cyclic error coefficients are calculated and used in real time. The coefficient update period is 409.6 µs.

- **High velocity**. At high velocity, cyclic errors are reduced by cyclic error filtering (CEF) in the DFT and digital filter. Table shows the combined bandwidth of the DFT and the digital filter for typical settings of *Kp* and *Kv* in Control Register 1. CEF is most effective when the cyclic error frequency is greater than the -20 dB bandwidth of the filter.

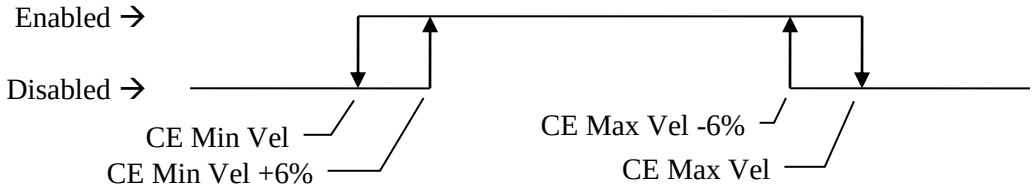
  The CE Max Vel register determines the threshold between medium velocity and high velocity. CEC can operate up to a Cyclic Error frequency of approximately 5 MHz, corresponding to a Doppler frequency of approximately 2.5 MHz. The default setting of the CE Max Vel register is 31457, which represents a 2.4 MHz Doppler shift, or a velocity of approximately 0.38 m/s (double pass).

Table 3-32 Cyclic Error Filtering

Kp (CR1)	Kv (CR1)	-3 dB BW (kHz)	-20 dB BW (kHz)	-20 dB BW (m/s, double pass)
0	1	1400	3300	0.52
1	1	1000	2700	0.43
2	2	563	2000	0.32
3	3	247	1500	0.24
4	4	118	1000	0.16
5	5	58	500	0.08
6	6	29	250	0.04
7	7	15	125	0.02

- **Errors.** A CE error sets a bit in the CE Error Status register. If the corresponding bit in the CEC Error Mask register is set, the occurrence of the error also sets the *CEC Error* bit in the VME Error Status 0 and the P2 Error Status 0 registers. The CE Error Status register is cleared by axis reset (see section 3.8.2), or CE error reset (writing a 1 to the *Reset CEC Errors* bit in the CE Command register). It is not necessary to clear the CE Error Status register before clearing the CEC Error bits in the VME Error Status 0 and the P2 Error Status 0 registers. The CEC Error may be due to any of a number of reasons:
  - **CE Overflow.** A CE Overflow will occur at cyclic error levels greater than 20% of the measurement signal.
  - **CE Limit.** A CE Limit error occurs if the cyclic error exceeds the value in the CE limit register.

The following figure illustrates the operation of the CE Min Vel and CE Max Vel registers. These registers have a 6% hysteresis when determining the boundaries of the CEC compensation. Note that the presence of cyclic errors also causes uncertainty in the calculation of velocity, which may make the apparent hysteresis smaller.



3.14.1 CEC Diagnostics

The CEC Hardware includes several diagnostic features. These are described individually in Chapter 4, their use and common features are described here. Note that most CE values have special numeric formats that are described in Chapter 4. In the following discussion, a ".re" suffix refers to the real part of a complex value, and a ".im" suffix refers to the imaginary part of a complex value.

- **Calculated Coefficient registers.** The CE C1 Calculated, CE C0 Calculated, and CE CN Calculated registers contain calculated coefficients that may be read through the VME interface. The values from these registers may be used to calculate the amount of cyclic error.
  - Measurement Signal = $\sqrt{C1}$
  - Cyclic Error 0 ratio = $\frac{\sqrt{C0.re^2 + C0.im^2}}{\sqrt{C1}}$
  - Cyclic Error N ratio = $\frac{\sqrt{CN.re^2 + CN.im^2}}{C1}$

  The cyclic error ratios can be converted to other units as follows:

  - Cyclic Error (dB) = $20 \cdot \log_{10}$(Cyclic Error Ratio)
  - Cyclic Error (percent of signal) = Cyclic Error Ratio * 100
  - Cyclic Error (nm RMS) = Cyclic Error ratio $\cdot \frac{1}{2\pi} \cdot \frac{\lambda}{2n} \cdot \frac{\sqrt{2}}{2}$

    For n = 2 (double pass interferometer): Cyclic Error (nm RMS) = Cyclic Error ratio * 17.8

- **User Coefficient registers.** The CE C1 User, CE C0 User, and CE CN User registers allow user-defined cyclic error coefficients. Typically these would be loaded by the user with previously obtained values, and used only at startup. The user coefficients are selected for use at startup by the *Enab User Startup* bit in the CE Control register, or enabled at any time by the *Enab User C1*, *Enab User C0*, and *Enab User CN* bits in the CE Control register.

- **Mag, Min, and Max registers.** The CE 0 Mag and CE N Mag registers use an approximation to calculate the cyclic error percentage. Due to the approximation used, these values may differ from values calculated from the coefficient registers by approximately 10%, depending on the phase of the coefficient.

  The CE 0 Min and CE 0 Max registers record the minimum and maximum values of the CE 0 Mag register. The CE N Min and CE N Max registers record the minimum and maximum values of the CE N Mag register. These max/min registers are reset during CE Initialization (after axis reset), or by the *Reset CEC Max/Min* bit in the CE Command register.

  The values from these registers may be used to calculate the current, maximum, and minimum percentage of cyclic error. In the equations below, M0 refers to a value from the CE 0 Mag, CE 0 Min, or CE 0 Max register, and MN refers to a value from the CE N Mag, CE N Min, or CE N Max register.

  - Cyclic Error 0 percentage = $100 \cdot \frac{M0}{\sqrt{C1}}$
  - Cyclic Error N percentage = $100 \cdot MN$

- **Limit registers.** The CE 0 Limit and CE N Limit registers specify the CE values that will result in a corresponding *CE Max Limit 0* or *CE Max Limit N* error indication in the CE Error Status register.
    - CE 0 Limit = $\frac{\sqrt{C1}}{100} \cdot$ Cyclic Error 0 percentage
    - CE N Limit = $\frac{1}{100} \cdot$ Cyclic Error N percentage
- **Diagnostic RAM.** The Diag FFT RAM is enhanced to allow saving several different types of data. The choice of data is determined by setting the *Data Source* bits in the Diag FFT Control register to the desired value before saving data in the Diag FFT RAM.

Chapter 4 Registers

In register descriptions all axes are listed. When an axis is listed in parenthesis after an axis number, it indicates that the axis in parenthesis is also controlled. The number of axes per board is indicated by the *Config* bits in Status Register 1.

4.1 Register Groups

A detailed register address map is provided in Appendix A. The registers are divided into several groups as shown in the following table.

Table 4-1 Register Groups

P2 Offset (hex)	VME Offset (hex)	Group
00-01	00-02	Command and Status registers
-	04-0A	VME interrupt registers
08-0F	10-1E	Control registers
10-13	20-26	P2bus Interrupt registers
14-1B	28-36	16-bit registers
1C-1F	38-3E	Control Registers
20-3F	40-7E	37-bit data registers
-	A0-BE	Diagnostic Registers and EEPROM
-	C0-FE	Diagnostic registers
-	100-1FE	Data Age RAM *
-	100-13E	CEC registers *
	180-1FE	APD registers *
-	200-3FE	DFT Diagnostic RAM
-	800-FFE	ADC Diagnostic RAM

* Access controlled by *Enable Aux Data* bit in Control Register 2.

4.1.1 VME and P2 Registers

Most registers are accessible from either the VMEbus interface or the P2 interface. Both the VMEbus and P2bus interfaces have position, time, velocity, absolute phase, command, error, and interrupt registers that are completely independent. The P2 registers do not include the diagnostic registers, diagnostic RAM, or data age RAM.

In the case of a simultaneous write from both busses to a single register, a *Write Error* is detected and the P2 data will be written. Note that a nearly-simultaneous write from both busses to a single register will cause unexpected results if the data values are different, but will not be detected as an error. It is the programmer's responsibility to take suitable precautions to avoid problems.

For applications that only require 32 bits of position data, the *Sign Extension* bit in Control Register 0 enables sign extension when a write is done to any 37-bit register (Preset Position, Offset, Compare A, Compare B). This is necessary to prevent spurious 32-bit overflows when a negative value is written.

The P2 registers are identical to the VME registers with the following exceptions:

- The command registers are different.
- The VME error and interrupt registers are not accessible via P2.
- The position, time, velocity, and absolute phase registers are separate.
- The diagnostic registers, the Data Age RAM, and the Diagnostic RAM are not accessible via P2.

The address of a P2 register is equal to the address of the corresponding VME register divided by two.

4.1.2 CEC and APD Register Access

The registers for the CEC and APD functions are located in the same address area as the Data Age RAM (0x100-0x1FE). The *Enable Aux Data* bit in Control Register 2 enables access to the CEC registers and disables access to the Data Age RAM. These registers are accessible only through the VMEbus interface.

Several of the CEC registers are named according to the signal that they represent or control.

- CE C1 (Calculated, User) Doppler signal magnitude.
- CE C0 (Calculated, User), CE 0 (Limit, Mag, Min, Max) 20 MHz (Leakage) cyclic error.
- CE CN (Calculated, User), CE N (Limit, Mag, Min, Max) Negative Doppler cyclic error.

During bias calculation, when the *Cmd Busy* bit or *Bias Calc Busy* bit in Status Register 1 is set, write operations to Control Register 5 or to APD control registers (VME offsets 0x180 to 0x1FE) are inhibited, and will produce a *Write Protect Error* in P2 Error Status 2 and VME Error Status 2 registers. See the *Start Bias Calc* bit in the VME Command Register or P2 Command Register for more information.

4.2 Information Common to Several Registers

4.2.1 37-bit Registers

The following registers are 37-bit registers: Compare A, Compare B, Offset, P2 Position, Preset Pos, Quick Reset, VME Position, and VME Sample Position.

The 37-bit data registers are arranged as groups of four 16-bit registers that can be read as two 32-bit registers. Read the MSB 16-bits first for P2 latch or VME Sample. The layout is:

0. MSB, bits 31:16.
1. LSB, bits 15:0.
2. Extension, three fractional bits and five upper bits.
   - On the VME interface, the extension may be read or written as bytes.
   - Some registers have three fractional bits, 1F, 2F, and 3F with values of 1/2, 1/4, and 1/8 LSB respectively. These bits provide increased resolution to reduce quantization uncertainty for some applications, but do not increase the resolution of the measurement. On a 37-bit register write, these bits should be set to zero if they are not used. On a 32-bit sign-extended write, these bits are automatically set to zero.
   - The five upper bits are bits 36 to 32. These bits are used if position ranges greater than 32 bits are required. On a position read, these bits are sign extended in bits 37-39 (to the byte boundary) to simplify the user's software.
3. Error bits.
   - The error bits are a summary of the bits in the corresponding error register. In some cases, this may reduce the amount of data transfer that is required for the application. Refer to Table 4-2.

The VME Sample Position register and the P2 Position (Position read latch mode) register must be read MSB first, since reading the MSB latches the position, time, velocity, and absolute phase values. The other 37-bit registers may be read with 16-bit and/or 32-bit reads in any order.

The 37-bit read/write registers (Compare A, Compare B, Offset, Preset Position) are updated when the LSB is written. These registers may be written with 16-bit and/or 32-bit writes, as long as the 16-bit or 32-bit LSB is written last. A value written to the Extension or the MSB will not appear in the corresponding read register, or affect the measurement, until the LSB is written.

Table 4-2 Error Bits and the Corresponding Error Register

Bit	Meaning	VME Position Errors VME Sample Position Errors	P2 Position Errors
0	Ref Present	Status Register 0, bit 1	Status Register 0, bit 1
1	Ref Error	VME Ref Error, see error list	P2 Ref Error, see error list
2	Meas Present	Status Register 1, bit 1	Status Register 1, bit 1
3	Meas Error	VME Meas Error, see error list	P2 Meas Error, see error list
4	Comparator State	VME Error Status 1, bit 5	P2 Error Status 1, bit 5
5	User P2d in	Status Register 1, bit 15	Status Register 1, bit 15
6	User P2d out	Control Register 16, bit 0	Control Register 16, bit 0

4.2.2 Error Status and Interrupt Enable Registers

The following registers have similar error and status bit definitions. These are described in the next two tables.

VME Interrupt Enable

VME Error Clear

VME Error Status

P2 Interrupt Enable

P2 Error Clear

P2 Error Status

The exceptions to identical bit definitions are:

- The VME registers do not have the *P2 External Sample (SCLK)* bit.
- The P2 registers do not have the *VME 32 Bit Overflow* bit or the *VME External Sample (SCLK)* bit.

The P2 serial error flag, the error output from the P2d_ERRn* and P2d_ERRANY* pins, and the High Speed Position error output (if present) are from either the VME Error Status register or the P2 Error Status register, as selected by the *Error Output Source* bit in Control Register 0. There is no masking of individual errors. This error is the logical OR of all of the Reference ("R") or Measure ("M") errors shown in the following tables for Error Status Registers 0, 1 and 2.

The reference error LED is the logical OR of the reference error signal for all measurement axes.

Error Clear, Error Status, and Interrupt Enable Register 0 Functions

Bit	Type(1)	Description
0	R	*Power Error*. This error occurs if one of the on-board power supplies is not operating properly. For more information, use the diagnostic ADC to measure the supply voltages.
1		*Write Error*. This error occurs when a VME write and a P2 write are performed to the same register at the same time.
2	R	*Reference Signal Missing*. The reference signal is missing.
3	R	*Reference PLL Error*. The PLL that generates the on-board system clock is not operating properly. This will normally occur when the reference signal is missing.
4		*Reset Complete*. This condition occurs when the *Reset Complete* bit in Status Register 1 is set after a position reset, axis reset, or load position operation is complete. This bit goes low immediately following the reset, and returns high after the reset is complete.
5	M F	*Reset Failure*. This error indicates that there was no signal present after an axis reset or position reset.

Error Clear, Error Status, and Interrupt Enable Register 0 Functions (continued)

Bit	Type(1)	Description
6	R	*FPGA Sync Error*. This indicates that the slave FPGA (axis 1 and 2) is not properly synchronized to the master FPGA (axis 3 and 4) or the Delay Locked Loop (DLL) in the FPGA is not operating properly.
7	M	*Overtemp Error*. This error causes the measure error LED to flash. It indicates that the board temperature or FPGA temperature, as measured by the diagnostic temperature monitor, exceeds the preset limits. The default setting produces an error if the FPGA internal temperature exceeds +85°C. After the temperature returns below the limit, the error must be cleared as described in the description of the Diag Temp Monitor Control register.
8	M F	*Measure Signal Missing*. There is no detectable measurement signal. The threshold for this error is defined by the SSI Squelch register.
9	M	*Measure Signal Saturated*. This error indicates the measurement signal is saturating the Analog-to-Digital converter input, resulting in inaccurate phase measurements.
10		*SSI Max Limit*. This error is for test use only. If the value of the SSI Max register exceeds the value set in the User Excess Velocity register, the *SSI Max Limit* error status bit is set. This produces an error indication only if enabled by the *SSI Max Limit* bit in the VME Interrupt Enable register or the P2 Interrupt Enable register. (See Appendix D line 17 for applicability.)
11	M	*Measure Signal Dropout*. A momentary loss of the measurement signal was detected.
12	M F	*Measure Signal Glitch*. A glitch was detected on the measurement signal. A glitch is detected by the phase noise monitor when the instantaneous error in the position calculator exceeds $\pm 0.98\ \pi$.
13	M F	*Acceleration Error*. An acceleration was greater than the circuitry could follow. This error is rare because the digital filter can follow accelerations greater than 1000 g.
14	M	*Phase Noise Error*. Phase noise greater than the limit set by the Phase Noise Limit register was detected.
15	M	*CEC Error. (ZMI 4100C only)* This bit is set at the same time any bit in the CE Error Status register is set.

(1) Type refers to the error type: M= Measurement Error, R= Reference or System Error, F= Fatal Error (requires axis reset).

Error Clear, Error Status, and Interrupt Enable Register 1 Functions

Bit	Type(1)	Description
0	M F	*Velocity Error*. The average velocity was greater than 5.1 m/s (single pass) or 2.55 m/s (double pass). This limit corresponds to input frequencies of 3.9 MHz to 36.1 MHz. This limit may be disabled with the *Disable Excess Velocity* bit in the Test Control 0 register, however system accuracy and signal sensitivity are undefined at velocities outside the normal range.
1	M	*User Velocity Error*. The average velocity was greater than the limit specified by the User Excess Velocity register.
2	M F	*37 bit Position Overflow*. This error is detected when the position value exceeds the range of the 37-bit position register. When a position overflow occurs, the sign of the measured position will change. Note that use of the quick reset register or the preset function may reduce the usable position range.
3	M (VME only)	*VME 32 bit Position Overflow*. (Not available for P2 registers.) This error is detected when the position value exceeds the range of the 32-bit register. When a position overflow occurs, the sign of the measured position will change. This error is enabled by the *VME Enable 32-bit Overflow* bit in Control Register 2.
4	M (P2 only)	*P2 32 bit Position Overflow*. This error is detected when the position value exceeds the range of the 32-bit register. When a position overflow occurs, the sign of the measured position will change. This error is enabled by the *P2 Enable 32-bit Overflow* bit in Control Register 4.
5		*Compare*. This condition is the result of the compare operation. This is described in Chapter 3.
7-6		*Reserved*.
8		*VME External Sample (SCLK)*. (not available for P2 registers) This condition occurs when an SCLK input samples the measurement data. This condition does not occur if the SCLK sample is causing a reset as controlled by the *SCLK Reset Enable* bit in Control Register 3.
9		*P2 External Sample (SCLK)*. (not available for VME registers) This condition occurs when an SCLK input samples the measurement data. This condition does not occur if the SCLK sample is causing a reset as controlled by the *SCLK Reset Enable* bit in Control Register 3.
14-10		*Reserved*.
15		*VME Interrupt Enable* (VME Interrupt Enable register only) This enables the VME interrupt.

(1) Type refers to the error type: M= Measurement Error, R= Reference or System Error, F= Fatal Error (requires axis reset).

4.2.3 Error Register 2 Bits

This table shows the bit assignments for the following registers: P2 Error Clear 2, P2 Interrupt Enable 2, P2 Error Status 2, VME Error Clear 2, VME Interrupt Enable 2, and VME Error Status 2. Additional information for APD related errors is given in the APD Error Code register.

Error Clear, Error Status, and Interrupt Enable Register 2 Functions

Bit	Type(1)	Description
0	M F	*APD Temp Error*. This indicates that the APD temperature exceeds the allowable range.
1	M F	*APD Fail Error*. This indicates that an error exists that prevents the APD from providing a usable signal. For more information see the value in the Error Code register.
2		*APD Command Error*. This indicates that an APD bias calculation command was initiated with command parameters that were invalid or out of range.
3	M F	*APD DC Error*. This indicates that the Meas DC voltage (measured by the Diagnostic ADC) exceeded the allowable range. This may occur if there is a sudden large increase in signal, or if there is a large DC signal with a small AC signal.
4	M	*Bias Error*. This indicates that the APD controller was unable to correctly set the APD gain or bias.
5		*Bias Calc Complete*. This indicates that the controller has completed adjustment of the APD gain.
6		*Sig RMS L2 Min*. This indicates that the Sig RMS L2 value was less than the value in the Sig RMS L2 Min Lim register.
7		*Sig RMS L2 Max*. This indicates that the Sig RMS L2 value was greater than the value in the Sig RMS L2 Max Lim register.
8		*APD Controller Software Error*. This bit is set to indicate a software error detected by the APD Controller. The Error Type is posted to the upper 4 bits of the SW Error ID register. The Error ID is posted to the lower 12 bits of the Software Error ID register. See section 3.8.10 for a description of APD Controller Software errors.
9-11		*Reserved.*
12		*Write protect error*. This indicates that a write operation was attempted to Control Register 5 or to an APD control register (VME offsets 0x180 to 0x1FE) when the APD controller was busy executing a command (indicated by *Bias Calc Busy* or *Cmd Busy* in Status Register 1).
13	R F	*Bias Supply Error*. This indicates that the APD bias supply is off or failed the powerup self-test operation.
14	R F	*Proc Fail*. This indicates that there was a failure of the initialization of the APD controls.
15	R F	*Proc Init Busy*. This indicates that the APD control processor is busy doing initial self-tests and initialization of the APD controls. When the initialization is complete, or if there is an error during initialization, this bit is cleared.

(1) Type refers to the error type: M= Measurement Error, R= Reference or System Error, F= Fatal Error (requires axis reset).

4.2.4 CEC Register Formats

The internal processing for the CEC function uses integer, floating point, complex integer, and complex floating point arithmetic. This section describes the different numeric formats as they appear in the CEC registers, and methods for converting formats. Note that the methods described have no error checking, in an actual application consideration for zero, negative, large, and small values are required.

CEC Register Formats

Register Format	Abbreviation	Bits	Registers
32-bit Unsigned Integer	UInt32	32	CEC Age
Complex Integer	CInt16	32	CE C0 Calculated, CE C0 User
Complex Float	CFloat	32	CE CN Calculated, CE CN User
Float	Float	32	CE C1 Calculated, CE C1 User
Unsigned Short Float	USFloat	16	CE 0, CE N (Limit, Mag, Min, Max)

The 32-bit registers (UInt32, CInt16, CFloat and Float) may be read and written as a 32-bit word, or as two adjacent 16-bit words. When writing as two 16-bit words, the MSB must be written first, then the LSB. When reading as two 16-bit words, the MSB must be read first, then the LSB.

The floating point and complex floating point formats can represent values from 5.9e-39 to 6.8e+38.

In the following descriptions, the notation “C ? A : B” represents a conditional assignment where the value of A is used if condition C is true, otherwise the value of B is used.

32-bit Unsigned Integer (UInt32)

The 32-bit unsigned integer value consists of 32 bits, the value is in the range from 0 to 4 294 967 295.

Complex Integer (CInt16)

The complex integer value has a real part and an imaginary part. Each part is in the range from -32768 to 32767. The real part is in bits 31 (MSB) to 16 (LSB), and the imaginary part is in bits 15 (MSB) to 0 (LSB).

Complex Float (CFloat)

The complex floating point value consists of an exponent, two sign bits, and two mantissas to represent the real part and the imaginary part of a complex number.

Complex Floating Point Value

Part	Abbreviation	Bits	Bit range	Notes
Exponent	Exp	8	31-24	Bias = 127
Real sign	Rsign	1	23	
Real mantissa	Rmant	11	22-12	Includes MSB
Imaginary sign	Isign	1	11	
Imaginary mantissa	Imant	11	10-0	Includes MSB

The larger of the real and imaginary parts can represent a value from ±5.9e-39 to ±6.8e+38. The two parts have the same exponent, so the smaller part has the same resolution as the larger part.

To convert a CFloat to a complex real number, convert each part shown in the table above to an unsigned integer and use the following equations:`

Real = (1 - 2 * Rsign) * Rmant * $2^{(Exp-127-10)}$

Imaginary = (1 - 2 * Isign) * Imant * $2^{(Exp-127-10)}$

To convert the real (R) and imaginary (I) parts of complex real number to a CFloat value (CF), use the following equations:

REx = floor(log2(abs(R)))

IEx = floor(log2(abs(I)))

Ex = max(REx, IEx)

CF = (Ex + 127) * 0x1000000

+ (R < 0 ? 0x800000 : 0) + round(abs(R) * $2^{-(Ex-10)}$) * 0x1000

+ (I < 0 ? 0x800 : 0) + round(abs(I) * $2^{-(Ex-10)}$)

Float (Float)

The floating point number consists of an exponent, a sign bit, and a mantissa.

Floating Point Number

Part	Abbreviation	Bits	Bit range	Notes
-	-	7	31-25	Not used
Sign	Sign	1	24	
Exponent	Exp	8	23-16	Bias = 127
Mantissa	Mant	16	15-0	Implied MSB

To convert a float to a real number (R), convert each part in the table above to an unsigned integer and use the following equation:

R = (1 - 2 * Sign) * (Mant + 0x10000) * $2^{(Exp-127-16)}$

To convert a real number (R) to a float (F), use the following equations:

Ex = floor(log2(abs(R)))

F = (R < 0 ? 0x1000000:0) + (Ex+127)*0x10000 + (round(abs(R) * $2^{(16-Ex)}$) and 0xffff)

Unsigned Short Float (USFloat)

The unsigned short floating point number consists of an exponent and a mantissa.

Unsigned Short Floating Point Number

Part	Abbreviation	Bits	Bit range	Notes
Exponent	Exp	8	15-8	Bias = 127
Mantissa	Mant	8	7-0	Implied MSB

To convert a USFloat to a real number, convert each part in the table above to an unsigned integer and use the following equation:

Real = (Mant + 0x100) * $2^{(Exp-127-8)}$

To convert a real number R to an unsigned short float U, use the following equations:

Ex = floor(log2(R))

U = (Ex+127)*0x100 + (round{R * $2^{(8-Ex)}$} and 0x00ff)

4.3 Register Descriptions

The registers are described here, listed in alphabetical order. For each register, the VME and P2 offset address are given, if applicable. If the register is read-only or write-only, that is also noted.

VME registers may be accessed separately as 16 bits, or in pairs as 32 bits. P2 registers may be accessed only in pairs as 32 bits, although many registers are only 16 bits. Table 4-3 shows the bit assignments and address offsets for VME and P2 registers.

Table 4-3 Bit Assignment and Address Offsets

	MSB 31:24	23:16	15:8	LSB 7:0
8-bit VME	0	1	2	3
16-bit VME	0		2	
32-bit VME	0			
16-bit P2	0		1	
32-bit P2	0			

All control and configuration registers have a powerup default value of zero, except for the following registers, in which case the default value is listed below. These are described fully in the register descriptions.

Control Register 16 = 0x0c00
Control Register 17 = 0x0c00 (SW5-1 on) or 0x0c20 (SW5-1 off)
Diag Temp Monitor Control = 0x2a0d
Diag Temp Monitor Write = 0x0055
Phase Noise Limit = 0x07ff (2047)
SSI Squelch = 0x0080 (128)
Test Control 0 = 0x0800
User Excess Velocity = 0xffff (65535)
CE Max Vel Register = 0x7ae1 (31457)
CE Min Vel Register = 0x0060 (96)

APD Bias DAC

Axis	VME (read/write)	P2
1	0x00DE	-
2	0x10DE	-
3	0x20DE	-
4	0x30DE	-

In Constant Voltage Mode, this register sets the APD bias voltage directly. In other modes, this register is read-only and contains the APD bias voltage that is set by the controller. The APD Bias voltage is calculated as follows:

APD_Bias_Voltage = APD_Bias_DAC * 61.65 mV

APD_Bias_DAC = APD_Bias_Voltage / 61.65 mV

APD Bias DAC Register Functions

Bit	*Description*
15-12	*Reserved*
11-0	*APD Bias*

APD Error Code

Axis	VME (read)	P2
1	0x018A	-
2	0x118A	-
3	0x218A	-
4	0x318A	-

This register contains a value posted by the microcontroller when an error occurs. When more than one error occurs, the first error code is retained. This register is reset by a reset axis command.

APD Error Code Register Functions

Bit	*Description*
15-8	System error codes. These errors indicate board-level problems that may affect all axes.
7-0	Axis error codes. These errors indicate axis errors that affect only the axis with the error.

System Error Codes

Errors indicated as FB prevent operation of all axes. FB (Fatal Board) errors are reset by powerup, by VME SYSRESET, or by APD microcontroller reset (Test Command 1 register *Reset Controller* bit).

Code	*Name*	*Type*	*Description*
0	No error	-	
1	HV Init Error	FB	HV failed limit test during board initialization
2	LV Init Error	FB	LV reading failed limit test during board initialization
3	FOR Init Error	FB	Fiber Optic Receiver not detected during board initialization (no APD temp)
4	LV OK Timeout Error	FB	Slave did not detect LV_OK within allotted time
5	Slave Act FOR Timeout Error	FB	Master did not receive Slave response that FOR detected
6	HV OK Timeout Error	FB	Slave did not detect HV_OK within allotted time
7	EE Cal Read Error	FB	Master unable to read EE calibration data
8	EE Cal Xfer Error	FB	EE Cal transfer to Slave failed or timeout
9	CEC Ver Timeout Error	FB	Slave failed to tell Master that CEC enabled
10	Ovr Ver Timeout Error	FB	Master unable to verify that Override enabled on Slave
11	Illegal Opcode Error	FB	Hardware exception due to an attempt to execute an illegal opcode
12	Divide By Zero Error	-	Hardware exception due to divide by zero
128	HV Operation Error	FB	HV Failed limits after board initialization
129	LV Operation Error	FB	LV reading failed limit test after board initialization
130	EEprom Checksum Error	NF	EEprom Checksum Error during Board Initialization
131	Slave Timeout Op Error	FB	The Slave did not respond to the Master within the specified time
132	Slave Req. Not Conf. Op Error	FB	Master unable to confirm the request for Slave status
133	Master Rcvd Slave Fatal Error	FB	Master received fatal error status from Slave

Axis Error Codes

Errors indicated as FB prevent operation of all axes. FB (Fatal Board) errors are reset by powerup, by VME SYSRESET, or by APD microcontroller reset (Test Command 1 register *Reset Controller* bit).

Code	*Name*	*Type*	*Description*
0	No Error	-	
1	APD Temp Init Error	FB	FOR failed APD Temp limit check (5 to 70 °C) during axis initialization
2	Bias Range Init Error	FB	Bias failed range check during axis initialization (deviation > 10 V after 0.5 sec)
3	DC Meas Low Init Error	-	Meas DC failed low limit check (-4.5 V) during axis initialization
7	Bias Limit Init Error	FB	Bias failed limit check (175 V) during axis initialization
8	DC Meas High Init Error	FB	Meas DC failed high limit check (-1.4 V) during axis initialization
9	Bias Limit Op Error	FB	Bias failed limit check (175 V) after axis initialization
128	APD Gain Set Error	-	APD Gain Setting out of range (2048 to 5120, equivalent to gain 4 to 32)
129	Sig RMS Set Error	-	Sig RMS Setting out of range (Sig RMS Max/Min Limit registers)
130	Opt Power Set Error	-	Optical Power Setting out of range (-3930 to 3402, equivalent to 0.07 to 10 μW)
133	Sig RMS Cal Max Error	-	Sig RMS greater than Sig RMS Max Limit register value
134	Sig RMS Cal Min Error	-	Sig RMS less than Sig RMS Min Limit register value
135	APD Math Gain	-	Invalid APD Gain (2048 to 5120, equivalent to gain 4 to 32)
136	APD Math Poly	-	Invalid APD bias equation coefficients (zero)
137	APD Math Temp	-	Invalid APD temperature (10 to 70 °C)
138	APD Math T0	-	Invalid APD bias equation T0 (15 to 50 °C)
139	APD Math TC	-	Invalid APD bias equation TC (0.3 to 0.9 V/°C)
140	APD Temp Op Error	-	FOR failed APD Temp limit check (5 to 70 °C) after axis initialization
141	Bias Range Op Error	-	APD Bias failed range check after axis initialization (deviation > 10 V after 0.5 sec)
142	DC Meas Low Op Error	-	Meas DC failed low limit check (-4.5 V) after axis initialization
143	DC Meas Hi Op Error	-	Meas DC failed high limit check (-1.4 V) after axis initialization

APD Gain L2

Axis	VME (read)	P2
1	0x01A2	-
2	0x11A2	-
3	0x21A2	-
4	0x31A2	-

This register reports the actual APD gain, calculated from the measured APD bias voltage. This register is periodically updated in all APD bias control modes. This value slightly lags the APD gain or APD voltage setting due to delays in voltage setting, voltage sampling and gain calculation. The APD gain values used in all calculations are relative to the responsivity of a standard PIN photodiode at 633 nm. (The actual gain of the APD is approximately 1.7 times this gain.) The register value is calculated as follows:

$$APD\_Gain\_L2 = Log2(APD\_Gain)*1024$$

$$APD\_Gain = 2^{(APD\_Gain\_L2 / 1024)}$$

APD Gain L2 Set

Axis	VME (read/write)	P2
1	0x018C	-
2	0x118C	-
3	0x218C	-
4	0x318C	-

This register specifies the APD gain in Constant Gain mode. In other modes, this register is not used. The APD gain values used in all calculations are relative to the responsivity of a standard PIN photodiode at 633 nm. The register value is calculated as follows:

$$APD\_Gain\_L2\_Set = Log2(APD\_Gain\_Set)*1024$$

$$APD\_Gain\_Set = 2^{(APD\_Gain\_L2\_Set / 1024)}$$

The value in this register only takes effect when processing a *Start Bias Calc* command from the P2 Command Register or the VME Command Register. The default value is approximately 7 (2875 L2) and the accepted range is 4 (2048 L2) to 32 (5120 L2).

APD Opt Pwr L2 Set

Axis	VME (read/write)	P2
1	0x018E	-
2	0x118E	-
3	0x218E	-
4	0x318E	-

This register specifies the maximum optical power that is expected in Constant Optical Power mode. This is used to determine the APD gain. The units of optical power are microwatts into the fiber optic receiver. The register value is calculated as follows:

$$APD\_Opt\_Pwr\_L2\_Set = Log2(APD\_Opt\_Pwr\_Set)*1024$$

$$APD\_Opt\_Pwr\_Set = 2^{(APD\_Opt\_Pwr\_L2\_Set / 1024)}$$

The value in this register only takes effect when processing a *Start Bias Calc* command from the P2 Command Register or the VME Command Register. The default value is 1uW (0 L2) and the accepted range is 70nW (-3930 L2) to 10uW (3402 L2).

APD Sig RMS L2 Set

Axis	VME (read/write)	P2
1	0x0190	-
2	0x1190	-
3	0x2190	-
4	0x3190	-

This register specifies the desired Sig RMS L2 value used in Sig RMS Adjust mode and in Constant Optical Power mode. This is used by the internal processor to determine the APD gain. The register value is calculated as follows:

$$APD\_Sig\_RMS\_L2\_Set = Log2(APD\_Sig\_RMS\_Set)*1024$$

$$APD\_Sig\_RMS\_Set = 2^{(APD\_Sig\_RMS\_L2\_Set / 1024)}$$

The value in this register only takes effect when processing a *Start Bias Calc* command from the P2 Command Register or the VME Command Register. The default value is 13,200 and the accepted range is within the values set in Sig RMS L2 Min Lim and Sig RMS L2 Max Lim.

APD Temp

Axis	VME (read)	P2
1	0x01A0	-
2	0x11A0	-
3	0x21A0	-
4	0x31A0	-

This register reports the APD temperature in degrees C. This is calculated by the APD controller using the Diagnostic ADC. The resolution is approximately 0.05 °C. The register value is calculated as follows:

$$APD\_Temp\_Reg = APD\_Temp*256$$

$$APD\_Temp = APD\_Temp\_Reg/256$$

CE Age Register

Axis	VME (read)	P2
1	0x0114	-
2	0x1114	-
3	0x2114	-
4	0x3114	-

The CE Age register contains a value that is the time from when the CE Coefficients were last updated. This is a 32-bit unsigned register, with time units of 1 ms. The maximum value is 2^{32}-1, equivalent to 1193 hours.

CE Build Register

Axis	VME (read)	P2
1	0x0110	-
2	0x1110	-
3	0x2110	-
4	0x3110	-

The CE Build register contains an encoded value representing the date when the firmware was created. This is for Zygo factory use only.

CE Command Register

Axis	VME (write)	P2
1	0x0100	-
2	0x1100	-
3	0x2100	-
4	0x3100	-

CE Command Register Functions

Bit	*Description*
0	*Reset CEC Errors*. This resets all errors in the CEC Error Status register.
1	*Reset CEC Max/Min*. This resets the values in the CEC Max/Min registers (CE 0 Max, CE 0 Min, CE N Max, and CE N Min).
15-2	*Reserved*.

CE Control Register

Axis	VME (read/write)	P2
1	0x0102	-
2	0x1102	-
3	0x2102	-
4	0x3102	-

CE Control Register Functions

Bit	*Description*
0	*Enab Comp 0*. This enables compensation of Cyclic Error 0.
1	*Enab Comp N*. This enables compensation of Cyclic Error N.
2	*Enab User C1*. This selects use of a user-supplied coefficient for C1.
3	*Enab User C0*. This selects use of a user-supplied coefficient for C0.
4	*Enab User CN*. This selects use of a user-supplied coefficient for CN.
5	*Disab VME Calc Hold*. This disables the hold of calculated coefficients (C0, C1, and CN) for VME read when the velocity is below the value specified in the CE Min Vel register. This affects only the VME read of coefficients, and has no effect on operation.
6	*Enab User Startup*. This selects use of user-supplied coefficients (C0, C1, and CN) after axis reset, until new calculated coefficients are available when motion at velocity greater than the value specified in the CE Min Vel register occurs.
14-7	*Reserved*.
15	*CE Age Test*. This selects the CE Age register time unit to be 25 ns (range = 107 sec) for test purposes.

CE Data Age Register

Axis	VME (read)	P2
1	0x0112	-
2	0x1112	-
3	0x2112	-
4	0x3112	-

The CE Data Age register contains an encoded value representing the additional data age due to the presence of the CEC processing. This is for ZYGO factory use only.

CE Error Mask Register

Axis	VME (read/write)	P2
1	0x0104	-
2	0x1104	-
3	0x2104	-
4	0x3104	-

This register enables the errors in the CE Error Status register to cause a *CE Error*. If an error is indicated by the CE Error Status register, and the corresponding bit in the CE Error Mask register is a one, a *CE Error* occurs in the VME Error Status register and the P2 Error Status register.

CE Error Status Register

Axis	VME (read)	P2
1	0x0108	-
2	0x1108	-
3	0x2108	-
4	0x3108	-

CE Error Status Register Functions

Bit	*Description*
0	*CE 0 Max Limit.* This indicates the cyclic error 0 value has exceeded the value set in the CE 0 Limit register.
1	*CE N Max Limit.* This indicates the cyclic error N value has exceeded the value set in the CE N Limit register.
3-2	*Reserved.*
14-4	*CE Over.* These bits indicate that there was an arithmetic overflow at some point in the CEC signal processing. This may occur if the CE levels are greater than 20%. Contact ZYGO for more information.
15	*Reserved.*

The CE Error Status register is cleared by an axis reset (see section 3.8.2) or CE error reset (writing a 1 to the *Reset CEC Error* bit in the CE Command register.

CE Max Vel Register

Axis	VME (read/write)	P2
1	0x010E	-
2	0x110E	-
3	0x210E	-
4	0x310E	-

This specifies the maximum velocity where CEC will be applied. The units of this register are 76.3 Hz, or 12 µm/sec for a double-pass interferometer. The default value is 0x7ae1 (31457), which corresponds to 2.4 MHz or 380 mm/s.

CE Min Vel Register

Axis	VME (read/write)	P2
1	0x010C	-
2	0x110C	-
3	0x210C	-
4	0x310C	-

This specifies the minimum velocity where CEC will be applied. The units of this register are 76.3 Hz, or 12 µm/sec for a double-pass interferometer. The default value is 0x0060 (96), which corresponds to 7.3 kHz or 1.2 mm/s. Settings lower than this value may adversely affect CE functionality.

CE Status Register

Axis	VME (read)	P2
1	0x0100	-
2	0x1100	-
3	0x2100	-
4	0x3100	-

CE Status Register Functions

Bit	*Description*
0	*Enab Comp 0.* This is set if compensation of Cyclic Error 0 is enabled.
1	*Enab Comp N*. This is set if compensation of Cyclic Error N is enabled.
2	*Hold C1*. This is set if the value of Cyclic Error Coefficient C1 is held.
3	*Hold C0*. This is set if the value of Cyclic Error Coefficient C0 is held.
4	*Hold CN*. This is set if the value of Cyclic Error Coefficient CN is held.
5	*CE Init Complete.* This is set when the initialization of the Cyclic Error coefficients is complete. This occurs after the following steps have occurred: (a) Axis reset (b) Motion at a velocity where Cyclic Error coefficients are calculated (Greater than CE Min Vel and less than CE Max Vel). (c) Delay of 4.1 ms. For more information, see “Startup” in section 3.14
15-6	*Reserved.*

Compare A

Axis	VME MSB (read/write)	VME LSB (read/write)	VME Ext (read/write)	P2 MSB (read/write)	P2 LSB (read/write)	P2 Ext (read/write)
1	0x0070	0x0072	0x0074	0x38	0x39	0x3A
2	0x1070	0x1072	0x1074	0x78	0x79	0x7A
3	0x2070	0x2072	0x2074	0xB8	0xB9	0xBA
4	0x3070	0x3072	0x3074	0xF8	0xF9	0xFA

This is a 37-bit register, which functions as described in the beginning of this chapter. The operation of the comparators is described in Chapter 3.

Compare B

Axis	VME MSB (read/write)	VME LSB (read/write)	VME Ext (read/write)	P2 MSB (read/write)	P2 LSB (read/write)	P2 Ext (read/write)
1	0x0078	0x007A	0x007C	0x3C	0x3D	0x3E
2	0x1078	0x107A	0x107C	0x7C	0x7D	0x7E
3	0x2078	0x207A	0x207C	0xBC	0xBD	0xBE
4	0x3078	0x307A	0x307C	0xFC	0xFD	0xFE

This is a 37-bit register which functions as described in the beginning of this chapter. The operation of the comparators is described in Chapter 3.

Control Register 0

Axis	VME (read/write)	P2 (read/write)
1	0x0010	0x08
2	0x1010	0x48
3	0x2010	0x88
4	0x3010	0xC8

Control Register 0 Functions

Bit	*Description*
0	*Reserved.*
1	*Enable Data Age Velocity Comp*. This enables Dynamic Data Age velocity compensation.
2	*Reserved.*
3	*Reserved*.
4	*Error LED Source*. 0=VME 1=P2. This selects which error register is used to operate the measurement error and reference error LEDs. The reference error LED is the logical OR of the reference error signal for all measurement axes.
5	*Error Output Source*. 0=VME 1=P2. This determines if the P2D error outputs are controlled by the P2 error register or by the VME error register.
6	*Sign Extension*. This enables the sign extension of 32 bit data to match the 37 bit register size when register data is written. If 16 bit data access is used, the lower 16 bits should be written last.
7	*Position Direction*. This bit reverses the polarity of the position and velocity measurement data. The polarity relationships are: bit 7 = 0: Shorter Measurement path ⇔ + Doppler shift ⇔ + Position ⇔ + Velocity bit 7 = 1: Shorter Measurement path ⇔ + Doppler shift ⇔ - Position ⇔ - Velocity
15-8	*Reserved*.

Control Register 1 (Filters)

Axis	VME (read/write)	P2 (read/write)
1	0x0012	0x09
2	0x1012	0x49
3	0x2012	0x89
4	0x3012	0xC9

Control Register 1 Functions

Bit	*Description*
2-0	*Filter K_V*. KV[2:0] The K_V value for the digital filter is set to produce the best dynamic response for a given value of K_P. See the tables in Chapter 3 for more information.
3	*Reserved*.
6-4	*Filter K_P*. KP[2:0] The KP value for the digital filter primarily determines the bandwidth and response time of the digital filter. See the tables in Chapter 3 for more information.
7	*Reserved.*
11-8	*Glitch Filter*. GF[3:0] The glitch filter controls suppression of glitches that would otherwise cause a loss of valid measurements. When these bits are set to 0 0 0 0 there is a filter time constant of 1.5 µs; when set to 0 0 0 1 the time constant is 3.8 µs.
12	*Disable Quick Reset.* This disables the quick reset function. When this bit is set, the lower 13 bits of the Quick Reset register value is always zero, so the absolute phase register is the same as the lower 13 bits (including the 3 fractional bits) of the position register.
15-12	*Reserved.*

Control Register 2

Axis	VME (read/write)	P2 (read/write)
1	0x0014	0x0A
2	0x1014	0x4A
3	0x2014	0x8A
4	0x3014	0xCA

Control Register 2 Functions

Bit	*Description*
0	*Compare Mode*. This determines if the comparator functions as a window comparator (Mode = 1) or a comparator with hysteresis (Mode = 0).
1	*Compare Interrupt Pol*. This determines the polarity of the comparator result that causes a VME or P2 interrupt.
2	*Compare Out Pol*. This determines the polarity of the comparator signal output to the P2D connector.
3	*Compare Out Enab*. This enables the comparator output on the P2D connector.
4	*DAC x16*. This multiplies the SSI DAC output by 16 to provide better observation of low signal levels.
7-5	*VME Bit Window.* VBW[2:0]. These bits determine how the position register appears in the VME Position and VME Sample Position registers. Refer to Table 3-19.
8	*Serial Data Enable.* This enables the serial data output on the P2Z and P2D connectors.
9	*Enable Aux Data.* This enables access to the Aux Data registers in the address space normally used for the Data Age RAM.
10	*Reserved.*
11	*VME Enable 32-bit Overflow*. This enables detection of the VME 32-bit overflow error.
12	*SCLK VME Sample In*. 0=SCLK0 1=SCLK1. This determines which SCLK signal on the P2 bus causes the VME Position, VME Velocity, VME Time, and VME Absolute Phase registers to be updated.
13	*VME Hold Sample Enable*. If this bit is set, the VME Position value is held until it is read through the VME interface. The *VME External Sample Flag* in Status Register 0 is set when the position value is sampled. Additional samples will set the interrupt bit, but will not update the sample. The *VME External Sample Flag* is cleared by reading the LSB of the VME Position register with a 16-bit read, or as part of a 32-bit read. (See Appendix D line 15 for applicability.)
14	*RFV Mode.* When set, this bit selects an optional fast mode for the Reset Finds Velocity (RFV) operation selected by the *Enable Reset Finds Velocity* bit in Control Register 3. For more information, see the reset descriptions in section 3-8.
15	*Reserved.*

Control Register 3 (Init)

Axis	VME (read/write)	P2 (read/write)
1	0x0016	0x0B
2	0x1016	0x4B
3	0x2016	0x8B
4	0x3016	0xCB

Also see Chapter 3 for more information on reset functions.

Control Register 3 Functions

Bit	*Description*
0	*P2d RESET VME Error Reset Enable*. This controls the reset actions caused by the P2D reset signals.
1	*P2d RESET P2 Error Reset Enable*. This controls the reset actions caused by the P2D reset signals.
2	*P2d RESET Position Reset Enable*. This controls the reset actions caused by the P2D reset signals. Position reset resets the measurement function, but does not reset errors.
3	*P2d RESET Time Reset Enable*. This controls the reset actions caused by the P2D reset signals.
4	*P2d RESET Quick Reset Enable*. This controls the reset actions caused by the P2D reset signals.
5	*P2d ResetAll*. 1=p2reset 0=p2dreset This determines the action of the P2D_RESETALL signal, which may be combined with the P2RESET* signal or the individual P2D_RESETn* signals.
7-6	*Reset Mode*. RM[1:0]. This determines the operation of the P2D_RESETn* and P2D_RESETALL* signals.
8	*Preset Enable*. This enables the preset function. When the axis is reset, the position value is initialized to the value in the 37-bit Preset Pos register.
9	*SCLK Reset Enable*. This enables SCLK0 or SCLK1 (as selected by the SCLK Reset Select bit) to perform a quick reset and a time reset on the first occurrence of SCLK after an axis reset.
10	*SCLK Reset Select*. 0=SCLK0 1=SCLK1. This determines which SCLK signal on the P2 bus causes the reset enabled by the SCLK Reset Enable bit.
11	*Enable Reset Finds Velocity*. This enables searching for the measurement signal frequency after an axis reset. This is required if the velocity when the axis is reset may be greater than 0.1 m/sec.
14-12	*Reset Time. RT[2:0]* This determines the time delay between an axis reset or position reset command and the assertion of the Position Reset Complete bit. The delay choices are shown in Table 4-4. If the *Enable Reset Finds Velocity* bit is set, this is the delay after the velocity finding operation is finished.
15	*Reserved*.

Table 4-4 Control Register 3 - Reset Time Bit

RT2	RT1	RT0	Reset Delay (µs)
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Control Register 4 (P2)

Axis	VME (read/write)	P2 (read/write)
1	0x0018	0x0C
2	0x1018	0x4C
3	0x2018	0x8C
4	0x3018	0xCC

Also see Chapter 3 for more information on reset functions.

Control Register 4 Functions

Bit	*Description*
0	*P2 RESET VME Error Reset Enable*. Controls the reset actions caused by the P2_RESET* signal.
1	*P2 RESET P2 Error Reset Enable*. Controls the reset actions caused by the P2_RESET* signal.
2	*P2 RESET Position Reset Enable*. This controls the reset actions caused by the P2_RESET* signal. Position reset resets the measurement function, but does not reset errors.
3	*P2 RESET Time Reset Enable*. This controls the reset actions caused by the P2_RESET* signal.
4	*P2 RESET Quick Reset Enable*. This controls the reset actions caused by the P2_RESET* signal.
7-5	*P2 Bit Window*. PBW[2:0] This selects determine how the position register appears in the P2 Position register and the Serial Interface output data. Refer to Table 3-20.
9-8	*P2 Int Level*. PIL[1:0] This selects the interrupt level for the P2 bus as shown in Table 4-5. Each axis has its own P2 interrupt level selection.
10	*P2 Int Driver*. PID0 This selects the type of interrupt driver for the P2 bus. When the bit is 0 there is no interrupt driver; when the bit is 1, the interrupt drive is open collector active low.
11	*P2 Enable 32-bit Overflow*. This enables detection of the P2 32-bit overflow error.
12	*SCLK P2 Sample In*. 0=SCLK0, 1=SCLK1 This determines which SCLK signal causes the measurement data to be sampled for output through the P2 interface.
13	*P2 Latch Mode*. 1=Pos Read, 0=SCLK. This determines how the data is latched for reading by the P2 interface.
15-14	*Reserved*.

Table 4-5 Control Register 4 – Interrupt Level Bits

Interrupt Level	PIL1	PIL0
INT0	0	0
INT1	0	1
INT2	1	0
INT3	1	1

Control Register 5 (APD)

Axis	VME (read/write)	P2 (read/write)
1	0x001A	0x0D
2	0x101A	0x4D
3	0x201A	0x8D
4	0x301A	0xCD

The value in this register only takes effect when processing a *Start Bias Calc* command from the P2 Command Register or the VME Command Register.

Control Register 5 Functions

Bit	*Description*
2-0	*Bias Control Mode.* BCM[2:0] This selects the mode of operation for the APD Bias control as shown in Table 4-6.
3	*Gain Control Max.* For Constant Gain, Constant Optical Power mode or Sig RMS Adjust mode, after the initial adjustment the APD gain is reduced only if necessary in response to exceeding the Sig RMS L2 Max Lim register value.
4	*Gain Control Min.* For Constant Gain, Constant Optical Power mode or Sig RMS Adjust mode, after the initial adjustment the APD gain is increased only if necessary in response to exceeding the Sig RMS L2 Min Lim register value.
5	*Gain Control AGC.* For Sig RMS Adjust mode, the APD gain will continuously be adjusted in response to changing signal levels. This option is disabled if the *Gain Control Min* or *Gain Control Max* bit is set.
6	*Disable Auto Gain Reduction*. This disables the automatic reduction in gain when Meas DC indicates exceeding maximum allowed signal level. This is for test purposes only.
7	*Reserved.*
8	*SSI DAC Mode.* This selects a DAC output proportional to the logarithm of the optical power.
15-9	*Reserved.*

Table 4-6 Bias Control Modes

Value	2 1 0	Mode	Description
0	0 0 0	Off	APD bias set to minimum value (55 V)
1	0 0 1	Constant Voltage Mode (diagnostic use only)	APD bias is determined by APD Bias DAC register.
2	0 1 0	Constant Gain Mode	APD bias is determined by APD Gain L2 Set register, APD gain calculation, and temperature compensating algorithm.
3	0 1 1	Constant Optical Power Mode	APD gain is set to achieve the Sig RMS L2 value specified by the APD Sig RMS L2 Set register with the optical power specified by the APD Opt Pwr L2 Set register.
4	1 0 0	Sig RMS Adjust Mode	APD gain is adjusted to obtain the Sig RMS L2 value specified by APD Sig RMS L2 Set register.
5-7		Reserved	

In all modes, the APD gain is reduced if the Meas DC voltage (measured by the Diagnostic ADC) is less than -4.25 V. Gain Set Error (GSE) registers are provided to assist in diagnosing errors related to setting APD gain for SigRMS Adjust, Constant Optical Power and Constant Gain Modes.

Control Register 15

Axis	VME (read/write)	P2 (read/write)
1 (2)	0x003A	0x1D
3 (4)	0x203A	0x9D

Serial output should be enabled prior to starting/enabling the SCLK.

Control Register 15 Functions

Bit	*Description*
0	*SCLK Serial Sample In*. 0=SCLK0, 1=SCLK1. This selects which SCLK signal controls the sampling of data for the serial output on the P2Z connector.
1	*Serial Output Enable P2D.* This enables the serial output driver on the P2D connector (axis 3 only).
2	*Serial Output Enable P2Z.* This enables the serial output driver on the P2Z connector (axis 3 only).
3	*Serial Data Size*. 0=32 1=37. This selects the size of the data being sent out the serial data connector.
7-4	*SDV[3:0]*. *SCLK Divider*. (Axis 3 only) This controls the period of a secondary SCLK signal. The period of the SCLK Divider signal is (SD+1) times the period of the SCLK Timer signal. This function is enabled by the *SCLK Divider Enable* bit in Control Register 16.
11-8	*Reserved.*
13-12	*Reserved.*
14	*SCLK0 In Polarity*. This selects the active edge of the P2_SCLK0 input signal. 0 = falling edge (standard), 1 = rising edge. This bit must be set to the same value on all axes to obtain simultaneous sampling.
15	*SCLK1 In Polarity*. This selects the active edge of the P2_SCLK1 input signal. 0 = falling edge (standard), 1 = rising edge. This bit must be set to the same value on all axes to obtain simultaneous sampling.

Control Register 16

Axis	VME (read/write)	P2 (read/write)
1 (2)	0x003C	0x1E
3 (4)	0x203C	0x9E

Control Register 16 Functions

Bit	*Description*
0	*User P2d Out*. On axis 3, this bit controls the state of the P2D_OUT1 signal and may be read back in the User P2d Out bit of the VME Position Errs, VME Sample Position Errs, or P2 Position Errs registers of axis 3 or 4. On axis 1, this bit does not control hardware, and may be read back in the User P2d Out bit of the VME Position Errs, VME Sample Position Errs, or P2 Position Errs registers of axis 1 or 2.
1	*User LED*. This controls the User LED on the front panel. This bit is present on all axes, but only axis 3 controls the LED.
2	*Disable VME SYSRESET* input*. This bit should normally be set to zero. Normally the VMEbus SYRESET* signal resets all data and register contents in the FPGA. In some applications this is not desired. Setting this bit to one prevents SYSRESET* from resetting the axis.
3	*Reserved*.
4	*Trigger Delay Enable*. This enables a delay (1 µs) in the sampling caused by SCLK0. The delay is approximately equal to the delay through the electronics so that the data sample corresponds to the position at the time when the SCLK input occurred. Sampling caused by SCLK1 does not have a selectable delay.
5	*SCLK Divide by 2 Enable.* (Axis 3 only) This selects an optional divide-by-2 for the Sample Timer and SCLK Divider drives of SCLK0 and SCLK1. The standard SCLK output is a low pulse 50 ns wide. With the divide-by-2 selected, the sample timer and SCLK divider outputs are square waves with a 50% duty cycle, at half the normal frequency. This may be useful when customer hardware connects to SCLK0 or SCLK1, or when SCLK0 or SCLK1 is used to drive SCLK2 on another measurement board. When using the SCLK Divider with the SCLK Divide by 2 function, the two SCLK outputs are synchronized so a falling edge on the slower output is always coincident with a falling edge on the faster output. In some cases (when the SCLK Divider register is an even number), this results in the Sample Timer divided-by-2 output having one cycle soon after startup with a longer period.
6	*SCLK Divider Enable.* (Axis 3 only) This enables a secondary SCLK output with a period that is an integer multiple of the SCLK Timer output. The SCLK Divider output is on SCLK0 or SCLK1, as selected by the SCLK Timer Drive bit below. The rate is selected by the SD[3:0] bits in Control Register 15. The SCLK Divider signal is synchronized so that it always occurs at the same time as the corresponding SCLK Timer signal.

continued

Control Register 16 Functions (continued)

Bit	*Description*
7	*SCLK Timer Enable*. (Axis 3 only) This enables the sample timer that can be used to drive the SCLK signal with a periodic signal. The period of the timer is specified by the Sample Timer register. The signal is a 50 ns wide low-going pulse. When the timer is enabled, the first pulse output will be approximately one timer period later.
8	*SCLK Timer Drive*. (Axis 3 only). This determines which SCLK signals are driven by the SCLK Timer and SCLK Divider when the outputs are enabled. *Bit 8* — *SCLK Timer Drive* — *SCLK Divider Drive* 0 — SCLK0 — SCLK1 1 — SCLK1 — SCLK0
9	*SCLK0 Out Enable*. (Axis 3 only) This enables SCLK0 to drive the P2 bus. The first board in the reference tree is usually chosen to drive the SCLK signals. The SCLK0 signal must not have more than one driver enabled at any time. The enable signal is synchronized to the 20 MHz clock to prevent partial output pulses.
13-10	*SCLK0 Sample Time*. SST0[3:0] This determines the time within the system clock cycle that the SCLK0 signal is sampled. Correct setting of this register is listed in Table 3-14. The powerup default is 3.
15-14	*SCLK0 Delay*. SD0[1:0] This delays the SCLK0 signal up to 150 ns, as shown in Table 4-7.

Table 4-7 SCLK0 Delay

SD01	SD00	Delay (ns)
0	0	0
0	1	50
1	0	100
1	1	150

Control Register 17

Axis	VME (read/write)	P2 (read/write)
1 (2)	0x003E	0x1F
3 (4)	0x203E	0x9F

Control Register 17 Functions

Bit	*Description*
3-0	*P2 Address*. P2A[11:8] This selects the P2 base address when SW5-1 is set to "0" (on). For more information see section 3-3. This may only be written from the VMEbus interface.
4	*Reserved*.
5	*P2 IO Enable*. This bit enables read and write operations of the P2 bus. This bit can only be written from the VMEbus interface. The powerup default is 0 (disabled) if SW5-1 is on, or 1 (enabled) if SW5-1 is off.
7-6	*SCLK2 Resync Mode*. (Axis 3 only) SRM[1:0]. This controls the operation of the SCLK2 input as shown in Table 4-8.
8	*SCLK2 Resync Drive*. (Axis 3 only) 0=SCLK0, 1=SCLK1. This determines which SCLK signal is driven by the resynchronized SCLK2 signal when it is enabled.
9	*SCLK1 Out Enable*. (Axis 3 only) This enables SCLK1 to drive the P2 bus. . The first board in the reference tree is usually chosen to drive the SCLK signals. The SCLK1 signal must not have more than one driver enabled at any time. The enable signal is synchronized to the 20 MHz clock to prevent partial output pulses.
13-10	*SCLK1 Sample Time*. SST1[3:0] This determines the time within the system clock cycle that the SCLK1 signal is sampled. Correct setting of this value is described in Table 3-13. The powerup default is 3.
15-14	*SCLK1 Delay*. SD1[1:0] This delays the SCLK1 signal up to 150 ns as shown in Table 4-9. This value is normally set to zero.

Table 4-8 SCLK2 Resync Mode

SRM1	SRM0	SCLK2 Resync Input
0	0	Disabled
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Table 4-9 SCLK1 Delay

SD11	SD10	Delay
0	0	0
0	1	50 ns
1	0	100 ns
1	1	150 ns

Data Age Adjust

Axis	VME (read/write)	P2 (read/write)
1	0x0030	0x18
2	0x1030	0x58
3	0x2030	0x98
4	0x3030	0xD8

This is the static data age adjust value described in Chapter 3.

Data Age Adjust Register Functions

Bit	*Description*
15-0	*DAA[15:0]* Data Age Adjust(15:0) – The range of the Data Age register depends on the firmware version and firmware revision Extended range: 0-40959 (0-0x9fff), or 0 to 1333 ns. (see Appendix D line 16 for Normal range 0-8191 (0-0x1fff), or 0 to 266 ns, applicability to other products.)

Data Age RAM

Axis	VME (read/write)	P2
1	0x0100-0x01FE	-
2	0x1100-0x11FE	-
3	0x2100-0x21FE	-
4	0x3100-0x31FE	-

This RAM contains APD phase compensation data for reference use only. It is write protected.

The Aux registers (0x100-0x1FE) share the same address space as the Data Age RAM (0x100-0x1FE). To access the Data Age RAM, clear the *Enable Aux Data* bit in Control Register 2. The power up default of the *Enable Aux Data* bit is 0.

Diag ADC

Axis	VME (read)	P2
1	0x00AA	-
3	0x20AA	-

This is the diagnostic ADC that is used to measure on-board voltages. The diagnostic ADCs may be operated by either the user VME interface, or the internal processor interface. During factory calibration, these reading are stored in EEPROM.

Diag ADC Register Functions

Bit	*Description*
11-0	*ADC[11:0]* This register is updated once shortly after the Test Control 1 register is written to. When the *ADC Busy* bit is 0, the data in this register is valid.
14-12	*Reserved*.
15	*ADC Busy*. This indicates that the ADC data in the Diag ADC register is not yet valid. This bit is cleared when valid data is ready after writing the *ADC Mux* value to the Test Control 1 register.

To read the Diagnostic ADC:

1. Poll the *ADC Busy* bit until it is in a '0' state. This time delay will be a maximum of approximately 300 µs.
2. Write the desired *ADC Mux* value to the Test Control 1 register. Note that the *ADC Mux* value is different from the ADC channel number.
3. Poll the *ADC Busy* bit until it is in a '0' state. This time delay will be approximately 150 µs or a maximum of 300 µs.
4. Convert the *ADC[11:0]* value to volts using the appropriate equation as described in Table 4-11.

The ADC Mux is selected by Test Control 1 register bits 4:0. ADC Channels 0 to 23 are accessed through the master FPGA (axis 3), ADC Channels 24 to 31 are accessed through the slave FPGA (axis 1). The Test Control 1 and Diag ADC registers for the ZMI 4104 also exist in the slave FPGA.

Table 4-10 Diagnostic ADC Inputs

ADC Channel	ADC Mux	FPGA	ADC	Equation	Voltage
0	0	Master	1	2	+5 V Digital PS
1	4	Master	1	2	+3.3 V Digital PS
2	1	Master	1	7	+2.5 V Digital PS
3	5	Master	1	1	+1.8 V Digital PS
4	2	Master	1	1	+1.2 V Digital PS
5	6	Master	1	2	+5 V Analog PS
6	3	Master	1	2	+3.3 V Analog PS
7	7	Master	1	5	-5 V Analog PS
8	8	Master	2	3	+15 V Analog PS
9	12	Master	2	6	-15 V Analog PS
10	9	Master	2	6	-12 V Analog PS
11	13	Master	2	3	+10 V Analog PS
12	10	Master	2	4	HV PS
13	14	Master	2	2	VCXO Control V
14	11	Master	2	9	Ref SSI
15	15	Master	2	8	Ref Offset
16	16	Master	3	4	Meas 3 Bias
17	20	Master	3	4	Meas 4 Bias
18	17	Master	3	5	Meas 3 DC
19	21	Master	3	5	Meas 4 DC
20	18	Master	3	1, 10	Meas 3 Temp
21	22	Master	3	1, 10	Meas 4 Temp
22	19	Master	3	1	DAC Reference
23	23	Master	3	-	Spare
24	0	Slave	4	4	Meas 1 Bias
25	4	Slave	4	4	Meas 2 Bias
26	1	Slave	4	5	Meas 1 DC
27	5	Slave	4	5	Meas 2 DC
28	2	Slave	4	1, 10	Meas 1 Temp
29	6	Slave	4	1, 10	Meas 2 Temp
30	3	Slave	4	-	Spare
31	7	Slave	4	-	Spare

Table 4-11 Diagnostic ADC Ranges

Equation No.	Equation	FS Range
1	V = N * 0.6104 mV	0 to 2.5 V
2	V = N * 1.8311 mV	0 to 7.5 V
3	V = N * 5.295 mV	0 to 21.7 V
4	V = N * 61.646 mV	0 to 252 V
5	V = 2.5 V – (4096 – N) * 2.090 mV	-6 to +2.5 V
6	V = 2.5 V – (4096 – N) * 5.295 mV	-19.2 to +2.5 V
7	V = N * 1.2208 mV	0 to 5.0 V
8	V = 2.5 V – (4096 – N) * 3.803 mV	-13.1 to +2.5 V
9	V = N * 0.7327 mV	0 to 3.0 V
10	T = (N * 0.6104 - 1864.1)/-11.71	0 C to +65 C

Diag FFT Control

Axis	VME (read/write)	P2
1 (2)	0x00B4	-
3 (4)	0x20B4	-

This is the diagnostic register that is used to read FFT RAM. This register is not present in the 8020-9274-01 firmware.

Diag FFT Control Register Functions

Bit	*Description*
5-0	*Data Read Page*. This selects the desired page of data to be read from the Diag FFT RAM.
7-6	*Reserved*.
8	*Data Write Select*. This selects the desired axis to have data stored in the Diag FFT RAM.
9	*Start on Compare*. This enables the start of data acquisition into the Diag FFT RAM data memory when the P2D comparator output changes from a ‘0’ to a ‘1’. The choice of P2d comparator output is selected by the *Data Write Select* bit. It is not necessary for the P2D comparator output to be enabled for this function to operate.
10	*Start on Input*. This enables the start of data acquisition into the Diag FFT RAM data memory when the user P2D input changes from a ‘1’ to a ‘0’.
11	*Reserved.*
15-12	*Data Source.* (see “Diag FFT RAM Data Source” table.*)*

To use the diagnostic RAM, perform the following steps:

1. Select the desired axis with the *Data Write Select* bit in the Diag FFT Control register.
2. Start acquiring data by writing a '1' to the *Start Diag FFT Data* bit in Test Command 1 register.
3. Wait until the *Diag FFT Data Busy* bit in the Test Status 1 register is '0'. This time depends on the number of samples and the rate of the data source. ADC data is at 120 MHz (275µs) , DFT and CEC data is at 10 MHz (820 µs or 410 µs), and position data is at the SCLK rate set by the user.
4. Read the data. Select the *Data Read Page* in the Diag FFT Control register, and read 512 words of data from Diag FFT RAM. Perform this step for each page 0 to 63.
5. Analyze the data. A 32768 point FFT (Fast Fourier Transform) with a Nuttall window is suggested.

Table 4-12 Diag FFT RAM Data Sources

Data Source	Format	Samples	Data Source
0000 (default)	12 bit integer (sign extended)	32768	ADC Data
0001(1)	Complex	8192	DFT Output (CEC input)
0010(1)	Complex	8192	CE Compensation
0011(1)	Complex	8192	CEC Output
0100(1)	Complex Complex	4096 4096	CEC Input CEC Output
0101(1)	Complex Complex	4096 4096	CEC Input axis 1 (or 3), CEC Input axis 2 (or 4)
0110(1)	Complex Complex	4096 4096	CEC Output axis 1 (or 3), CEC Output axis 2 (or 4)
0111(1)	-	-	Reserved
1000	32 bit Signed	16384	Position
1001	32 bit Signed 32 bit Signed	8192 8192	Position axis 1 (or 3), Position axis 2 (or 4)
1010-1111	-	-	Reserved

(1) Available only on ZMI 4104C.

Diag FFT RAM Data

Axis	VME (read)	P2
1 (2)	0x0400-0x07FE	-
3 (4)	0x2400-0x27FE	-

The Diag FFT RAM is controlled by the Diag FFT Control register and the Test command 1 register. The status is read from the Test Status 1 register. The *Data Write Select* bit in the Diag FFT Control register selects the axis data to be acquired.

Table 4-13 Diag FFT RAM Write Select Bit

Data	Diag FFT RAM	Data Write Select
Axis 1	axis 1	0
Axis 2	axis 1	1
Axis 3	axis 3	0
Axis 4	axis3	1

The Diagnostic FFT RAM can store 32768 consecutive samples of the input data for one selected axis. The data stored in the Diag FFT RAM is from the source specified by the *Data Source* bits in the Diag FFT Control register. The data format depends on the data source.

- ADC data is 12-bit data sign extended to 16 bits.
- Complex data is represented in four consecutive words as follows:
  <4 bit sign extension> <12 MSB real>
  <4 bit zero> <9 LSB real> <3 bit zero>
  <4 bit sign extension> <12 MSB imaginary>
  <4 bit zero> <9 LSB imaginary> <3 bit zero>
- Position data is from the VME Position register, as sampled by SCLK. It is a 32-bit signed value (including three fractional bits) represented in two consecutive 16-bit words, MSB first. The SCLK rate may be as fast as 10 MHz.
- When two complex or position values are stored, they are stored in adjacent pairs representing a single sample time.

The memory is arranged as 64 pages of 512 words each, the page is selected by the Diag FFT Control register. This data is used for diagnostics to detect low-level noise and cyclic errors. The RAM data should not be read while data is being acquired, as indicated by the *Diag FFT Data Busy* bit in the Test Status 1 register. When busy, an attempt to read data may return invalid data.

Diag FFT RAM Data Register Functions

Bit	*Description*
15-0	*DFR[15:0]*

Diag RAM Data

Axis	VME (read)	P2
1	0x0800-0x0FFE	-
2	0x1800-0x1FFE	-
3	0x2800-0x2FFE	-
4	0x3800-0x3FFE	-

This Diagnostic RAM can store 1024 consecutive samples of the input data.

Diag RAM Data Register Functions

Bit	*Description*
11-0	*DRD[11:0]*
15-12	*Reserved.*

Diag RAM Start

Axis	VME (read)	P2
1	0x00CE	-
2	0x10CE	-
3	0x20CE	-
4	0x30CE	-

This specifies the location in the Diagnostic RAM where the data begins. Data may be read from the diagnostic RAM as a circular buffer beginning at this location plus one and wrapping around modulo 1024.

For example, for N = 0 to 1023
DiagRamData (N) = VME Read (0x800 + 2 * ((DiagRamStart + 1 + N) Mod 1024))

Diag RAM Start Register Functions

Bit	*Description*
9-0	*DRS[9:0]*
15-10	*Reserved.*

Diag SSI RAM

Axis	VME (read)	P2
1	0x0200-0x03FE	-
2	0x1200-0x13FE	-
3	0x2200-0x23FE	-
4	0x3200-0x33FE	-

This Diagnostic RAM contains information on the signal strength. This data is written once during initialization when an axis reset is performed. If the *Enable Reset Finds Velocity* bit in Control Register 3 is set, locations 22 to 178 (address offsets 44 to 356) contain the signal strength for frequencies from 4.6 MHz to 36.1 MHz. If the *Enable Reset Finds Velocity* bit is not set, location 96 (address offset 192) contains the signal strength at 20.0 MHz. The scale factor of these values is approximately 4.5% greater than the SSI Average value.

Frequency = Location Offset * 208.33 kHz.

Diag Temp Monitor Control

Axis	VME (read/write)	P2
1 (2)	0x00A4	-
3 (4)	0x20A4	-

This specifies the mode, address and command for the diagnostic temperature monitor. There are two monitors, one for each FPGA. The local temperature is the temperature at the temp monitor device; the remote temperature is the temperature of PCB near the FPGA. After powerup the default value of this register is automatically written to the diagnostic temperature monitor. This configures the device for a +85°C alarm for the FPGA temperature sensor.

Diag Temp Monitor Control Register Functions

Bit	*Description*
7-0	*DTC[7:0]* Diagnostic Temperature Monitor Command. The commands are shown in the following table. The powerup default value for the command is 0x0d = WRHA.
14-8	*DTA[6:0]* Diagnostic Temperature Monitor Address. The powerup default for the address is 0x2A.
15	*Reserved.*

To reset the alarm output after an over temperature condition:

1. Write 0x2A02 to the Diag Temp Monitor Control register.
2. Wait until the *Diag Temp Monitor Busy* bit of the Diag Temp Monitor Read register is zero (approximately 400 µs).
3. Write 0x0c00 to the Diag Temp Monitor Control register.
4. Wait until the *Diag Temp Monitor Busy* bit of the Diag Temp Monitor Read register is zero (approximately 200 µs).

Table 4-15 Diagnostic Temperature Monitor Commands

Register	Command	Function
RLTS	00h	Read local temperature: returns latest temperature
RRTE	01h	Read remote temperature: returns latest temperature
RSL	02h	Read status byte (reset flags)
RLHN	05h	Read local THIGH limit
RLLI	06h	Read local TLOW limit
RRHI	07h	Read remote THIGH limit
RRLS	08h	Read remote TLOW limit
WLHO	0Bh	Write local THIGH limit
WLLM	0Ch	Write local TLOW limit
WRHA	0Dh	Write remote THIGH limit
WRLN	0Eh	Write remote TLOW limit

Table 4-16 Diag Temp Monitor Status Byte

Bit	Name	Function
7	BUSY	A/D is busy.
6	LHIGH	Local high temperature alarm.
5	LLOW	Local low temperature alarm.
4	RHIGH	Remote high temperature alarm.
3	RLOW	Remote low temperature alarm.
2	OPEN	Remote sensor open.
1-0	-	Reserved

Diag Temp Monitor Read

Axis	VME (read)	P2
1 (2)	0x00A8	-
3 (4)	0x20A8	-

This contains the value read from the diagnostic temperature monitor. The read operation is initiated by writing a read command to the Diag Temp Monitor Control register. There are two monitors, one for each FPGA. The most significant bit indicates when the temperature monitor is busy transferring data. The value read indicates the temperature in degrees Celsius.

Diag Temp Monitor Read Register Functions

Bit	*Description*
7-0	*DTR[7:0]* Diag Temp Read data.
14-8	*Reserved.*
15	*Diag Temp Monitor Busy*. When this bit is zero, the read data is valid.

To read the Diagnostic Temperature Monitor:

1. Poll the *Diag Temp Monitor Busy* bit until it is in a '0' state. This time delay will be a maximum of approximately 400 us.
2. Write to the Diag Temp Monitor Control register. For example, a value of 0x2A00 will read the board surface temperature, or a value of 0x2A01 will read the FPGA temperature.
3. Poll the *Diag Temp Monitor Busy* bit until it is in a '0' state. This time delay will be approximately 400 us.
4. The *DTR[7:0]* value contains the temperature in degrees C.

Diag Temp Monitor Write

Axis	VME (read/write)	P2
1	0x00A6	-
3	0x20A6	-

This contains the value to be written to a register in the diagnostic temperature monitor. The write operation is initiated by writing a write command to the Diag Temp Monitor Control register. There are two monitors, one for each FPGA.

Diag Temp Monitor Write Register Functions

Bit	*Description*
7-0	*DTW[7:0]* Diag Temp Write data. The powerup default value is 85 = 0x55.
15-8	*Reserved.*

EEPROM Control

Axis	VME (read/write)	P2
3 only	0x20AC	-

This register controls the operation of the EEPROM and specifies the address to be read or written. The EEPROM may be operated by either the user VME interface, or the internal processor interface. The EEPROM is addressed as 1024 16-bit locations.

EEPROM Control Register Functions

Bit	*Description*
9-0	*EEA[9:0]* EEPROM Address.
11-10	*Reserved.*
13-12	*EEOP[1:0]* EEPROM Operation. The operation field together with the address field selects the operation as shown in EEPROM Operation table.
15-14	*Reserved*

Table 4-17 EEPROM Operation

Operation	EEOP1-EEOP0	Address
Read	10	Read Address
Write Enable	00	0x300
Write	01	Write Address
Write All	00	0x100
Write Disable	00	0x000

To perform an EEPROM Read:

1. Verify that the *EEPROM Error* bit in Test Status 1 register is in a '0' state. If not, write a '1' to the *Clear EEPROM Error* bit in Test Command 1 register.
2. Poll the *EEPROM Busy* bit in Test Status 1 register until it is in a '0' state. This time delay will be a maximum of approximately 600 µs.
3. Write the read opcode (*EEOP[1:0]* = 10) and the read address (*EEA[9:0]*) to the EEPROM Control register. The *EEPROM Busy* bit in Test Status Register 1 will immediately change to a '1' state (busy).
4. Poll the *EEPROM Busy* bit in Test Status Register 1 until it returns to a '0' state. This time delay will be approximately 300 µs or a maximum of 600 µs. For a read operation, the busy bit returns to the '0' state after all data bits have been shifted in.
5. Read the 16-bit data value from the EEPROM Read register.

EEPROM Read

Axis	VME (read)	P2
3 only	0x20B0	-

This register contains the EEPROM data that is read. The read operation is initiated by a write to the EEPROM Control register. The data is not valid until the *EEPROM Busy* bit in Test Status Register 1 returns to a zero.

EEPROM Write

Axis	VME (read/write)	P2
3 only	0x20AE	-

This register contains data that will be written. The write operation is initiated by a write to the EEPROM Control register.

Firmware Revision

Axis	VME (read)	P2
1	0x00C8	-
2	0x10C8	-
3	0x20C8	-
4	0x30C8	-

This contains the firmware revision code, which is defined within the FPGA (Field Programmable Gate Array) design. This contains two ASCII characters, for example “A ”. For prototype or engineering use, this is a numeric value, for example “01”. The firmware revision code is always the same for all axes.

Firmware Version

Axis	VME (read)	P2 (read)
1	0x000E	0x07
2	0x100E	0x47
3	0x200E	0x87
4	0x300E	0xC7

This contains the firmware version code, which is defined within the FPGA (Field Programmable Gate Array) design. The firmware version code is always the same for all axes. See also Appendix D.

Table 4-18 4100 Product Part Numbers

Product	Board P/N and Revision	Firmware Version	Register last four digits
ZMI 4000	8020-0500-01 rev A, B, C	8020-9274-01	0x7401
ZMI 4000	8020-0500-07 rev A and later	8020-9274-01	0x7401
ZMI 4000	8020-0500-01 rev D and later	8020-9274-02	0x7402
ZMI 4000	8020-0500-02 rev A and later	8020-9274-02	0x7402
ZMI 4004CEC	8020-0500-03 rev A and later	8020-9274-03	0x7403
ZMI 4100	8020-0700-xx Rev A and later	8020-9276-01	0x7601

GSE (Gain Set Error) Registers

The Gain Set Error registers assist in diagnosing errors related to setting APD gain during Sig RMS Adjust, Constant Optical Power or Constant Gain Modes. If APD gain is not achieved within an allotted time, the APD Command Error bit will be set along with an APD Error code, APD Math Gain (error #135) in the APD Error Code Register. Note: regardless of an error condition, the Bias Calc Complete bit will be set upon completion of a bias control command. If a gain set error condition occurs, Target Gain, Actual Gain, Measure DC, and SigRMS will be updated at the following registers: GSE Target Gain Register, GSE Actual Gain Register, GSE SigRMS Register, GSE MeasDC Low (low word) Register and GSE MeasDC High (high word).

GSE Target Gain

Axis	VME (read)	P2
1	0x01BC	-
2	0x11BC	-
3	0x21BC	-
4	0x31BC	-

This register contains the value of target gain on a gain set error condition.

GSE Actual Gain

Axis	VME (read)	P2
1	0x01BE	-
2	0x11BE	-
3	0x21BE	-
4	0x31BE	-

This register contains the value of actual gain on a gain set error condition.

GSE SigRMS

Axis	VME (read)	P2
1	0x01C0	-
2	0x11C0	-
3	0x21C0	-
4	0x31C0	-

This register contains the value of SigRMS gain on a gain set error condition.

GSE MeasDC Low

Axis	VME (read)	P2
1	0x01C2	-
2	0x11C2	-
3	0x21C2	-
4	0x31C2	-

This register contains the lower 16-bit value of Meas DC on a gain set error condition.

GSE MeasDC High

Axis	VME (read)	P2
1	0x01C4	-
2	0x11C4	-
3	0x21C4	-
4	0x31C4	-

This register contains the upper 16-bit value of Meas DC on a gain set error condition.

Offset

Axis	VME			P2		
	MSB (read/write)	LSB (read/write)	Ext (read/write)	MSB (read/write)	LSB (read/write)	Ext (read/write)
1	0x0068	0x006A	0x006C	0x34	0x35	0x36
2	0x1068	0x106A	0x106C	0x74	0x75	0x76
3	0x2068	0x206A	0x206C	0xB4	0xB5	0xB6
4	0x3068	0x306A	0x306C	0xF4	0xF5	0xF6

This contains the offset value that is subtracted from all position measurements. This is a 37-bit register as described in the beginning of this chapter.

Opt Power DC L2

Axis	VME (read)	P2
1	0x01A4	-
2	0x11A4	-
3	0x21A4	-
4	0x31A4	-

This register specifies the logarithm of the approximate DC optical power, based on calculations using the APD_Gain_L2 value, and Meas DC from the Diag ADC Register. The units of power are microwatts into the fiber optic receiver. This register is periodically updated in all APD bias control modes. This value is useful for calculating the approximate mixing efficiency (Opt Power L2 - Opt Power DC L2). The register value is calculated as follows:

$$Opt\_Power\_DC\_L2 = Log2(Opt\_Power\_DC)*1024$$

$$Opt\_Power\_DC = 2^{(Opt\_Power\_DC\_L2/1024)}$$

The "*Enable Aux Data* bit in Control Register 2 must be enabled to access these values.

The maximum signal level for this register is approximately 10 uW to 30 uW, depending on APD gain. Above this level, a constant value of 6804 (0x1A94) representing 100 uW is provided. The minimum signal level for this register is approximately 0.1 uW to 1 uW, depending on APD gain. Below this level, the measurement is not accurate, and a constant value of -6804 (0xE56C) representing 0.01 uW is provided.

Opt Power L2

Axis	VME (read)	P2
1	0x0192	-
2	0x1192	-
3	0x2192	-
4	0x3192	-

This register specifies the logarithm of the approximate optical power, based on calculations using the APD Gain L2 and Sig RMS L2 values. This register is periodically updated in all APD bias control modes. The units of optical power are microwatts into the fiber optic receiver. The register value is calculated as follows:

$$Opt\_Power\_L2 = Log2(Opt\_Power)*1024$$

$$Opt\_Power = 2^{(Opt\_Power\_L2/1024)}$$

The "*Enable Aux Data* bit in Control Register 2 must be enabled to access these values.

Opt Power L2 Max

Axis	VME (read)	P2
1	0x019E	-
2	0x119E	-
3	0x219E	-
4	0x319E	-

This register provides the maximum value of the Opt Power L2 register since the issue of a *Reset Opt Power L2 Min/Max* command in the Test Command 0 register.

The "*Enable Aux Data* bit in Control Register 2 must be enabled to access these values.

Opt Power L2 Min

Axis	VME (read)	P2
1	0x019C	-
2	0x119C	-
3	0x219C	-
4	0x319C	-

This register provides the minimum value of the Opt Power L2 register since the issue of a *Reset Opt Power L2 Min/Max* command in the Test Command 0 register.

The "*Enable Aux Data* bit in Control Register 2 must be enabled to access these values.

P2 Absolute Phase

Axis	VME	P2 (read)
1	-	0x14
2	-	0x54
3	-	0x94
4	-	0xD4

This register provides an absolute measure of the phase of the measurement signal. This is used for data age calibration. The filtering for this measurement is identical to the filtering for the position measurement. The phase is a 13-bit value, which provides resolution of λ/8192, or 8 times finer than the position measurement. This is equivalent to 6.1 ps when measuring the 20 MHz reference. This is sampled simultaneously with the P2 Position register.

P2 Command Register

Axis	VME	P2 (write)
1	-	0x00
2	-	0x40
3	-	0x80
4	-	0xC0

P2 Command Register Functions

Bit	*Description*
0	*Reset VME Errors*. This resets all errors in the VME Error Status registers.
1	*Reset P2 Errors*. This resets all errors in the P2 Error Status registers.
2	*Reset Position*. This resets or presets the position measurement. Position reset resets the measurement function, but does not reset errors. If the *Preset Enable* bit in Control Register 3 is set, the value in the Preset Position register is preset into the position measurement. The reset or preset value is before the Offset register is subtracted.
3	*Reset Time*. This resets the time register.
4	*Reset Position Quick*. This performs a quick reset or preset of the position register.
5	*Reset Axis*. An axis reset resets the measurement function and all errors.
6	*Start Bias Calc.* This command starts the process to determine the APD bias voltage. The *Cmd Busy* bit in Status Register 1 is set immediately. When the command is recognized by the controller, the *Bias Calc Busy* bit in Status Register 1 is set, and the *Cmd Busy* bit is cleared. When the process is complete, the *Bias Calc Busy* bit is cleared and the *Bias Calc Complete* bits in P2 Error Status 2 and VME Error Status 2 registers are set. When the *Cmd Busy* bit or *Bias Calc Busy* bit is set, write operations to Control Register 5 or to APD control registers (VME offsets 0x180 to 0x1FE) are inhibited, and will produce a *Write Protect Error* in P2 Error Status 2 and VME Error Status 2 registers.
9-7	*Reserved*.
10	*Comparator Preset 0*. This presets the comparator hysteresis to zero.
11	*Comparator Preset 1*. This presets the comparator hysteresis to one.
12	*Load Position.* This presets the position to the value in the Preset Position register. Load position only loads a new position value, it assumes that a valid position measurement exists.
15-13	*Reserved*.

For more information on reset functions, see Chapter 3.

P2 Error Clear

Axis	Error Clear 0		Error Clear 1		Error Clear 2
	VME (write)	P2 (write)	VME (write)	P2 (write)	P2 (write)
1	0x0024	0x12	0x0026	0x13	0x0F
2	0x1024	0x52	0x1026	0x53	0x4F
3	0x2024	0x92	0x2026	0x93	0x8F
4	0x3024	0xD2	0x3026	0xD3	0xCF

Writing a one to a bit in these registers clears the corresponding bit in the P2 Error Status register. If the error condition is still present, the error bit will be immediately set again.

For bit descriptions, refer to Section 4.2.

P2 Error Status

Axis	Error Status 0		Error Status 1		Error Status 2
	VME (read)	P2 (read)	VME (read)	P2 (read)	P2 (read)
1	0x0024	0x12	0x0026	0x13	0x0F
2	0x1024	0x52	0x1026	0x53	0x4F
3	0x2024	0x92	0x2026	0x93	0x8F
4	0x3024	0xD2	0x3026	0xD3	0xCF

The bits in this register are set by error conditions, and cleared by writing a one to the corresponding bit in the P2 Error Clear register, or by a reset operation.

For bit descriptions, refer to Section 4.2.

P2 Interrupt Enable

Axis	P2 Interrupt Enable 0		P2 Interrupt Enable 1		P2 Interrupt Enable 2
	VME (read/write)	P2 (read/write)	VME (read/write)	P2 (read/write)	P2 (read/write
1	0x0020	0x10	0x0022	0x11	0x0E
2	0x1020	0x50	0x1022	0x51	0x4E
3	0x2020	0x90	0x2022	0x91	0x8E
4	0x3020	0xD0	0x3022	0xD1	0xCE

The bits in this register enable a P2 interrupt when a corresponding error occurs in the P2 Error Status register.

For bit descriptions, refer to Section 4.2.

P2 Position

Axis	MSB (read)	LSB (read))	Ext (read)	Errs (read)
1	0x20	0x21	0x22	0x23
2	0x60	0x61	0x62	0x63
3	0xA0	0xA1	0xA2	0xA3
4	0xE0	0xE1	0xE2	0xE3

This contains the position value that is read through the P2 bus. This is a 37-bit register as described in the beginning of this chapter. When the *P2 Latch Mode* bit in Control Register 4 is set to 1, the P2 position, time, velocity, and absolute phase values are latched by reading the MSB.

P2 Time

Axis	MSB (read)	LSB (read))
1	0x2A	0x2B
2	0x6A	0x6B
3	0xAA	0xAB
4	0xEA	0xEB

This contains the time value that is read through the P2 bus.

P2 Velocity

Axis	MSB (read)	LSB (read))
1	0x28	0x29
2	0x68	0x69
3	0xA8	0xA9
4	0xE8	0xE9

This contains the velocity value that is read through the P2 bus.

Phase Comp Bias

Axis	VME (read/write)	P2
1	0x00E0	-
2	0x10E0	-
3	0x20E0	-
4	0x30E0	-

This register is primarily for ZYGO test use; it is write-protected. This register is used by the APD microcontroller for compensation of changes in phase shift and data age due to changes in APD bias.

Phase Comp Control

Axis	VME (read/write)	P2
1	0x00E2	-
2	0x10E2	-
3	0x20E2	-
4	0x30E2	-

This register is primarily for ZYGO test use. This register controls the operation of the APD phase compensation.

Phase Comp Diag

Axis	VME (read)	P2
1	0x00E4	-
2	0x10E4	-
3	0x20E4	-
4	0x30E4	-

This register is primarily for ZYGO test use. This contains the APD phase compensation value plus the fine data age compensation, sign extended to 16 bits, for diagnostic purposes. The units of this register are fractional LSB, or $2\pi/8192$.

Phase Noise Average

Axis	VME (read)	P2
1	0x00DA	-
2	0x10DA	-
3	0x20DA	-
4	0x30DA	-

This is a number that is an approximation to the RMS phase noise on the measurement. This value is updated asynchronously at a 1 kHz rate.

Phase Noise Limit

Axis	VME (read/write)	P2 (read/write)
1	0x002E	0x17
2	0x102E	0x57
3	0x202E	0x97
4	0x302E	0xD7

This specifies the maximum value allowed for the Phase Noise Average. If this value is exceeded, the *Phase Noise Error* is set in the VME Error Status register and the P2 Error Status register. The powerup default value is 0x07ff (2047).

Phase Noise Peak

Axis	VME (read)	P2
1	0x00DB	-
2	0x10DB	-
3	0x20DB	-
4	0x30DB	-

This is the maximum-minus-minimum value of the difference signal within the glitch filter. This register is reset by an axis reset or by writing a one to the *Reset Phase Noise Peak* bit in the Test Command 0 register.

Preset Pos

Axis	VME			P2		
	MSB (read/write)	LSB (read/write)	Ext (read/write)	MSB (read/write)	LSB (read/write)	Ext (read/write)
1	0x0060	0x0062	0x0064	0x30	0x31	0x32
2	0x1060	0x1062	0x1064	0x70	0x71	0x72
3	0x2060	0x2062	0x2064	0xB0	0xB1	0xB2
4	0x3060	0x3062	0x3064	0xF0	0xF1	0xF2

This is the preset value that is loaded into the position register if the *Preset Enable* bit in Control Register 3 is set during an axis reset or position reset or by the load position command. This is a 37-bit register as described in the beginning of this chapter.

PROM Revision

Axis	VME (read)	P2
1	0x0182	-
2	0x1182	-
3	0x2182	-
4	0x3182	-

This register provides the revision level of the PROM data. This register contains two ASCII characters, for example “A “. For prototype and engineering use, this register contains a numeric value, for example “01”.

PROM Version

Axis	VME (read)	P2
1	0x0180	-
2	0x1180	-
3	0x2180	-
4	0x3180	-

This register provides version of the combined firmware and software in the PROM used to program the FPGA. This register contains the PROM version expressed as four hexadecimal digits, for example SPM8020-9278-03 appears as 0x7803.

Table 4-19 4100 PROM SPM Numbers

Product	Prom SPM number	PROM Version Register
ZMI 4104	SPM8020-9278-03	0x7803
ZMI 4104C	SPM8020-9278-05	0x7805

PSD (Power Supply Diagnostic) Registers

The following Power Supply Diagnostic registers are provided to assist in diagnosing Low Voltage, High Voltage and Bias Supply failures:

Note: these registers are available on axis 3 only.

Axis	Register name	VME (read)	P2 (read)
3 only	PSD LVPS Error ID	0x21E0	-
3 only	PSD LVPS First Err V	0x21E2	-
3 only	PSD LVPS First Err Max V	0x21E4	-
3 only	PSD LVPS First Err Min V	0x21E6	-
3 only	PSD LVPS First Err VCC In	0x21E8	-
3 only	PSD VCC In Fault V	0x21EA	-
3 only	PSD VCC In Max V	0x21EC	-
3 only	PSD VCC In Min V	0x21EE	-
3 only	PSD HVPS Error	0x21F0	-

PSD LVPS Error ID

This is a diagnostic register that indicates which of the Low Voltage Power Supplies went outside the limits since VME reset or power up. The Identification Bits (ID#) ID11-0 identify which of the Low Voltage Power Supplies (LVPS) exceeded the maximum or minimum limit. This register is cleared on power-up initialization.VCC In is monitored in PSD VCC In Max V and PSD VCC In Min V registers.

ID#	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
LVPS	+10A	-12A	-15A	15A	-5A	3.3A	5A	1.2D	1.8D	2.5D	3.3D	5.0V

PSD LVPS First Err V

This diagnostic register captures the fault voltage of first LVPS to post an error (except for Vcc In). Bits 15-12 indicate the LVPS ID, bits 11–0 indicate the LVPS supply voltage (ADC counts). This register is cleared on power-up initialization.

PSD LVPS First Err Max V

This diagnostic register captures the maximum voltage of first LVPS to post an error (except for Vcc In). It will continue to be updated after a LVPS limit fault is detected. Bits 15-12 indicate LVPS ID, bits 11-0 indicate LVPS supply voltage (ADC counts). This register is cleared on power-up initialization.

PSD LVPS First Err Min V

This diagnostic register captures the minimum voltage of first LVPS to post an error (except for Vcc In). It will continue to be updated after LVPS limit fault is detected. Bits 15-12 indicate LVPS ID, bits 11-0 indicate LVPS supply voltage (ADC counts). This register is cleared on power-up initialization.

PSD LVPS First Err VCC In

This diagnostic register captures the Vcc In voltage (ADC counts) in bits 11-0, when the first LVPS error is detected (except when LVPS error = Vcc In). This register is cleared on power-up initialization.

PSD VCC In Fault V

This diagnostic register captures the Vcc In fault voltage (ADC counts) in bits 11-0, when Vcc In voltage exceeds the maximum or minimum limits. This register is cleared on power-up initialization.

PSD VCC In Max V

This diagnostic register captures the Vcc In maximum voltage (ADC counts) in bits 11-0, updated since VME reset or power up. This register will continue to be updated after LVPS limit fault detected. This register is cleared on power-up initialization.

PSD VCC In Min V

This diagnostic register captures the Vcc In minimum voltage (ADC counts) in bits 11 - 0, updated since VME reset or power up. This register will continue to be updated after LVPS limit fault detected. This register is cleared on power-up initialization.

PSD HVPS Error

This diagnostic register captures the error condition if the HVPS is outside the limits since VME reset or power up. Bits 15-14 indicate the error condition (0 - No error, 1 - NORM_TEST_ERR, 2 - HV_TEST_ERR). Bits 11-0 indicate the HVPS voltage (ADC counts). This register is cleared on power-up initialization.

PSD HV Bias Err Meas

Axis	VME (read)	P2 (read)
1	0x01C6	-
2	0x11C6	-
3	0x21C6	-
4	0x31C6	-

This diagnostic register captures the first Bias limit error. Bit 15 indicates the error condition (0 - no error, 1 - error). Bits 11-0 indicate the HV Bias Regulator Measured Bias voltage (ADC counts). This register is cleared on power-up initialization and Axis reset. Note: This register is axis specific.

PSD HV Bias Err Exp

Axis	VME (read)	P2 (read)
1	0x01C8	-
2	0x11C8	-
3	0x21C8	-
4	0x31C8	-

This diagnostic register captures the expected voltage associated with first Bias limit error. Bit 15 indicates the error condition (0 - no error, 1 - error). Bits 11-0 indicate the HV Bias Regulator Expected Bias voltage (ADC counts). This register is cleared on power-up initialization and Axis Reset. Note: This register is axis specific.

Quick Reset

Axis	MSB (read)	LSB (read)	Ext (read)
1	0x00D0	0x00D2	0X00D4
2	0x10D0	0x10D2	0X10D4
3	0x20D0	0x20D2	0X20D4
4	0x30D0	0x30D2	0X30D4

This is a VME diagnostic register that shows the contents of the quick reset register. This is a 37-bit register as described in the beginning of this chapter.

Reference ID

Axis	VME (read)	P2
3 only	0x20CA	-

This register contains the identification value received through the reference tree input connector. This function is described in Section 3-10.

Reference ID Register Functions

Bit	*Description*
9-0	*RID[9:0]* VME Base Address A(23:14) of the board supplying the reference signal.
10	*RID[10]* User P2d Out bit from axis 1 or 3 of the board supplying the reference signal.
11	*RID[11]* Reference Out identifier, 0 if from Reference Out 1, 1 if from Reference Out 2.
14-12	*Reserved*.
15	*RID Invalid*. This bit is set to one by powerup reset, error reset, or axis reset. When a valid ID is received, this bit is set to zero.

Sample Timer

Axis	VME (read/write)	P2 (read/write)
3 only	0x2038	0x9C

This register controls the period of the P2 external sample clock. The period of the timer is:

ST = Period/50 ns -1

Where ST is the value of the Sample Timer register (1 to 65535).

The SCLK Timer period is twice this calculated value if the *SCLK Divide by 2 Enable bit* in Control Register 16 is set.

SCLK Command

Axis	VME (write)	P2 (write)
3 only	0x2002	0x81

SCLK Command Register Functions

Bit	*Description*
0	*External Sample (SCLK0).* This outputs a sample pulse on the P2 bus SCLK0 signal. The P2 bus SCLK0 output must be enabled for this to function.
1	*External Sample (SCLK1).* This outputs a sample pulse on the P2 bus SCLK1 signal. The P2 bus SCLK1 output must be enabled for this to function.
15-2	*Reserved.*

Sig RMS L2

Axis	VME (read)	P2 (read)
1	0x0036	0x1B
2	0x1036	0x5B
3	0x2036	0x9B
4	0x3036	0xDB

This register provides the logarithm of the RMS value of the digitized measurement signal, after subtraction of any constant offset. The register value is calculated as follows:

$$Sig\_RMS\_L2 = Log2(Sig\_RMS)*1024$$

$$Sig\_RMS = 2^{(Sig\_RMS\_L2 / 1024)}$$

Sig RMS L2 Max

Axis	VME (read)	P2
1	0x0196	-
2	0x1196	-
3	0x2196	-
4	0x3196	-

This register provides the maximum value of the Sig RMS L2 register since the issue of a *Reset Sig RMS L2 Min/Max* command in the Test Command 0 register.

Sig RMS L2 Max Lim

Axis	VME (read/write)	P2
1	0x019A	-
2	0x119A	-
3	0x219A	-
4	0x319A	-

This register specifies the maximum acceptable Sig RMS L2 register value, a value greater than this will cause a *Sig RMS L2 Max* error and, depending on APD Control mode, adjust the APD gain. The value in this register only takes effect when processing a *Start Bias Calc* command from the P2 Command Register or the VME Command Register. The default value is 13,600.

Sig RMS L2 Min

Axis	VME (read)	P2
1	0x0194	-
2	0x1194	-
3	0x2194	-
4	0x3194	-

This register provides the minimum value of the Sig RMS L2 register since the issue of a *Reset Sig RMS L2 Min/Max* command in the Test Command 0 register.

Sig RMS L2 Min Lim

Axis	VME (read/write)	P2
1	0x0198	-
2	0x1198	-
3	0x2198	-
4	0x3198	-

This register specifies the minimum acceptable Sig RMS L2 register value, a value less than this will cause a *Sig RMS L2 Min* error and, depending on APD Control mode, adjust the APD gain. The value in this register only takes effect when processing a *Start Bias Calc* command from the P2 Command Register or the VME Command Register. The default value is 5,800 (to prevent nuisance trips in simultaneous low signal and low gain situations). However, actual Sig RMS L2 values must be above 8,000 for satisfactory operation. This register may be set to a higher value to generate an error whenever the input signal is lower than the expected value.

Software Detail

Axis	VME (read)	P2
1	0x0188	-
2	0x1188	-
3	0x2188	-
4	0x3188	-

This register provides detailed information on the revision level of the software in the microcontroller. This register contains two 4-bit fields and an 8-bit field representing a software revision indicator, for example 0x2312 is 2.3.18. Note that the software revision is independent of the firmware revision shown in the Firmware Revision register.

Software Error ID

Axis	VME (read)	P2
1	0x01BA	-
2	0x11BA	-
3	0x21BA	-
4	0x31BA	-

Software Error ID Register Functions

Bit	*Description*
0 - 11	*Software Error ID*. These bits define the Error ID.
12 - 15	*Software Error Type*. These bits define the Error Type. The Error Type can be any one of the following: Exception Error, Stack Overflow, Switch Default Error or Comm. Error.

Refer to section 3.8.10 APD Controller Software Errors, for a more detailed description of Software Error Types.

Software Revision

Axis	VME (read)	P2
1	0x0186	-
2	0x1186	-
3	0x2186	-
4	0x3186	-

This register provides revision level of the software in the microcontroller. This register contains two ASCII characters, for example “A”. For prototype and engineering use, this register contains a numeric value, for example “01”. Note that the software revision is independent of the firmware revision shown in the Firmware Revision register.

Software Version

Axis	VME (read)	P2
1	0x0184	-
2	0x1184	-
3	0x2184	-
4	0x3184	-

This register provides version of the software in the microcontroller. This register contains the software version expressed as four hexadecimal digits, for example SPM8020-9277-01 appears as 0x7701.

SSI Avg

Axis	VME (read)	P2 (read)
1	0x002A	0x15
2	0x102A	0x55
3	0x202A	0x95
4	0x302A	0xD5

This is the average value of the signal strength indicator (SSI). A value of 52832 (decimal) represents maximum signal level and 1.0 V output from the test point connection on the front panel. The maximum possible value of 65535 corresponds to a 1.25 V output from the test point connector. The EEPROM contains the actual measured SSI values for three optical power levels. The SSI value is very linear from zero power to the nominal value stored in EEPROM. The SSI value is nonlinear above the nominal value due to saturation of the electronics and the ADC. This value is updated asynchronously at a 10 kHz rate.

See Chapter 2 for more information.

SSI Avg Register Functions

Bit	*Description*
15-0	*SSI Average*

SSI DAC Test

Axis	VME (read/write)	P2
1	0x00C6	-
2	0x10C6	-
3	0x20C6	-
4	0x30C6	-

This register allows directly controlling the SSI DAC. This function is enabled by the *Enable SSI DAC Test Mode* bit in the Test Control 0 register. A value range of 0 to 4095 corresponds to an output of 0 to 1.25 V.

SSI Max

Axis	VME (read)	P2 (read)
1	0x002C	0x16
2	0x102C	0x56
3	0x202C	0x96
4	0x302C	0xD6

This monitors the maximum absolute value of the digitized input signal. This is important to be sure that the signal level is not close to saturating the ADC. A value of 2047 or 2048 indicates saturation. This value is reset by the reset *SSI Max* bit in the Test Command 0 register.

SSI Min

Axis	VME (read)	P2
1	0x00DC	-
2	0x10DC	-
3	0x20DC	-
4	0x30DC	-

This register records the minimum value of the SSI Average register since the most recent Axis Reset. This register is also reset by the Reset SSI Max/Min command in the Test Command 0 register.

SSI Offset

Axis	VME (read)	P2
1	0x00D6	-
2	0x10D6	-
3	0x20D6	-
4	0x30D6	-

This is a diagnostic register that measures the average DC offset of the digitized input signal. This register has a resolution of 1/3 LSB, or 162 µV referred to the 2V P-P input of the ADC. This is a signed value.

SSI Squelch

Axis	VME (read/write)	P2 (read/write)
1	0x0034	0x1A
2	0x1034	0x5A
3	0x2034	0x9A
4	0x3034	0xDA

This register allows setting the SSI level that controls the Measure Signal Present status. This affects the *Measure Signal Missing* bit in the VME Error Status and P2 Error Status registers; the *Measure Signal Present* bit in Status Register 1, and the Meas Pres LED on the front panel. The Measure Signal Present status turns on (‘1’) when the SSI Average is greater than or equal to the SSI_Squelch value, and turns off (‘0’) when the SSI Average is less than or equal to 0.875 times the SSI Squelch value. The power-up default value for this register is 128 to prevent nuisance trips during simultaneous low signal and low gain situations. However, actual SSI_Average values must be above 800 for satisfactory operation. This register may be set to a higher values to generate an error whenever the input signal is lower than the expected value.

SSI Squelch Register Functions

Bit	*Description*
11-0	*SSQ[11:0]*. SSI Squelch
15-12	*Reserved.*

Status Register 0

Axis	VME (read)	P2 (read)
1	0x0000	0x00
2	0x1000	0x40
3	0x2000	0x80
4	0x3000	0xC0

Status Register 0 Functions

Bit	*Description*
0	*Power OK*. All on-board analog power supplies (+10V, -12V, -5V) are operating properly. LED D10 on the measurement board also indicates this condition.
1	*Reference Signal Present.* The reference signal is present. This is true if either (but not both) the reference fiber signal or the electrical reference tree signal is present. If both references are present, the hardware will operate with the electrical reference tree signal, but an error will be indicated.
2	*Reference Tree Signal Present*. The electrical reference tree input is present.
3	*Reference Fiber Signal Present*. The optical reference fiber signal is present.
4	*Reference PLL Locked*. The PLL that generates the on-board system clock is operating properly.
5	*FPGA DLL Locked*. The master and slave FPGA on the ZMI 4104 are properly synchronized and the DLL in the FPGA is operating properly.
6	*Overtemp*. The FPGA temperature exceeds the preset limit (+85°C).
7	*APD Init Complete.* This indicates that the microcontroller and APD initialization and powerup testing is complete. Initiation of any axis reset will be delayed until after this condition occurs.
8	*VME IRQ Pending*. There is a VME interrupt being asserted on the VMEbus. This means that an error bit is asserted in the VME Error Status register and it is enabled by the corresponding bit in the VME Interrupt Enable register. If the *VME Interrupt Enable* bit in the VME Interrupt Enable register is set, the interrupt is asserted on the VMEbus.
9	*P2 INT Pending*. There is a P2 interrupt being asserted on the P2bus. This means that an error bit is asserted in the P2 Error Status register and it is enabled by the corresponding bit in the P2 Interrupt Enable register. If the *P2 Int Driver* bit in the Control Register 4 is set to drive the P2 interrupts, the interrupt is asserted.
10	*VME External Sample Flag*. The position data was latched by a SCLK sample input. This flag must be cleared, by writing to the *Clear VME External Sample Flag* bit in the VME Error Clear 1 register, then reading the position value.
11	*Reserved*.
15-12	*System Type*. These four bits specify the type of ZMI system. XX00 = ZMI 2000 series 1111 = ZMI 4004, ZMI 4002 0111 = ZMI 4104 1011 = ZMI 4104C

Status Register 1

Axis	VME (read)	P2 (read)
1	0x0002	0x01
2	0x1002	0x41
3	0x2002	0x81
4	0x3002	0xC1

Status Register 1 Functions

Bit	*Description*
0	*Reset Complete*. The position reset, or axis reset, or load position operation is complete. This bit goes low immediately following the reset, and returns high after the reset is complete. This time includes the delay specified by the *Reset Time* bits in Control Register 3.
1	*Measure Signal Present*. There is a measurement signal. The threshold for this indication is defined by the SSI Squelch register.
2	*Reserved*.
3	*Bias Calc Busy*. This indicates that the microcontroller is in the process of determining the APD bias voltage in response to a Start Bias Calc command from the P2 Command Register.
4	*Cmd Busy.* This indicates that the microcontroller is in the process of responding to a command.
8-5	*Reserved*.
9	*FIFO Overflow*. This bit indicates that the VME Position FIFO register was full (512 samples for the 4004 and 128 samples for the 4104) when another sample occurred. The samples in the register are valid.
10	*FIFO DAV (Data Available).* This bit indicates one or more position values are available to be read from the VME Position FIFO register.
13-11	*Config*. The value of these bits is defined by the board assembly configuration. See the following table.
14	*Comparator State (raw).* This indicates the state of the comparator before inversion by the *Compare Out Pol* bit in Control Register 2.
15	*User P2d In*. On all axes, this is the state of the User input on the P2d connector. This may be used for any purpose.

Table 4-20 Configuration Bits

Config 2-0	Board Type	Description
000	-	Reserved
001	-	Reserved
010	4104	Axes 1, 2, 3, and 4 populated
011	-	Reserved
100	-	Reserved
101	-	Reserved
110	-	Reserved
111	-	Reserved

Switches

Axis	VME (read)	P2
1	0x00CC	-
2	0x10CC	-
3	0x20CC	-
4	0x30CC	-

This is a diagnostic register that reads the state of the four rotary address switches (SW1-SW4).

Test Command 0

Axis	VME (write)	P2
1	0x00C0	-
2	0x10C0	-
3	0x20C0	-
4	0x30C0	-

Test Command 0 Register Functions

Bit	*Description*
0	*Reset Phase Noise Peak.* This resets the value accumulated in the Phase Noise Peak diagnostic register.
1	*Reset SSI Max/Min*. This resets the value accumulated in the SSI Max and SSI Min registers.
2	*Reset Sig RMS L2 Min/Max.* This command resets the Sig RMS L2 Min and Sig RMS L2 Max registers. The *Cmd Busy* bit in Status Register 1 is set immediately, and cleared when the registers have been reset.
3	*Reset Opt Power L2 Min/Max.* This command resets the Opt Power L2 Min and Opt Power L2 Max registers. The *Cmd Busy* bit in Status Register 1 is set immediately, and cleared when the registers have been reset.
15-4	*Reserved*.

Test Command 1

Axis	VME (write)	P2
1	0x00A0	-
3	0x20A0	-

Test Command 1 Register Functions

Bit	*Description*
0	*Send Ref ID*. This causes the hardware to send the reference ID through the reference output connectors. (axis 3 only)
1	*Clear Ref ID.* This resets the reference ID transmitter and receiver. (axis 3 only)
2	*Clear EEPROM Error*. Writing a '1' to this bit clears any error in the EEPROM control.
3	*Start Diag FFT Data.* Writing a '1' to this bit starts acquisition of data into the Diag FFT RAM Data memory. Acquisition will stop after 32768 data samples, or after writing a '1' to the *Stop Diag FFT Data* bit described below. *(*Not available in the 8020-9274-01 firmware)
4	*Stop Diag FFT Data.* Writing a '1' to this bit stops acquisition of data into the Diag FFT RAM Data memory. *(*Not in the 8020-9274-01 firmware)
14-5	*Reserved*.
15	*Reset Controller.* This command performs a hardware reset of the APD microcontroller (Axis 1 and 3 only). For a 4-axis board, axis 3 must be reset first, and axis 1 must be reset within 1 ms for proper operation. This is for factory use only.

Test Control 0

Axis	VME (read/write)	P2
1	0x00C2	-
2	0x10C2	-
3	0x20C2	-
4	0x30C2	-

Test Control 0 Register Functions

Bit	*Description*
0	*Meas Pres LED Test Mode*. This enables direct control of the Measure Present LED for test or other purposes.
1	*Meas Pres LED*. This controls the state of the Meas Pres LED when the *Meas Pres LED Test Mode* bit is set.
2	*Meas Err LED Test Mode.* This enables direct control of the Meas Error LED for test or other purposes.
3	*Meas Err LED*. This controls the state of the Meas Err LED when the *Meas Err LED Test Mode* bit is set.
4	*Create Test Signal.* This enables a simulated signal to be added to the digitized measurement signal. The simulated signal is added after the Diagnostic Data RAM and the Diagnostic FFT RAM, so it will not appear in that data. This signal is equivalent to a 1 μW fiber signal at 20 MHz, plus a 2 μW fiber signal at 10 MHz. This allows test operation without an optical signal in either of two modes: a. If the *Enable Reset Finds Velocity* bit in Control Register 3 is not set, the system will operate at simulated zero velocity after an axis reset. b. If the *Enable Reset Finds Velocity* bit in Control Register 3 is set, the system will operate at simulated high velocity (-1.6 m/s) after an axis reset. If a measurement signal is present, operation will depend on the mode and the relative signal levels. (See Appendix D line 18 for applicability.)
5	*Reserved.*
6	*Diagnostic Data Select.* When this bit is 1, the diagnostic data comes from the Preset Position register. When this bit is 0, diagnostic data comes from generated test data. Generation of test data is explained here. When the *Create Diag Data* bit of the Test Control 0 register is set, test data replaces the position data that is transmitted through all outputs. For 16 bit data, the test data consists of (from LSB to MSB) 6 bits time(5:0), 3 bits SCLK0 sample count, 2 bits axis number, 5 bits VME base address A19-A15. For 32 bit or 37 bit data, the second 16 bits of the test data consists of 10 bits time(9:0), 3 bits SCLK0 sample count, and 3 bits SCLK1 sample count. For 37 bit data, the upper five bits of the test data consists of a 2 bit axis number and a three bit SCLK0 sample count. The three bit sample counts are reset at the same time as the quick reset after an axis reset or position reset.
7	*Reserved.*
8	*Create Diag Data*. This enables diagnostic data to take the place of the position data for the P2, Serial, and High Speed Position outputs. This is used for verifying the proper operation of the data output circuitry. The type of data is determined by the *Diag Data Select* bit above.

Test Control 0 Register Functions (continued)

Bit	*Description*
9	*Diag Stop* 0=VME 1=P2. This determines which error register controls the diagnostic RAM data acquisition. When an error occurs in the specified error register, the diagnostic data acquisition stops.
10	*Diag RAM Stop on Error*. This configures the diagnostic RAM to stop acquiring data when an error occurs, as selected by the *Diag Stop* bit. See the procedure below.
11	*Disab Diag RAM*. This disables the diagnostic RAM data acquisition. The powerup default value is 1 (disabled).
12	*Comparator Test Mode*. This disables the comparator. If it is in hysteresis mode, the *Comparator Preset* bits in the Command Register may be used to toggle the output high or low.
13	*Enable SSI DAC Test Mode*. This enables the SSI DAC Test register to directly control the value output to the SSI DAC. This may be used for diagnostics or for outputting any value to the DAC.
14	*Disable Error Hold*. Normally, an error causes the position register to stop updating. This bit allows the registers to continue updating.
15	*Disable Excess Velocity*. This disables the normal excess velocity limit. A higher limit that will detect overflows will remain functional.

To use the stop on error function (bit 10), perform the following separate steps:

a) Set the *Disab Diag RAM* bit
b) Set the *Diag RAM Stop on Error* bit
   select the desired error register with the *Diag Stop* bit
c) Clear the *Disab Diag RAM* bit
d) After an error occurs, wait for the *Diag RAM Busy* bit in Test Status 0 register to be zero.
e) Read and process the Diag RAM Data starting at the address in the Diag RAM Start register.

Test Control 1

Axis	VME (read/write)	P2
1	0x00A2	-
3	0x20A2	-

Test Control 1 Register Functions

Bit	*Description*
4-0	*ADC Mux.* (Axis 1 and 3 only) This selects the desired measurement to be performed by the diagnostic ADC. The measurements that can be performed are listed under Diag ADC register. When this register is written, the ADC Busy bit in the Diag ADC register is 1 until the new data is in the Diag ADC register. The ADC Mux value is not the same as the ADC channel number. Channels 0-23 are located in axis 3. Channels 24-31 are located in axis 1. ADC Channel 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 ADC Mux 0 4 1 5 2 6 3 7 8 12 9 13 10 14 11 15 ADC Channel 16 17 18 19 20 21 22 23 24 25 26 27 27 29 30 31 ADC Mux 16 20 17 21 18 22 19 23 0 4 1 5 2 6 3 7
7-5	*Reserved.*
8	*Ref LED Test Mode*. This enables direct control of the Ref Present and Ref Error LEDs for test or other purposes.
9	*Ref Pres LED*. This controls the state of the Ref Pres LED when the *Ref LED Test Mode* bit is set. (Axis 3 only)
10	*Ref Err LED.* This controls the state of the Ref Err LED when the *Ref LED Test Mode* bit is set. (Ref Err LED is Logical OR of Axis 1 and Axis 3 Ref Error LED outputs.)
11	*Reserved.*
12	*Config 10m*. For ZYGO use only. (See Appendix D line 19 for applicability.)
13	*Bias Supply Override.* This enables the *Bias Supply Test* and *Bias Supply Enable* bits in the Test Control 1 register to control the bias supply instead of the internal microcontroller. This is for diagnostic purposes only. (Axis 3 only)
14	*Bias Supply Test.* This selects a higher voltage for the APD bias supply. This is for diagnostic purposes only, and is effective only when the *Bias Supply Override* bit is set. (Axis 3 only)
15	*Bias Supply Enable.* This enables the APD bias supply. This is for diagnostic purposes only, and is effective only when the *Bias Supply Override* bit is set. (Axis 3 only)

Test Status 0

Axis	VME (read)	P2
1	0x00C0	-
2	0x10C0	-
3	0x20C0	-
4	0x30C0	-

Test Status 0 Register Functions

Bit	*Description*
5-0	*GAP, GA[4:0].* This allows directly reading the VME64x geographic address. This may be hard-wired on the backplane as specified by VME64x specification, section 3.2.3. Note that these bits are negated relative to the values on the backplane.
7-6	*Reserved.*
8	*Diag RAM Busy.* This indicates that the diagnostic RAM is acquiring raw measurement data.
9	*Reserved.*
13-10	*Measure State.* This provides information indicating the state of the measurement control subsystem. This is for factory use only.
15-14	*SW5-2, SW5-1*. This allows directly reading the state of the two on-board configuration switches.

Test Status 1

Axis	VME (read)	P2
1	0x00A0	-
3	0x20A0	-

Test Status 1 Register Functions

Bit	*Description*
3-0	*SCLK0 Input Time*. This is used to verify the input timing of the SCLK0 signal. Typical values are shown in Table 3-14.
7-4	*SCLK1 Input Time*. This is used to verify the input timing of the SCLK1 signal. Typical values are shown in Table 3-14.
8	*A_PS_OK*. The +10V, -5V, and –12V analog power supplies are within tolerance.
9	*EEPROM Busy*. This indicates that the EEPROM is busy performing an operation. (Axis 3 only)
10	*Diag FFT Data Busy.* This bit indicates that the Diag FFT Ram is busy acquiring data. When busy, an attempt to read data will return invalid data. *(*Not in the 8020-9274-01 firmware)
11	*EEPROM Error*. This indicates that an EEPROM operation had an error.
15-12	*Reserved.*

Test Status 2

Axis	VME (read)	P2
1	0x00B6	-
2	-	-
3	0x20B6	-
4	-	-

Test Status 2 Register Functions

Bit	*Description*
0	*LVPS Ok.* This indicates that the voltages of the +15 V, -15 V, +10 V, -12 V, and -5 V power supplies are within normal operating range. These supplies are not required for communication with the ZMI 4100, but they are required for measurements.
1	*HVPS Ok.* This indicates that the voltage of the APD bias supply is within normal operating range.
2-13	*Reserved*
14	*Bias Supply Test.* This indicates that the APD bias supply is selected to have a higher voltage for diagnostic purposes.
15	*Bias Supply Enable.* This indicates that the APD bias supply is enabled.

User Excess Velocity

Axis	VME (read/write)	P2 (read/write)
1	0x0032	0x19
2	0x1032	0x59
3	0x2032	0x99
4	0x3032	0xD9

This sets the velocity limit for the User Excess Velocity error. If the absolute value of the most significant 16 bits of the velocity register exceeds the 16 bit value stored in this register, then the *User Excess Velocity Error* bit is set. The resolution of this register is 193 µm/sec for a single-pass interferometer, or 96.5 µm/sec for a double-pass interferometer. The default value for this register is 65535 (0xFFFF), which results in no limit checking.

VME Absolute Phase

Axis	VME (read)	P2
1	0x0028	-
2	0x1028	-
3	0x2028	-
4	0x3028	-

This register provides an absolute measure of the phase of the measurement signal. This is used for data age calibration. The filtering for this measurement is identical to the filtering for the position measurement. The phase is a 13-bit value, which provides resolution of λ/8192, or 8 times finer than the position measurement. This is equivalent to 6.1 ps when measuring the 20 MHz reference. This is sampled simultaneously with either the VME Position register or the VME Sample Position register.

VME Command

Axis	VME (write)	P2
1	0x0000	-
2	0x1000	-
3	0x2000	-
4	0x3000	-

VME Command Register Functions

Bit	*Description*
0	*Reset VME Errors*. This resets all errors in the VME Error Status registers.
1	*Reset P2 Errors*. This resets all errors in the P2 Error Status registers.
2	*Reset Position*. This resets or presets the position measurement. Position reset resets the measurement function, but does not reset errors. If the *Preset Enable* bit in Control Register 3 is set, the value in the Preset Position register is preset into the position measurement. The reset or preset value is before the Offset register is subtracted.
3	*Reset Time*. This resets the time register.
4	*Reset Position Quick*. This performs a quick reset or preset of the position register.
5	*Reset Axis*. An axis reset resets the measurement function and all errors.
6	*Start Bias Calc*. This command starts the process to determine the APD bias voltage. The *Cmd Busy* bit in Status Register 1 is set immediately. When the command is recognized by the controller, the *Bias Calc Busy* bit in Status Register 1 is set, and the *Cmd Busy* bit is cleared. When the process is complete, the *Bias Calc Busy* bit is cleared and the *Bias Calc Complete* bits in P2 Error Status 2 and VME Error Status 2 registers are set. When the *Cmd Busy* bit or *Bias Calc Busy* bit is set, write operations to Control Register 5 or to APD control registers (VME offsets 0x180 to 0x1FE) are inhibited, and will produce a *Write Protect Error* in P2 Error Status 2 and VME Error Status 2 registers.
7	*Reserved*.
8	*FIFO Clear*. This bit clears the VME Position FIFO register and the *FIFO DAV* and *FIFO Overflow* flags in Status Register 1.
9	*Sample VME Position*.
10	*Comparator Preset 0*. This presets the comparator hysteresis to zero.
11	*Comparator Preset 1*. This presets the comparator hysteresis to one.
12	*Load Position.* This presets the position to the value in the Preset Position register. Load position only loads a new position value, it assumes that a valid position measurement exists.
15-13	*Reserved*.

VME Error Clear

	Error Clear0		Error Clear1		Error Clear 2
Axis	VME (write)	P2	VME (write)	P2	VME (write)
1	0x0008	-	0x000A	-	0x001E
2	0x1008	-	0x100A	-	0x101E
3	0x2008	-	0x200A	-	0x201E
4	0x3008	-	0x300A	-	0x301E

Writing a one to a bit in this register clears the corresponding bit in the VME Error Status register. If the error condition is still present, the error bit will be immediately set again.

For bit descriptions, refer to Section 4.2.

VME Error Status

Axis	Error Status0 VME (read)	Error Status0 P2	Error Status1 VME (read)	Error Status1 P2	Error Status 2 VME (read)
1	0x0008	-	0x000A	-	0x001E
2	0x1008	-	0x100A	-	0x101E
3	0x2008	-	0x200A	-	0x201E
4	0x3008	-	0x300A	-	0x301E

The bits in this register are set by error conditions, and cleared by writing a one to the corresponding bit in the VME Error Clear register, or by a reset operation.

For bit descriptions, refer to Section 4.2.

VME Interrupt Enable

Axis	Interrupt Enable0 VME (read/write)	Interrupt Enable0 P2	Interrupt Enable1 VME (read/write)	Interrupt Enable1 P2	Interrupt Enable 2 VME (read/write)
1	0x0004	-	0x0006	-	0x001C
2	0x1004	-	0x1006	-	0x101C
3	0x2004	-	0x2006	-	0x201C
4	0x3004	-	0x3006	-	0x301C

The bits in this register enable a VME interrupt when a corresponding error occurs in the VME Error Status register.

For bit descriptions, refer to Section 4.2.

VME Interrupt Vector

Axis	VME (read/write)	P2
1 (2)	0x00B2	-
3 (4)	0x20B2	-

Axis 1 and 2 share a VME interrupt level and interrupt vector. Axis 3 and Axis 4 share a VME interrupt level and interrupt vector.

VME Interrupt Vector Register Functions

Bit	*Description*
7-0	*VME Interrupt Vector*. VIV[7:0]
10-8	*VME Interrupt Level*. VIL[2:0]
15-11	*Reserved*.

VME Position

Axis	MSB (read)	LSB (read))	Ext (read)	Errs (read)
1	0x0040	0x0042	0x0044	0x0046
2	0x1040	0x1042	0x1044	0x1046
3	0x2040	0x2042	0x2044	0x2046
4	0x3040	0x3042	0x3044	0x3046

This contains the position data after sampling by the *Sample VME Position* VME Command, or by the SCLK signal selected by the *SCLK VME Sample In* bit in Control Register 2. This is a 37-bit register as described in Section 4.2. The VME Position register supports byte (8-bit) access to the extension portion.

VME Position FIFO

Axis	VME (write)	P2
1	0x0080	-
2	0x1080	-
3	0x2080	-
4	0x3080	-

This register reads data from a 128 word (ZMI 4100) or 512 word (ZMI 4000) FIFO (First In First Out) register that is loaded by SCLK sampling or the *VME Sample* Command. The FIFO allows faster VME data acquisition when using a computer that may be interrupted to do other tasks. The SCLK0/1 selection and the bit window selection are the same as for the VME Position register. The FIFO is cleared by an axis reset, or by the *FIFO Clear* bit in the VME Command register. The FIFO status is indicated by the *FIFO DAV* (Data Available) and *FIFO Overflow* bits in Status Register 1.

To use the VME Position FIFO:

1. Disable the SCLK timer by writing a 0 to the *SCLK Timer Enable* bit in Control Register 16 of the axis driving SCLK.
2. Reset all axes and wait for reset complete.
3. Enable the SCLK timer by writing a 1 to the *SCLK Timer Enable* bit in Control Register 16 of the axis driving SCLK**.** The SCLK enable after axis reset is required so that the first sample of all axes occurs at the same time. Otherwise, some axes may miss the first sample.
4. Poll the *FIFO DAV* bit in Status Register 1 of any axis until the *FIFO DAV* bit is set. It may safely be assumed that all axes have data available when any one *FIFO DAV* bit is set. The sampling delay between axes (< 50 ns) is much less than the time to read a VME register (> 500 ns). Optionally, the *FIFO Overflow* bit may be checked here if the Status Register 1 value used corresponds to the last axis read in step 5.
5. Read and save one value from the VME Position FIFO register of all axes.
6. Repeat steps 4 and 5 until the desired number of samples has been acquired.
7. Disable the SCLK timer by writing a 0 to the *SCLK Timer Enable* bit in Control Register 16 of the axis driving SCLK.
8. Verify that the *FIFO Overflow* bit in Status Register 1 is not set. This should be checked on all axes, although checking only on the last axis read in Step 5 may be sufficient. A FIFO overflow indicates that some data samples have been missed. Either the sample rate must be decreased, or the processing speed must be increased.

VME Sample Position

Axis	MSB (read)	LSB (read))	Ext (read)	Errs (read)
1	0x0048	0x004A	0x004C	0x004E
2	0x1048	0x104A	0x104C	0x104E
3	0x2048	0x204A	0x204C	0x204E
4	0x3048	0x304A	0x304C	0x304E

A read of this register samples the position, then reads the data. The latching occurs when the MSB is read by either a 16-bit or 32-bit read. The remaining bits may be read in any order after the latching. The VME Sample Position register supports byte (8-bit) access to the extension portion.

VME Time

Axis	MSB (read)	LSB (read))
1	0x0054	0x0056
2	0x1054	0x1056
3	0x2054	0x2056
4	0x3054	0x3056

This contains the time value. This is sampled simultaneously with either the VME Sample Position register or the VME Position register. The time units are 25 ns, for a maximum positive 32-bit time value of 107 seconds.

VME Velocity

Axis	MSB (read)	LSB (read))
1	0x0050	0x0052
2	0x1050	0x1052
3	0x2050	0x2052
4	0x3050	0x3052

This contains the velocity value. This is sampled simultaneously with either the VME Sample Position register or the VME Position register.

Appendix A Register Map (Numerical)

ZMI 4100 Series Measurement Board Register Map

The table in this appendix is a summary of the offset address locations of the registers, and the function for each register bit, for the ZMI 4100 Measurement Boards. This table is a useful reference when programming the board for use in the VME backplane.

Notes on the Table

Shaded areas indicate the register is not available.

Notes for R/W column:

R	Read Only
W	Write only
RW	Write with Readback at same address

Notes for bit definitions: All unused bits are reserved for future use, and should not be used for other purposes. If written, the bit should be set to zero.

#	Bit reserved for future use, may be written and read back.
0	Bit reserved for future use, will always read as zero.
X	Bit reserved for future use, readback data is undefined.
?	Bit undefined and may read as a 0 or a 1.
‡	Register or bit exists in axis 3 only.
§	Register bit exists in axis 1 and 3 only.
◊	Bit can only be written by VME.

Several registers are indicated as "Axis 1 *and* 3 only." These registers also control the next higher axis; axis 1 controls axis 2, and axis 3 controls axis 4.

Writing to a register that does not exist will produce no error and will have no effect. Reading from a register that does not exist will produce no error and will return undefined data.

The P2 interface is 32 bits only. A P2 read or write operates on a register with an even address and the register with the next higher (odd) address. For example, address offset 0x08 reads or writes Control Register 0 (data bits 31-16) and Control Register 1 (data bits 15-0).

intentionally left blank

P2	VME	R/W	DESCRIPTION	Byte 2 (VME A1 = 1)								Byte 3 (VME A1 = 1)							
OFFSET	OFFSET			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				Byte 0 (VME A1 = 0)								Byte 1 (VME A1 = 0)							
				D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
00	00	R	Status Register 0	System Type SY3	System Type SY2	System Type SY1	System Type SY0	0	VME External Sample Flag	P2 INT Pending	VME IRQ Pending	APD Init Complete	Overtemp	FPGA DLL Locked	Reference PLL Locked	Reference Fiber Signal Present	Reference Tree Signal Present	Reference Signal Present	Power OK
	00	W	VME Command Register	X	X	X	Load Position	Compar-ator Preset 1	Compar-ator Preset 0	Sample VME Position	FIFO Clear	X	Start Bias Calc	Reset Axis	Reset Position Quick	Reset Time	Reset Position	Reset P2 Errors	Reset VME Errors
00		W	P2 Command Register	X	X	X	Load Position	Compar-ator Preset 1	Compar-ator Preset 0	Reserved	X	X	Start Bias Calc	Reset Axis	Reset Position Quick	Reset Time	Reset Position	Reset P2 Errors	Reset VME Errors
01	02	R	Status Register 1	User P2d In	Comparat or State (raw)	Config 2	Config 1	Config 0	FIFO DAV	FIFO Overflow	0	0	0	0	Cmd Busy	Bias Calc Busy	Reserved	Measure Signal Present	Reset Complete
01	02	W	SCLK Command Register (Axis ‡ only)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	External Sample (SCLK1)	External Sample (SCLK0)
	04	RW	VME Interrupt Enable 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
	06	RW	VME Interrupt Enable 1	VME Interrupt Enable	#	#	#	#	#	Reserved	VME External Sample (SCLK)	#	#	Compare	P2 32 bit Position Overflow	VME 32 bit Position Overflow	37 bit Position Overflow	User Velocity Error	Velocity Error
	08	R	VME Error Status 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
	08	W	VME Error Clear 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
	0A	R	VME Error Status 1	0	0	0	0	0	0	Reserved	VME External Sample (SCLK)	0	0	Compare	P2 32 bit Position Overflow	VME 32 bit Position Overflow	37 bit Position Overflow	User Velocity Error	Velocity Error
	0A	W	VME Error Clear 1	X	X	X	X	X	X	Reserved	VME External Sample (SCLK)	X	X	Compare	P2 32 bit Position Overflow	VME 32 bit Position Overflow	37 bit Position Overflow	User Velocity Error	Velocity Error
02-05		RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
06	0C	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
07	0E	R	Firmware Version	Firmware Version FV15	Firmware Version FV14	Firmware Version FV13	Firmware Version FV12	Firmware Version FV11	Firmware Version FV10	Firmware Version FV9	Firmware Version FV8	Firmware Version FV7	Firmware Version FV6	Firmware Version FV5	Firmware Version FV4	Firmware Version FV3	Firmware Version FV2	Firmware Version FV1	Firmware Version FV0
07	0E	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
08	10	RW	Control Register 0	#	#	#	#	#	#	#	#	Position Direction	Sign Extension	Error Output Source 0=VME 1=P2	Error LED Source 0=VME 1=P2	#	#	Enable Data Age Velocity Comp	#
09	12	RW	Control Register 1 (Filters)	#	#	#	Disable Quick Reset	Glitch Filter GF3	Glitch Filter GF2	Glitch Filter GF1	Glitch Filter GF0	#	Filter KP2	Filter KP1	Filter KP0	#	Filter KV2	Filter KV1	Filter KV0
0A	14	RW	Control Register 2	#	RFV Mode	VME Hold Sample Enable	SCLK VME Sample In 0=SCLK0 1=SCLK1	VME Enable 32-bit Overflow	#	Aux Register Enable	Serial Data Enable	VME Bit Window VBW2	VME Bit Window VBW1	VME Bit Window VBW0	SSI DAC x16	Compare Out Enable	Compare Out Pol	Compare Interrupt Pol	Compare Mode
0B	16	RW	Control Register 3 (Init)	#	Reset Time RT2	Reset Time RT1	Reset Time RT0	Enable Reset Finds Velocity	SCLK Reset Select 0=SCLK0 1=SCLK1	SCLK Reset Enable	Preset Enable	Reset Mode RM1	Reset Mode RM0	P2d ResetAll 1=p2reset 0=p2dreset	P2d RESET Quick Reset Enable	P2d RESET Time Reset Enable	P2d RESET Position Reset Enable	P2d RESET P2 Error Reset Enable	P2d RESET VME Error Reset Enable
0C	18	RW	Control Register 4 (P2)	#	#	P2 Latch Mode 1=Pos Read 0=SCLK	SCLK P2 Sample In 0=SCLK0 1=SCLK1	P2 Enable 32-bit Overflow	P2 Int Driver PID0	P2 Int Level PIL1	P2 Int Level PIL0	P2 Bit Window PBW2	P2 Bit Window PBW1	P2 Bit Window PBW0	P2 RESET Quick Reset Enable	P2 RESET Time Reset Enable	P2 RESET Position Reset Enable	P2 RESET P2 Error Reset Enable	P2 RESET VME Error Reset Enable
0D	1A	RW	Control Register 5 (APD)	#	#	#	#	#	#	#	SSI DAC Mode	#	Disab Auto Gain Reduction	Gain Control AGC	Gain Control Min	Gain Control Max	Bias Control Mode BCM2	Bias Control Mode BCM1	Bias Control Mode BCM0
	1C	RW	VME Interrupt Enable 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	#	#	#	#	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	Bias Set Error	APD Fail Error	APD Temp Error
	1E	R	VME Error Status 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	0	0	0	0	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
	1E	W	VME Error Clear 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	X	X	X	X	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
0E		RW	P2 Interrupt Enable 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	#	#	#	#	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
0F		R	P2 Error Status 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	0	0	0	0	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
0F		W	P2 Error Clear 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	X	X	X	X	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
10	20	RW	P2 Interrupt Enable 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
11	22	RW	P2 Interrupt Enable 1	#	#	#	#	#	#	P2 Ext. Sample (SCLK)	Reserved	#	#	Compare	P2 32 bit Position Overflow	Reserved	37 bit Position Overflow	User Velocity Error	Velocity Error

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12	24	R	P2 Error Status 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
12	24	W	P2 Error Clear 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
13	26	R	P2 Error Status 1	0	0	0	0	0	0	P2 Ext. Sample (SCLK)	Reserved	0	0	Compare	P2 32 bit Position Overflow	Reserved	37 bit Position Overflow	User Velocity Error	Velocity Error
13	26	W	P2 Error Clear 1	X	X	X	X	X	X	P2 Ext. Sample (SCLK)	Reserved	X	X	Compare	P2 32 bit Position Overflow	Reserved	37 bit Position Overflow	User Velocity Error	Velocity Error
14		R	P2 Absolute Phase	0	0	0	AP12	AP11	AP10	AP9	AP8	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
	28	R	VME Absolute Phase	0	0	0	AP12	AP11	AP10	AP9	AP8	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
15	2A	R	SSI Avg	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
16	2C	R	SSI Max	0	0	0	0	SSM11	SSM10	SSM9	SSM8	SSM7	SSM6	SSM5	SSM4	SSM3	SSM2	SSM1	SSM0
14-16	28-2C	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
17	2E	RW	Phase Noise Limit	#	#	#	#	#	PNL10	PNL9	PNL8	PNL7	PNL6	PNL5	PNL4	PNL3	PNL2	PNL1	PNL0
18	30	RW	Data Age Adjust	DAA15	DAA14	DAA13	DAA12	DAA11	DAA10	DAA9	DAA8	DAA7	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0
19	32	RW	User Excess Velocity	UEV15 (1)	UEV14 (1)	UEV13 (1)	UEV12 (1)	UEV11 (1)	UEV10 (1)	UEV9 (1)	UEV8 (1)	UEV7 (1)	UEV6 (1)	UEV5 (1)	UEV4 (1)	UEV3 (1)	UEV2 (1)	UEV1 (1)	UEV0 (1)
1A	34	RW	SSI Squelch	#	#	#	#	SSQ11	SSQ10	SSQ9	SSQ8	SSQ7	SSQ6	SSQ5	SSQ4	SSQ3	SSQ2	SSQ1	SSQ0
1B	36	R	Sig RMS L2	SRMS15	SRMS14	SRMS13	SRMS12	SRMS11	SRMS10	SRMS9	SRMS8	SRMS7	SRMS6	SRMS5	SRMS4	SRMS3	SRMS2	SRMS1	SRMS0
1C	38	RW	Sample Timer (Axis ‡ only)	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
1D	3A	RW	Control Register 15 (Axis 1 and 3 only)	SCLK1 In Polarity	SCLK0 In Polarity	Reserved	Reserved	#	#	#	#	SCLK Divider SDV3 ‡	SCLK Divider SDV2 ‡	SCLK Divider SDV1 ‡	SCLK Divider SDV0 ‡	Serial Data Size 0=32 1=37	Serial Output Enable P2z ‡	Serial Output Enable P2d ‡	SCLK Serial Sample In 0=SCLK0 1=SCLK1
1E	3C	RW	Control Register 16 (Axis 1 and 3 only)	SCLK0 Delay SD01	SCLK0 Delay SD00	SCLK0 Sample Time SST03	SCLK0 Sample Time SST02	SCLK0 Sample Time SST01	SCLK0 Sample Time SST00	SCLK0 Out Enable ‡	SCLK Timer Drive ‡ 0=SCLK0 1=SCLK1	SCLK Timer Enable ‡	SCLK Divider Enable ‡	SCLK Divide by 2 Enable ‡	Trigger Delay Enable	#	Disable VME SYS-RESET* input.	User LED ‡	User P2d Out ‡
1F	3E	RW	Control Register 17 (Axis 1 and 3 only)	SCLK1 Delay SD11	SCLK1 Delay SD10	SCLK1 Sample Time SST13	SCLK1 Sample Time SST12	SCLK1 Sample Time SST11	SCLK1 Sample Time SST10	SCLK1 Out Enable ‡	SCLK2 Resync Drive ‡ 0=SCLK0 1=SCLK1	SCLK2 Resync Mode SRM1 ‡	SCLK2 Resync Mode SRM0 ‡	P2 IO Enable ◊	#	P2 Address P2A11 ◊	P2 Address P2A10 ◊	P2 Address P2A9 ◊	P2 Address P2A8 ◊
	40	R	VME Position MSB	VP31	VP30	VP29	VP28	VP27	VP26	VP25	VP24	VP23	VP22	VP21	VP20	VP19	VP18	VP17	VP16
	42	R	VME Position LSB	VP15	VP14	VP13	VP12	VP11	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
	44	R	VME Position Ext	0	0	0	0	0	VP1F	VP2F	VP3F	VP36	VP36	VP36	VP36	VP35	VP34	VP33	VP32
	46	R	VME Position Errs	0	0	0	0	0	0	0	0	0	User P2d Out	User P2d In	Comparat or state	Meas Error	Meas Present	Ref Error	Ref Present

APPENDIX A - ZMI 4100 SERIES MEASUREMENT BOARD REGISTER MAP (NUMERICAL)

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
20		R	P2 Position MSB	PP31	PP30	PP29	PP28	PP27	PP26	PP25	PP24	PP23	PP22	PP21	PP20	PP19	PP18	PP17	PP16
21		R	P2 Position LSB	PP15	PP14	PP13	PP12	PP11	PP10	PP9	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
22		R	P2 Position Ext	0	0	0	0	0	PP1F	PP2F	PP3F	PP36	PP36	PP36	PP36	PP35	PP34	PP33	PP32
23		R	P2 Position Errs	0	0	0	0	0	0	0	0	0	User P2d Out ‡	User P2d In	Comparat or state	Meas Error	Meas Present	Ref Error	Ref Present
24-27		R	Reserved	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
	48	R	VME Sample Position MSB	VSP31	VSP30	VSP29	VSP28	VSP27	VSP26	VSP25	VSP24	VSP23	VSP22	VSP21	VSP20	VSP19	VSP18	VSP17	VSP16
	4A	R	VME Sample Position LSB	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0
	4C	R	VME Sample Position Ext	0	0	0	0	0	VSP1F	VSP2F	VSP3F	VSP36	VSP36	VSP36	VSP36	VSP35	VSP34	VSP33	VSP32
	4E	R	VME Sample Position Errs	0	0	0	0	0	0	0	0	0	User P2d Out ‡	User P2d In	Comparat or state	Meas Error	Meas Present	Ref Error	Ref Present
	50	R	VME Velocity MSB	VV31	VV30	VV29	VV28	VV27	VV26	VV25	VV24	VV23	VV22	VV21	VV20	VV19	VV18	VV17	VV16
	52	R	VME Velocity LSB	VV15	VV14	VV13	VV12	VV11	VV10	VV9	VV8	VV7	VV6	VV5	VV4	VV3	VV2	VV1	VV0
	54	R	VME Time MSB	VT31	VT30	VT29	VT28	VT27	VT26	VT25	VT24	VT23	VT22	VT21	VT20	VT19	VT18	VT17	VT16
	56	R	VME Time LSB	VT15	VT14	VT13	VT12	VT11	VT10	VT9	VT8	VT7	VT6	VT5	VT4	VT3	VT2	VT1	VT0
28		R	P2 Velocity MSB	PV31	PV30	PV29	PV28	PV27	PV26	PV25	PV24	PV23	PV22	PV21	PV20	PV19	PV18	PV17	PV16
29		R	P2 Velocity LSB	PV15	PV14	PV13	PV12	PV11	PV10	PV9	PV8	PV7	PV6	PV5	PV4	PV3	PV2	PV1	PV0
2A		R	P2 Time MSB	PT31	PT30	PT29	PT28	PT27	PT26	PT25	PT24	PT23	PT22	PT21	PT20	PT19	PT18	PT17	PT16
2B		R	P2 Time LSB	PT15	PT14	PT13	PT12	PT11	PT10	PT9	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0
20-2B	40-56	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
2C-2F	58-5E	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
30	60	RW	Preset Pos MSB	PR31	PR30	PR29	PR28	PR27	PR26	PR25	PR24	PR23	PR22	PR21	PR20	PR19	PR18	PR17	PR16
31	62	RW	Preset Pos LSB	PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
32	64	RW	Preset Pos Ext	#	#	#	#	#	PR1F	PR2F	PR3F	#	#	#	PR36	PR35	PR34	PR33	PR32
33	66	R	Reserved	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
34	68	RW	Offset MSB	O31	O30	O29	O28	O27	O26	O25	O24	O23	O22	O21	O20	O19	O18	O17	O16
35	6A	RW	Offset LSB	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
36	6C	RW	Offset Ext	#	#	#	#	#	O1F	O2F	O3F	#	#	#	O36	O35	O34	O33	O32
37	6E	R	Reserved	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
38	70	RW	Compare A MSB	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
39	72	RW	Compare A LSB	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
3A	74	RW	Compare A Ext	#	#	#	#	#	#	#	#	#	#	#	CA36	CA35	CA34	CA33	CA32
3B	76	R	Reserved	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
3C	78	RW	Compare B MSB	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
3D	7A	RW	Compare B LSB	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
3E	7C	RW	Compare B Ext	#	#	#	#	#	#	#	#	#	#	#	CB36	CB35	CB34	CB33	CB32
3F	7E	R	Reserved	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	80	R	VME Position FIFO MSB	VPF31	VPF30	VPF29	VPF28	VPF27	VPF26	VPF25	VPF24	VPF23	VPF22	VPF21	VPF20	VPF19	VPF18	VPF17	VPF16
	82	R	VME Position FIFO LSB	VPF15	VPF14	VPF13	VPF12	VPF11	VPF10	VPF9	VPF8	VPF7	VPF6	VPF5	VPF4	VPF3	VPF2	VPF1	VPF0
	80-82	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	84-9E	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	A0	R	Test Status 1 (Axis 1 and 3 only)	0	0	0	0	EEPROM Error	Diag FFT Data Busy	EEPROM Busy ‡	A_PS_OK	SCLK1 Input Time SIT13	SCLK1 Input Time SIT12	SCLK1 Input Time SIT11	SCLK1 Input Time SIT10	SCLK0 Input Time SIT03	SCLK0 Input Time SIT02	SCLK0 Input Time SIT01	SCLK0 Input Time SIT00
	A0	W	Test Command 1 (Axis 1 and 3 only)	Reset controller ‡	X	X	X	X	X	X	X	X	X	X	Stop Diag FFT Data	Start Diag FFT Data	Clear EEPROM Error	Clear Ref ID ‡	Send Ref ID ‡
	A2	RW	Test Control 1 (Axis 1 and 3 only)	Bias Supply Enab ‡	Bias Supply Test ‡	Bias Supply Override ‡	Config 10m	#	Ref Err LED	Ref Pres LED ‡	Ref LED Test Mode	#	#	#	ADC Mux AM4 §	ADC Mux AM3 §	ADC Mux AM2 §	ADC Mux AM1 §	ADC Mux AM0 §
	A4	RW	Diag Temp Monitor Control (Axis 1 and 3 only)	DTSR (0)	DTA6 (0)	DTA5 (1)	DTA4 (0)	DTA3 (1)	DTA2 (0)	DTA1 (1)	DTA0 (0)	DTC7 (0)	DTC6 (0)	DTC5 (0)	DTC4 (0)	DTC3 (1)	DTC2 (1)	DTC1 (0)	DTC0 (1)
	A6	RW	Diag Temp Monitor Write (Axis 1 and 3 only)	# (0)	# (0)	# (0)	# (0)	# (0)	# (0)	# (0)	# (0)	DTW7 (0)	DTW6 (1)	DTW5 (0)	DTW4 (1)	DTW3 (0)	DTW2 (1)	DTW1 (0)	DTW0 (1)
	A8	R	Diag Temp Monitor Read (Axis 1 and 3 only)	Diag Temp Mon Busy	0	0	0	0	0	0	0	DTR7	DTR6	DTR5	DTR4	DTR3	DTR2	DTR1	DTR0
	AA	R	Diag ADC (Axis 1 and 3 only)	ADC Busy	0	0	0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	A8-AA	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	AC	RW	EEPROM Control (Axis ‡ only)	#	#	EEOP1	EEOP0	#	#	EEA9	EEA8	EEA7	EEA6	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
	AE	RW	EEPROM Write (Axis ‡ only)	EEW15	EEW14	EEW13	EEW12	EEW11	EEW10	EEW9	EEW8	EEW7	EEW6	EEW5	EEW4	EEW3	EEW2	EEW1	EEW0
	B0	R	EEPROM Read (Axis ‡ only)	EER15	EER14	EER13	EER12	EER11	EER10	EER9	EER8	EER7	EER6	EER5	EER4	EER3	EER2	EER1	EER0
	B0	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	B2	RW	VME Interrupt Vector (Axis 1 and 3 only)	X	#	#	#	#	VME Interrupt Level VIL2	VME Interrupt Level VIL1	VME Interrupt Level VIL0	VME Interrupt Vector VIV7	VME Interrupt Vector VIV6	VME Interrupt Vector VIV5	VME Interrupt Vector VIV4	VME Interrupt Vector VIV3	VME Interrupt Vector VIV2	VME Interrupt Vector VIV1	VME Interrupt Vector VIV0
	B4	RW	Diag FFT Control (axis 1 and 3 only)	Data Source DFS3	Data Source DFS2	Data Source DFS1	Data Source DFS0	#	Start on Input	Start on Compare	Data Write Select	#	#	DRP5	DRP4	DRP3	DRP2	DRP1	DRP0
	B6	R	Test Status 2 (Axis 1 and 3 only)	Bias Supply Enable	Bias Supply Test	0	0	0	**0**	0	0	0	0	0	0	0	0	HVPS Ok	LVPS Ok
	B6-BE	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	C0	R	Test Status 0	SW5-2	SW5-1	Meas State 3	Meas State 2	Meas State1	Meas State 0	0	Diag RAM busy	0	0	VME GAP	VME GA4	VME GA3	VME GA2	VME GA1	VME GA0
	C0	W	Test Command 0	X	X	X	X	X	X	X	X	X	X	X	X	Reset Opt Power L2 Min/Max	Reset Sig RMS L2 Min/Max	Reset SSI Max/Min	Reset Phase Noise Peak
	C2	RW	Test Control 0	Disable Excess Velocity	Disable Error Hold	Enable SSI DAC Test Mode	Comparat or Test mode	Disab Diag RAM	Diag RAM stop on error	Diag Stop 0=VME 1=P2	Create Diag Data	#	Diag Data Sel 1=preset 0=pattern	#	Create Test Signal	Meas Error LED	Meas Err LED Test Mode	Meas Pres LED	Meas Pres LED Test Mode
	C4	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	C6	RW	SSI DAC Test	#	#	#	#	SSD11	SSD10	SSD9	SSD8	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
	C8	R	Firmware Revision	FR15	FR14	FR13	FR12	FR11	FR10	FR9	FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
	CA	R	Reference ID (Axis ‡ only)	RID Invalid	0	0	0	RID11	RID10	RID9	RID8	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0
	CC	R	Switches	SW1-3	SW1-2	SW1-1	SW1-0	SW2-3	SW2-2	SW2-1	SW2-0	1	1	1	1	SW4-3	SW4-2	SW4-1	SW4-0
	CE	R	Diag RAM Start	0	0	0	0	0	0	DRS9	DRS8	DRS7	DRS6	DRS5	DRS4	DRS3	DRS2	DRS1	DRS0
	D0	R	Quick Reset MSB	QR31	QR30	QR29	QR28	QR27	QR26	QR25	QR24	QR23	QR22	QR21	QR20	QR19	QR18	QR17	QR16
	D2	R	Quick Reset LSB	QR15	QR14	QR13	QR12	QR11	QR10	QR9	QR8	QR7	QR6	QR5	QR4	QR3	QR2	QR1	QR0
	D4	R	Quick Reset Ext	0	0	0	0	0	QR1F	QR2F	QR3F	0	0	0	QR36	QR35	QR34	QR33	QR32
	D6	R	SSI Offset	SSO11	SSO11	SSO11	SSO11	SSO11	SSO10	SSO9	SSO8	SSO7	SSO6	SSO5	SSO4	SSO3	SSO2	SSO1	SSO0
	D8	R	Phase Noise Peak	0	0	0	0	0	PNP10	PNP9	PNP8	PNP7	PNP6	PNP5	PNP4	PNP3	PNP2	PNP1	PNP0
	DA	R	Phase Noise Average	0	0	0	0	0	PNA10	PNA9	PNA8	PNA7	PNA6	PNA5	PNA4	PNA3	PNA2	PNA1	PNA0
	DC	R	SSI Min	SSN15	SSN14	SSN13	SSN12	SSN11	SSN10	SSN9	SSN8	SSN7	SSN6	SSN5	SSN4	SSN3	SSN2	SSN1	SSN0
	C8-DC	W	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	DE	RW	APD Bias DAC	0	0	0	0	ABD11	ABD10	ABD9	ABD8	ABD7	ABD6	ABD5	ABD4	ABD3	ABD2	ABD1	ABD0
	E0	RW	Phase Comp Bias	#	#	#	#	#	ACX10	ACX9	ACX8	ACX7	ACX6	ACX5	ACX4	ACX3	ACX2	ACX1	ACX0
	E2	RW	Phase Comp Control	#	#	#	Disab DB Comp	Disab PB Comp	Enab MB Comp Table	Enab VME Comp Table	Enab VME Phase Comp Bias	#	#	Comp Table Page CTP5	Comp Table Page CTP4	Comp Table Page CTP3	Comp Table Page CTP2	Comp Table Page CTP1	Comp Table Page CTP0
	E4	R	Phase Comp Diag	PCD12	PCD12	PCD12	PCD12	PCD11	PCD10	PCD9	PCD8	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
	E6-FE	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	100-1FE	RW	Data Age RAM (CR2-9 = 0)	DAR17	DAR16	DAR15	DAR14	DAR13	DAR12	DAR11	DAR10	DAR07	DAR06	DAR05	DAR04	DAR03	DAR02	DAR01	DAR00
	100-13E	RW	Aux Registers	Aux registers for ZMI 4100C (CR2-9 = 1) (listed below)								Aux registers for ZMI 4100C (CR2-9 = 1) (listed below)							
	100	R	CE Status	0	0	0	0	0	0	0	0	0	0	CE Init Complete	Hold CN	Hold C0	Hold C1	Enab Comp N	Enab Comp 0
	100	W	CE Command	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reset CEC max/min	Reset CEC Errs
	102	RW	CE Control	CE Age Test	#	#	#	#	#	#	#	#	Enab User Startup	Disab VME Calc Hold	Enab User CN	Enab User C0	Enab User C1	Enab Comp N	Enab Comp 0
	104	RW	CE Error Mask	0	rd over	ds over	psi over	psi4 over	psi4 mag over	psi4c over	cN over	s2 over	s1int over	C1t over	di over	0	0	CE N Max Limit	CE 0 Max Limit
	106	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	108	R	CE Error Status	0	rd over	ds over	psi over	psi4 over	psi4 mag over	psi4c over	cN over	s2 over	s1int over	c1t over	di over	0	0	CE N Max Limit	CE 0 Max Limit
	10A	RW	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	10C	RW	CE Min Vel	CEN15	CEN14	CEN13	CEN12	CEN11	CEN10	CEN9	CEN8	CEN7	CEN6	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0
	10E	RW	CE Max Vel	CEX15	CEX14	CEX13	CEX12	CEX11	CEX10	CEX9	CEX8	CEX7	CEX6	CEX5	CEX4	CEX3	CEX2	CEX1	CEX0
	110	R	CE Build	CEBY1	CEBY0	CEBM3	CEBM2	CEBM1	CEBM0	CEBD4	CEBD3	CEBD2	CEBD1	CEBD0	CEBH4	CEBH3	CEBH2	CEBH1	CEBH0
	112	R	CE Data Age	CED15	CED14	CED13	CED12	CED11	CED10	CED9	CED8	CED7	CED6	CED5	CED4	CED3	CED2	CED1	CED0
	114	R	CE Age	CEA31	CEA30	CEA29	CEA28	CEA27	CEA26	CEA25	CEA24	CEA23	CEA22	CEA21	CEA20	CEA19	CEA18	CEA17	CEA16
	116	R	CE Age	CEA15	CEA14	CEA13	CEA12	CEA11	CEA10	CEA9	CEA8	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0
	118	R	CE C1 Calculated	Float, see “CEC Register Formats” in section 4-2															
	11C	RW	CE C1 User	Float, see “CEC Register Formats” in section 4-2															
	120	R	CE C0 Calculated	Complex Integer (CInt16), see “CEC Register Formats” in section 4-2															
	124	RW	CE C0 User	Complex Integer (CInt16), see “CEC Register Formats” in section 4-2															
	128	RW	CE 0 Limit	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	12A	R	CE 0 Mag	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	12C	R	CE 0 Min	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	12E	R	CE 0 Max	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	130	R	CE CN Calculated	Complex Float (CFloat), see “CEC Register Formats” in section 4-2															
	134	RW	CE CN User	Complex Float (CFloat), see “CEC Register Formats” in section 4-2															
	138	RW	CE N Limit	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	13A	R	CE N Mag	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	13C	R	CE N Min	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	13E	R	CE N Max	Unsigned Short Float (USFloat), see “CEC Register Formats” in section 4-2															
	140-17E	RW	Reserved (Aux)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

APPENDIX A - ZMI 4100 SERIES MEASUREMENT BOARD REGISTER MAP (NUMERICAL)

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	180-1FE	RW	Aux Registers	Aux registers for ZMI 4100 (CR2-9 = 1) (listed below)								Aux registers for ZMI 4100 (CR2-9 = 1) (listed below)							
	180	R	PROM Version	PRV15	PRV14	PRV13	PRV12	PRV11	PRV10	PRV9	PRV8	PRV7	PRV6	PRV5	PRV4	PRV3	PRV2	PRV1	PRV0
	182	R	PROM Revision	PRR15	PRR14	PRR13	PRR12	PRR11	PRR10	PRR9	PRR8	PRR7	PRR6	PRR5	PRR4	PRR3	PRR2	PRR1	PRR0
	184	R	Software Version	SWV15	SWV14	SWV13	SWV12	SWV11	SWV10	SWV9	SWV8	SWV7	SWV6	SWV5	SWV4	SWV3	SWV2	SWV1	SWV0
	186	R	Software Revision	SWR15	SWR14	SWR13	SWR12	SWR11	SWR10	SWR9	SWR8	SWR7	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1	SWR0
	188	R	Software Detail	SWD15	SWD14	SWD13	SWD12	SWD11	SWD10	SWD9	SWD8	SWD7	SWD6	SWD5	SWD4	SWD3	SWD2	SWD1	SWD0
	18A	R	APD Error Code	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
	18C	RW	APD Gain L2 Set	AGS15	AGS14	AGS13	AGS12	AGS11	AGS10	AGS9	AGS8	AGS7	AGS6	AGS5	AGS4	AGS3	AGS2	AGS1	AGS0
	18E	RW	APD Opt Pwr L2 Set	AOS15	AOS14	AOS13	AOS12	AOS11	AOS10	AOS9	AOS8	AOS7	AOS6	AOS5	AOS4	AOS3	AOS2	AOS1	AOS0
	190	RW	APD Sig RMS L2 Set	ASS15	ASS14	ASS13	ASS12	ASS11	ASS10	ASS9	ASS8	ASS7	ASS6	ASS5	ASS4	ASS3	ASS2	ASS1	ASS0
	192	R	Opt Power L2	OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	194	R	Sig RMS L2 Min	SRN15	SRN14	SRN13	SRN12	SRN11	SRN10	SRN9	SRN8	SRN7	SRN6	SRN5	SRN4	SRN3	SRN2	SRN1	SRN0
	196	R	Sig RMS L2 Max	SRX15	SRX14	SRX13	SRX12	SRX11	SRX10	SRX9	SRX8	SRX7	SRX6	SRX5	SRX4	SRX3	SRX2	SRX1	SRX0
	198	RW	Sig RMS L2 Min Lim	SNL15	SNL14	SNL13	SNL12	SNL11	SNL10	SNL9	SNL8	SNL7	SNL6	SNL5	SNL4	SNL3	SNL2	SNL1	SNL0
	19A	RW	Sig RMS L2 Max Lim	SXL15	SXL14	SXL13	SXL12	SXL11	SXL10	SXL9	SXL8	SXL7	SXL6	SXL5	SXL4	SXL3	SXL2	SXL1	SXL0
	19C	R	Opt Power L2 Min	OPN15	OPN14	OPN13	OPN12	OPN11	OPN10	OPN9	OPN8	OPN7	OPN6	OPN5	OPN4	OPN3	OPN2	OPN1	OPN0
	19E	R	Opt Power L2 Max	OPX15	OPX14	OPX13	OPX12	OPX11	OPX10	OPX9	OPX8	OPX7	OPX6	OPX5	OPX4	OPX3	OPX2	OPX1	OPX0
	1A0	R	APD Temp	AT15	AT14	AT13	AT12	AT11	AT10	AT9	AT8	AT7	AT6	AT5	AT4	AT3	AT2	AT1	AT0
	1A2	R	APD Gain L2	AG15	AG14	AG13	AG12	AG11	AG10	AG9	AG8	AG7	KAG6	AG5	AG4	AG3	AG2	AG1	AG0
	1A4	R	Opt Power DC L2	OPD15	OPD14	OPD13	OPD12	OPD11	OPD10	OPD9	OPd8	OPD7	OPD6	OPD5	OPD4	OPD3	OPD2	OPD1	OPD0
	1BA	R	Software Error ID	ERRTYP3	ERRTYP2	ERRTYP1	ERRTYP0	ERRID11	ERRID10	ERRID9	ERRID8	ERRID7	ERRID6	ERRID5	ERRID4	ERRID3	ERRID2	ERRID1	ERRID0
	1BC	R	GSE Target Gain	GTG15	GTG14	GTG13	GTG12	GTG11	GTG10	GTG9	GTG8	GTG7	GTG6	GTG5	GTG4	GTG3	GTG2	GTG1	GTG0
	1BE	R	GSE Actual Gain	GAG15	GAG14	GAG13	GAG12	GAG11	GAG10	GAG9	GAG8	GAG7	GAG6	GAG5	GAG4	GAG3	GAG2	GAG1	GAG0
	1C0	R	GSE SigRMS Gain	GSG15	GSG14	GSG13	GSG12	GSG11	GSG10	GSG9	GSG8	GSG7	GSG6	GSG5	GSG4	GSG3	GSG2	GSG1	GSG0
	1C2	R	GSE MeasDC Low	GML15	GML14	GML13	GML12	GML11	GML10	GML9	GML8	GML7	GML6	GML5	GML4	GML3	GML2	GML1	GML0
	1C4	R	GSE MeasDC High	GMH15	GMH14	GMH13	GMH12	GMH11	GMH10	GMH9	GMH8	GMH7	GMH6	GMH5	GMH4	GMH3	GMH2	GMH1	GMH0
	1C6-1DE	RW	Reserved (Aux)	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1E0	R	PSD LVPS Error ID	x	x	x	x	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	1E2	R	PSD LVPS First Err V	LVPS ID3	LVPS ID2	LVPS ID1	LVPS ID0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E4	R	PSD LVPS First Err Max V	LVPS ID3	LVPS ID2	LVPS ID1	LVPS ID0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E6	R	PSD LVPS First Err Min V	LVPS ID3	LVPS ID2	LVPS ID1	LVPS ID0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E8	R	PSD LVPS First Err VCC In	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1EA	R	PSD VCC In Fault V	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1EC	R	PSD VCC In Max V	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1EE	R	PSD VCC In Min V	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1F0	R	PSD HVPS Error	HVPS ID1	HVPS ID0	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1C6	R	PSD HV Bias Err Meas	ErrStat	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1C8	R	PSD HV Bias Err Exp	ErrStat	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1CA-1FE	RW	Reserved (Aux)	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#
	200-3FE	R	Diag SSI RAM	DFT15	DFT14	DFT13	DFT12	DFT11	DFT10	DFT9	DFT8	DFT7	DFT6	DFT5	DFT4	DFT3	DFT2	DFT1	DFT0
	400-7FE	R	Diag FFT RAM Data (Axis 1 and 3 only)	DFR15	DFR14	DFR13	DFR12	DFR11	DFR10	DFR9	DFR8	DFR7	DFR6	DFR5	DFR4	DFR3	DFR2	DFR1	DFR0
	800-FFE	R	Diag RAM Data	0	0	0	0	DRD11	DRD10	DRD9	DRD8	DRD7	DRD6	DRD5	DRD4	DRD3	DRD2	DRD1	DRD0

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Appendix B Register Map (Alphabetical)

ZMI 4100 Series Measurement Board Register Map

The table in this appendix is a summary of the offset address locations of the registers, and the function for each register bit, for the ZMI 4100 Measurement Boards. This table is a useful reference when programming the board for use in the VME backplane.

Notes on the Table

Shaded areas indicate the register is not available.

Notes for R/W column:

R	Read Only
W	Write only
RW	Write with Readback at same address

Notes for bit definitions: All unused bits are reserved for future use, and should not be used for other purposes. If written, the bit should be set to zero.

#	Bit reserved for future use, may be written and read back.
0	Bit reserved for future use, will always read as zero.
X	Bit reserved for future use, readback data is undefined.
?	Bit undefined and may read as a 0 or a 1.
‡	Register or bit exists in axis 3 only.
§	Register bit exists in axis 1 and 3 only.
◊	Bit can only be written by VME.

Several registers are indicated as "Axis 1 *and* 3 only." These registers also control the next higher axis; axis 1 controls axis 2, and axis 3 controls axis 4.

Writing to a register that does not exist will produce no error and will have no effect. Reading from a register that does not exist will produce no error and will return undefined data.

The P2 interface is 32 bits only. A P2 read or write operates on a register with an even address and the register with the next higher (odd) address. For example, address offset 0x08 reads or writes Control Register 0 (data bits 31-16) and Control Register 1 (data bits 15-0).

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P2	VME	R/W	DESCRIPTION	Byte 2 (VME A1 = 1)								Byte 3 (VME A1 = 1)							
OFFSET	OFFSET			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				Byte 0 (VME A1 = 0)								Byte 1 (VME A1 = 0)							
				D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
	DE	RW	APD Bias DAC	0	0	0	0	ABD11	ABD10	ABD9	ABD8	ABD7	ABD6	ABD5	ABD4	ABD3	ABD2	ABD1	ABD0
	18A	R	APD Error Code	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
	1A2	R	APD Gain L2	AG15	AG14	AG13	AG12	AG11	AG10	AG9	AG8	AG7	KAG6	AG5	AG4	AG3	AG2	AG1	AG0
	18C	RW	APD Gain L2 Set	AGS15	AGS14	AGS13	AGS12	AGS11	AGS10	AGS9	AGS8	AGS7	AGS6	AGS5	AGS4	AGS3	AGS2	AGS1	AGS0
	18E	RW	APD Opt Pwr L2 Set	AOS15	AOS14	AOS13	AOS12	AOS11	AOS10	AOS9	AOS8	AOS7	AOS6	AOS5	AOS4	AOS3	AOS2	AOS1	AOS0
	190	RW	APD Sig RMS L2 Set	ASS15	ASS14	ASS13	ASS12	ASS11	ASS10	ASS9	ASS8	ASS7	ASS6	ASS5	ASS4	ASS3	ASS2	ASS1	ASS0
	1A0	R	APD Temp	AT15	AT14	AT13	AT12	AT11	AT10	AT9	AT8	AT7	AT6	AT5	AT4	AT3	AT2	AT1	AT0
	180-1FE	RW	Aux Registers	Aux registers for ZMI 4100 (CR2-9 = 1)								Aux registers for ZMI 4100 (CR2-9 = 1)							
	100-13E	RW	Aux Registers	Aux registers for ZMI 4100C (CR2-9 = 1)								Aux registers for ZMI 4100C (CR2-9 = 1)							
	128	RW	CE 0 Limit	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	12A	R	CE 0 Mag	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	12E	R	CE 0 Max	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	12C	R	CE 0 Min	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	114	R	CE Age	CEA31	CEA30	CEA29	CEA28	CEA27	CEA26	CEA25	CEA24	CEA23	CEA22	CEA21	CEA20	CEA19	CEA18	CEA17	CEA16
	116	R	CE Age	CEA15	CEA14	CEA13	CEA12	CEA11	CEA10	CEA9	CEA8	CEA7	CEA6	CEA5	CEA4	CEA3	CEA2	CEA1	CEA0
	110	R	CE Build	CEBY1	CEBY0	CEBM3	CEBM2	CEBM1	CEBM0	CEBD4	CEBD3	CEBD2	CEBD1	CEBD0	CEBH4	CEBH3	CEBH2	CEBH1	CEBH0
	120	R	CE C0 Calculated	Complex Integer (CInt16), see “CEC Register Formats” in Section 4.2															
	124	RW	CE C0 User	Complex Integer (CInt16), see “CEC Register Formats” in Section 4.2															
	118	R	CE C1 Calculated	Float, see “CEC Register Formats” in Section 4.2															
	11C	RW	CE C1 User	Float, see “CEC Register Formats” in Section 4.2															
	130	R	CE CN Calculated	Complex Float (CFloat), see “CEC Register Formats” in Section 4.2															
	134	RW	CE CN User	Complex Float (CFloat), see “CEC Register Formats” in Section 4.2															
	100	W	CE Command	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reset CEC max/min	Reset CEC Errs
	102	RW	CE Control	CE Age Test	#	#	#	#	#	#	#	#	Enab User Startup	Disab VME Calc Hold	Enab User CN	Enab User C0	Enab User C1	Enab Comp N	Enab Comp 0
	112	R	CE Data Age	CED15	CED14	CED13	CED12	CED11	CED10	CED9	CED8	CED7	CED6	CED5	CED4	CED3	CED2	CED1	CED0
	104	RW	CE Error Mask	0	rd over	ds over	psi over	psi4 over	psi4 mag over	psi4c over	cN over	s2 over	s1int over	C1t over	di over	0	0	CE N Max Limit	CE 0 Max Limit
	108	R	CE Error Status	0	rd over	ds over	psi over	psi4 over	psi4 mag over	psi4c over	cN over	s2 over	s1int over	c1t over	di over	0	0	CE N Max Limit	CE 0 Max Limit

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	10E	RW	CE Max Vel	CEX15	CEX14	CEX13	CEX12	CEX11	CEX10	CEX9	CEX8	CEX7	CEX6	CEX5	CEX4	CEX3	CEX2	CEX1	CEX0
	10C	RW	CE Min Vel	CEN15	CEN14	CEN13	CEN12	CEN11	CEN10	CEN9	CEN8	CEN7	CEN6	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0
	138	RW	CE N Limit	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	13A	R	CE N Mag	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	13E	R	CE N Max	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	13C	R	CE N Min	Unsigned Short Float (USFloat), see “CEC Register Formats” in Section 4.2															
	100	R	CE Status	0	0	0	0	0	0	0	0	0	0	CE Init Complete	Hold CN	Hold C0	Hold C1	Enab Comp N	Enab Comp 0
3A	74	RW	Compare A Ext	#	#	#	#	#	#	#	#	#	#	#	CA36	CA35	CA34	CA33	CA32
39	72	RW	Compare A LSB	CA15	CA14	CA13	CA12	CA11	CA10	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
38	70	RW	Compare A MSB	CA31	CA30	CA29	CA28	CA27	CA26	CA25	CA24	CA23	CA22	CA21	CA20	CA19	CA18	CA17	CA16
3E	7C	RW	Compare B Ext	#	#	#	#	#	#	#	#	#	#	#	CB36	CB35	CB34	CB33	CB32
3D	7A	RW	Compare B LSB	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
3C	78	RW	Compare B MSB	CB31	CB30	CB29	CB28	CB27	CB26	CB25	CB24	CB23	CB22	CB21	CB20	CB19	CB18	CB17	CB16
08	10	RW	Control Register 0	#	#	#	#	#	#	#	#	Position Direction	Sign Extension	Error Output Source 0=VME 1=P2	Error LED Source 0=VME 1=P2	#	#	Enable Data Age Velocity Comp	#
09	12	RW	Control Register 1 (Filters)	#	#	#	Disable Quick Reset	Glitch Filter GF3	Glitch Filter GF2	Glitch Filter GF1	Glitch Filter GF0	#	Filter KP2	Filter KP1	Filter KP0	#	Filter KV2	Filter KV1	Filter KV0
0A	14	RW	Control Register 2	#	RFV Mode	VME Hold Sample Enable	SCLK VME Sample In 0=SCLK0 1=SCLK1	VME Enable 32-bit Overflow	#	Aux Register Enable	Serial Data Enable	VME Bit Window VBW2	VME Bit Window VBW1	VME Bit Window VBW0	SSI DAC x16	Compare Out Enable	Compare Out Pol	Compare Interrupt Pol	Compare Mode
0B	16	RW	Control Register 3 (Init)	#	Reset Time RT2	Reset Time RT1	Reset Time RT0	Enable Reset Finds Velocity	SCLK Reset Select 0=SCLK0 1=SCLK1	SCLK Reset Enable	Preset Enable	Reset Mode RM1	Reset Mode RM0	P2d ResetAll 1=p2reset 0=p2dreset	P2d RESET Quick Reset Enable	P2d RESET Time Reset Enable	P2d RESET Position Reset Enable	P2d RESET P2 Error Reset Enable	P2d RESET VME Error Reset Enable
0C	18	RW	Control Register 4 (P2)	#	#	P2 Latch Mode 1=Pos Read 0=SCLK	SCLK P2 Sample In 0=SCLK0 1=SCLK1	P2 Enable 32-bit Overflow	P2 Int Driver PID0	P2 Int Level PIL1	P2 Int Level PIL0	P2 Bit Window PBW2	P2 Bit Window PBW1	P2 Bit Window PBW0	P2 RESET Quick Reset Enable	P2 RESET Time Reset Enable	P2 RESET Position Reset Enable	P2 RESET P2 Error Reset Enable	P2 RESET VME Error Reset Enable
0D	1A	RW	Control Register 5 (APD)	#	#	#	#	#	#	#	SSI DAC Mode	#	Disab Auto Gain Reduction	Gain Control AGC	Gain Control Min	Gain Control Max	Bias Control Mode BCM2	Bias Control Mode BCM1	Bias Control Mode BCM0
1D	3A	RW	Control Register 15 (Axis 1 and 3 only)	SCLK0 In Polarity	SCLK1 In Polarity	Reserved	Reserved	#	#	#	#	SCLK Divider SDV3 ‡	SCLK Divider SDV2 ‡	SCLK Divider SDV1 ‡	SCLK Divider SDV0 ‡	Serial Data Size 0=32 1=37	Serial Output Enable P2z ‡	Serial Output Enable P2d ‡	SCLK Serial Sample In 0=SCLK0 1=SCLK1

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1E	3C	RW	Control Register 16 (Axis 1 and 3 only)	SCLK0 Delay SD01	SCLK0 Delay SD00	SCLK0 Sample Time SST03	SCLK0 Sample Time SST02	SCLK0 Sample Time SST01	SCLK0 Sample Time SST00	SCLK0 Out Enable ‡	SCLK Timer Drive ‡ 0=SCLK0 1=SCLK1	SCLK Timer Enable ‡	SCLK Divider Enable ‡	SCLK Divide by 2 Enable ‡	Trigger Delay Enable	#	Disable VME SYS-RESET* input.	User LED ‡	User P2d Out ‡
1F	3E	RW	Control Register 17 (Axis 1 and 3 only)	SCLK1 Delay SD11	SCLK1 Delay SD10	SCLK1 Sample Time SST13	SCLK1 Sample Time SST12	SCLK1 Sample Time SST11	SCLK1 Sample Time SST10	SCLK1 Out Enable ‡	SCLK2 Resync Drive ‡ 0=SCLK0 1=SCLK1	SCLK2 Resync Mode SRM1 ‡	SCLK2 Resync Mode SRM0 ‡	P2 IO Enable ◊	#	P2 Address P2A11 ◊	P2 Address P2A10 ◊	P2 Address P2A9 ◊	P2 Address P2A8 ◊
18	30	RW	Data Age Adjust	DAA15	DAA14	DAA13	DAA12	DAA11	DAA10	DAA9	DAA8	DAA7	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0
	100-1FE	RW	Data Age RAM (CR2-9 = 0)	DAR17	DAR16	DAR15	DAR14	DAR13	DAR12	DAR11	DAR10	DAR07	DAR06	DAR05	DAR04	DAR03	DAR02	DAR01	DAR00
	AA	R	Diag ADC (Axis 1 and 3 only)	ADC Busy	0	0	0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	B4	RW	Diag FFT Control (axis 1 and 3 only)	Data Source DFS3	Data Source DFS2	Data Source DFS1	Data Source DFS0	#	Start on Input	Start on Compare	Data Write Select	#	#	DRP5	DRP4	DRP3	DRP2	DRP1	DRP0
	400-7FE	R	Diag FFT RAM Data (axis 1 and 3 only)	DFR15	DFR14	DFR13	DFR12	DFR11	DFR10	DFR9	DFR8	DFR7	DFR6	DFR5	DFR4	DFR3	DFR2	DFR1	DFR0
	800-FFE	R	Diag RAM Data	0	0	0	0	DRD11	DRD10	DRD9	DRD8	DRD7	DRD6	DRD5	DRD4	DRD3	DRD2	DRD1	DRD0
	CE	R	Diag RAM Start	0	0	0	0	0	0	DRS9	DRS8	DRS7	DRS6	DRS5	DRS4	DRS3	DRS2	DRS1	DRS0
	200-3FE	R	Diag SSI RAM	DFT15	DFT14	DFT13	DFT12	DFT11	DFT10	DFT9	DFT8	DFT7	DFT6	DFT5	DFT4	DFT3	DFT2	DFT1	DFT0
	A4	RW	Diag Temp Monitor Control (Axis 1 and 3 only)	DTSR (0)	DTA6 (0)	DTA5 (1)	DTA4 (0)	DTA3 (1)	DTA2 (0)	DTA1 (1)	DTA0 (0)	DTC7 (0)	DTC6 (0)	DTC5 (0)	DTC4 (0)	DTC3 (1)	DTC2 (1)	DTC1 (0)	DTC0 (1)
	A8	R	Diag Temp Monitor Read (Axis 1 and 3 only)	Diag Temp Mon Busy	0	0	0	0	0	0	0	DTR7	DTR6	DTR5	DTR4	DTR3	DTR2	DTR1	DTR0
	A6	RW	Diag Temp Monitor Write (Axis 1 and 3 only)	# (0)	# (0)	# (0)	# (0)	# (0)	# (0)	# (0)	# (0)	DTW7 (0)	DTW6 (1)	DTW5 (0)	DTW4 (1)	DTW3 (0)	DTW2 (1)	DTW1 (0)	DTW0 (1)
	AC	RW	EEPROM Control (Axis ‡ only)	#	#	EEOP1	EEOP0	#	#	EEA9	EEA8	EEA7	EEA6	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
	B0	R	EEPROM Read (Axis ‡ only)	EER15	EER14	EER13	EER12	EER11	EER10	EER9	EER8	EER7	EER6	EER5	EER4	EER3	EER2	EER1	EER0
	AE	RW	EEPROM Write (Axis ‡ only)	EEW15	EEW14	EEW13	EEW12	EEW11	EEW10	EEW9	EEW8	EEW7	EEW6	EEW5	EEW4	EEW3	EEW2	EEW1	EEW0
07	0E	R	Firmware Version	Firmware Version FV15	Firmware Version FV14	Firmware Version FV13	Firmware Version FV12	Firmware Version FV11	Firmware Version FV10	Firmware Version FV9	Firmware Version FV8	Firmware Version FV7	Firmware Version FV6	Firmware Version FV5	Firmware Version FV4	Firmware Version FV3	Firmware Version FV2	Firmware Version FV1	Firmware Version FV0
	C8	R	Firmware Revision	FR15	FR14	FR13	FR12	FR11	FR10	FR9	FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1BE	R	GSE Actual Gain	GAG15	GAG14	GAG13	GAG12	GAG11	GAG10	GAG9	GAG8	GAG7	GAG6	GAG5	GAG4	GAG3	GAG2	GAG1	GAG0
	1C2	R	GSE MeasDC Low	GML15	GML14	GML13	GML12	GML11	GML10	GML9	GML8	GML7	GML6	GML5	GML4	GML3	GML2	GML1	GML0
	1C4	R	GSE MeasDC High	GMH15	GMH14	GMH13	GMH12	GMH11	GMH10	GMH9	GMH8	GMH7	GMH6	GMH5	GMH4	GMH3	GMH2	GMH1	GMH0
	1C0	R	GSE SigRMS Gain	GSG15	GSG14	GSG13	GSG12	GSG11	GSG10	GSG9	GSG8	GSG7	GSG6	GSG5	GSG4	GSG3	GSG2	GSG1	GSG0
	1BC	R	GSE Target Gain	GTG15	GTG14	GTG13	GTG12	GTG11	GTG10	GTG9	GTG8	GTG7	GTG6	GTG5	GTG4	GTG3	GTG2	GTG1	GTG0
36	6C	RW	Offset Ext	#	#	#	#	#	O1F	O2F	O3F	#	#	#	O36	O35	O34	O33	O32
35	6A	RW	Offset LSB	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0
34	68	RW	Offset MSB	O31	O30	O29	O28	O27	O26	O25	O24	O23	O22	O21	O20	O19	O18	O17	O16
	1A4	R	Opt Power DC L2	OPD15	OPD14	OPD13	OPD12	OPD11	OPD10	OPD9	OPd8	OPD7	OPD6	OPD5	OPD4	OPD3	OPD2	OPD1	OPD0
	192	R	Opt Power L2	OP15	OP14	OP13	OP12	OP11	OP10	OP9	OP8	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
	19E	R	Opt Power L2 Max	OPX15	OPX14	OPX13	OPX12	OPX11	OPX10	OPX9	OPX8	OPX7	OPX6	OPX5	OPX4	OPX3	OPX2	OPX1	OPX0
	19C	R	Opt Power L2 Min	OPN15	OPN14	OPN13	OPN12	OPN11	OPN10	OPN9	OPN8	OPN7	OPN6	OPN5	OPN4	OPN3	OPN2	OPN1	OPN0
14		R	P2 Absolute Phase	0	0	0	AP12	AP11	AP10	AP9	AP8	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
00		W	P2 Command Register	X	X	X	Load Position	Compar-ator Preset 1	Compar-ator Preset 0	Reserved	X	X	Start Bias Calc	Reset Axis	Reset Position Quick	Reset Time	Reset Position	Reset P2 Errors	Reset VME Errors
12	24	W	P2 Error Clear 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
13	26	W	P2 Error Clear 1	X	X	X	X	X	X	P2 Ext. Sample (SCLK)	Reserved	X	X	Compare	P2 32 bit Position Overflow	Reserved	37 bit Position Overflow	User Velocity Error	Velocity Error
0F		W	P2 Error Clear 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	X	X	X	X	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
12	24	R	P2 Error Status 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
13	26	R	P2 Error Status 1	0	0	0	0	0	0	P2 Ext. Sample (SCLK)	Reserved	0	0	Compare	P2 32 bit Position Overflow	Reserved	37 bit Position Overflow	User Velocity Error	Velocity Error
0F		R	P2 Error Status 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	0	0	0	0	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
10	20	RW	P2 Interrupt Enable 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
11	22	RW	P2 Interrupt Enable 1	#	#	#	#	#	#	P2 Ext. Sample (SCLK)	Reserved	#	#	Compare	P2 32 bit Position Overflow	Reserved	37 bit Position Overflow	User Velocity Error	Velocity Error
0E		RW	P2 Interrupt Enable 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	#	#	#	#	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
23		R	P2 Position Errs	0	0	0	0	0	0	0	0	0	User P2d Out ‡	User P2d In	Comparat or state	Meas Error	Meas Present	Ref Error	Ref Present
22		R	P2 Position Ext	0	0	0	0	0	PP1F	PP2F	PP3F	PP36	PP36	PP36	PP36	PP35	PP34	PP33	PP32
21		R	P2 Position LSB	PP15	PP14	PP13	PP12	PP11	PP10	PP9	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
20		R	P2 Position MSB	PP31	PP30	PP29	PP28	PP27	PP26	PP25	PP24	PP23	PP22	PP21	PP20	PP19	PP18	PP17	PP16
2B		R	P2 Time LSB	PT15	PT14	PT13	PT12	PT11	PT10	PT9	PT8	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0
2A		R	P2 Time MSB	PT31	PT30	PT29	PT28	PT27	PT26	PT25	PT24	PT23	PT22	PT21	PT20	PT19	PT18	PT17	PT16
29		R	P2 Velocity LSB	PV15	PV14	PV13	PV12	PV11	PV10	PV9	PV8	PV7	PV6	PV5	PV4	PV3	PV2	PV1	PV0
28		R	P2 Velocity MSB	PV31	PV30	PV29	PV28	PV27	PV26	PV25	PV24	PV23	PV22	PV21	PV20	PV19	PV18	PV17	PV16
	E0	RW	Phase Comp Bias	#	#	#	#	#	ACX10	ACX9	ACX8	ACX7	ACX6	ACX5	ACX4	ACX3	ACX2	ACX1	ACX0
	E2	RW	Phase Comp Control	#	#	#	Disab DB Comp	Disab PB Comp	Enab MB Comp Table	Enab VME Comp Table	Enab VME Phase Comp Bias	#	#	Comp Table Page CTP5	Comp Table Page CTP4	Comp Table Page CTP3	Comp Table Page CTP2	Comp Table Page CTP1	Comp Table Page CTP0
	E4	R	Phase Comp Diag	PCD12	PCD12	PCD12	PCD12	PCD11	PCD10	PCD9	PCD8	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
	DA	R	Phase Noise Average	0	0	0	0	0	PNA10	PNA9	PNA8	PNA7	PNA6	PNA5	PNA4	PNA3	PNA2	PNA1	PNA0
17	2E	RW	Phase Noise Limit	#	#	#	#	#	PNL10	PNL9	PNL8	PNL7	PNL6	PNL5	PNL4	PNL3	PNL2	PNL1	PNL0
	D8	R	Phase Noise Peak	0	0	0	0	0	PNP10	PNP9	PNP8	PNP7	PNP6	PNP5	PNP4	PNP3	PNP2	PNP1	PNP0
32	64	RW	Preset Pos Ext	#	#	#	#	#	PR1F	PR2F	PR3F	#	#	#	PR36	PR35	PR34	PR33	PR32
31	62	RW	Preset Pos LSB	PR15	PR14	PR13	PR12	PR11	PR10	PR9	PR8	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0
30	60	RW	Preset Pos MSB	PR31	PR30	PR29	PR28	PR27	PR26	PR25	PR24	PR23	PR22	PR21	PR20	PR19	PR18	PR17	PR16
	182	R	PROM Revision	PRR15	PRR14	PRR13	PRR12	PRR11	PRR10	PRR9	PRR8	PRR7	PRR6	PRR5	PRR4	PRR3	PRR2	PRR1	PRR0
	180	R	PROM Version	PRV15	PRV14	PRV13	PRV12	PRV11	PRV10	PRV9	PRV8	PRV7	PRV6	PRV5	PRV4	PRV3	PRV2	PRV1	PRV0
	1C6	R	PSD HV Bias Err Meas	ErrStat	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1C8	R	PSD HV Bias Err Exp	ErrStat	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1F0	R	PSD HVPS Error	HVPS ID1	HVPS ID0	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E0	R	PSD LVPS Error ID	x	x	x	x	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	1E4	R	PSD LVPS First Err Max V	LVPS ID3	LVPS ID2	LVPS ID1	LVPS ID0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E6	R	PSD LVPS First Err Min V	LVPS ID3	LVPS ID2	LVPS ID1	LVPS ID0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E2	R	PSD LVPS First Err V	LVPS ID3	LVPS ID2	LVPS ID1	LVPS ID0	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1E8	R	PSD LVPS First Err VCC In	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1EA	R	PSD VCC In Fault V	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1EC	R	PSD VCC In Max V	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	1EE	R	PSD VCC In Min V	X	X	X	X	ADC11	ADC10	ADC9	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	D4	R	Quick Reset Ext	0	0	0	0	0	QR1F	QR2F	QR3F	0	0	0	QR36	QR35	QR34	QR33	QR32
	D2	R	Quick Reset LSB	QR15	QR14	QR13	QR12	QR11	QR10	QR9	QR8	QR7	QR6	QR5	QR4	QR3	QR2	QR1	QR0
	D0	R	Quick Reset MSB	QR31	QR30	QR29	QR28	QR27	QR26	QR25	QR24	QR23	QR22	QR21	QR20	QR19	QR18	QR17	QR16
	CA	R	Reference ID (Axis ‡ only)	RID Invalid	0	0	0	RID11	RID10	RID9	RID8	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0
1C	38	RW	Sample Timer (Axis ‡ only)	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
01	02	W	SCLK Command Register (Axis ‡ only)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	External Sample (SCLK1)	External Sample (SCLK0)
1B	36	R	Sig RMS L2	SRMS15	SRMS14	SRMS13	SRMS12	SRMS11	SRMS10	SRMS9	SRMS8	SRMS7	SRMS6	SRMS5	SRMS4	SRMS3	SRMS2	SRMS1	SRMS0
	196	R	Sig RMS L2 Max	SRX15	SRX14	SRX13	SRX12	SRX11	SRX10	SRX9	SRX8	SRX7	SRX6	SRX5	SRX4	SRX3	SRX2	SRX1	SRX0
	19A	RW	Sig RMS L2 Max Lim	SXL15	SXL14	SXL13	SXL12	SXL11	SXL10	SXL9	SXL8	SXL7	SXL6	SXL5	SXL4	SXL3	SXL2	SXL1	SXL0
	194	R	Sig RMS L2 Min	SRN15	SRN14	SRN13	SRN12	SRN11	SRN10	SRN9	SRN8	SRN7	SRN6	SRN5	SRN4	SRN3	SRN2	SRN1	SRN0
	198	RW	Sig RMS L2 Min Lim	SNL15	SNL14	SNL13	SNL12	SNL11	SNL10	SNL9	SNL8	SNL7	SNL6	SNL5	SNL4	SNL3	SNL2	SNL1	SNL0
	188	R	Software Detail	SWD15	SWD14	SWD13	SWD12	SWD11	SWD10	SWD9	SWD8	SWD7	SWD6	SWD5	SWD4	SWD3	SWD2	SWD1	SWD0
	1BA	R	Software Error ID	ERRTYP3	ERRTYP2	ERRTYP1	ERRTYP0	ERRID11	ERRID10	ERRID9	ERRID8	ERRID7	ERRID6	ERRID5	ERRID4	ERRID3	ERRID2	ERRID1	ERRID0
	186	R	Software Revision	SWR15	SWR14	SWR13	SWR12	SWR11	SWR10	SWR9	SWR8	SWR7	SWR6	SWR5	SWR4	SWR3	SWR2	SWR1	SWR0
	184	R	Software Version	SWV15	SWV14	SWV13	SWV12	SWV11	SWV10	SWV9	SWV8	SWV7	SWV6	SWV5	SWV4	SWV3	SWV2	SWV1	SWV0
15	2A	R	SSI Avg	SSA15	SSA14	SSA13	SSA12	SSA11	SSA10	SSA9	SSA8	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
	C6	RW	SSI DAC Test	#	#	#	#	SSD11	SSD10	SSD9	SSD8	SSD7	SSD6	SSD5	SSD4	SSD3	SSD2	SSD1	SSD0
16	2C	R	SSI Max	0	0	0	0	SSM11	SSM10	SSM9	SSM8	SSM7	SSM6	SSM5	SSM4	SSM3	SSM2	SSM1	SSM0
	DC	R	SSI Min	SSN15	SSN14	SSN13	SSN12	SSN11	SSN10	SSN9	SSN8	SSN7	SSN6	SSN5	SSN4	SSN3	SSN2	SSN1	SSN0
	D6	R	SSI Offset	SSO11	SSO11	SSO11	SSO11	SSO11	SSO10	SSO9	SSO8	SSO7	SSO6	SSO5	SSO4	SSO3	SSO2	SSO1	SSO0
1A	34	RW	SSI Squelch	#	#	#	#	SSQ11	SSQ10	SSQ9	SSQ8	SSQ7	SSQ6	SSQ5	SSQ4	SSQ3	SSQ2	SSQ1	SSQ0
00	00	R	Status Register 0	System Type SY3	System Type SY2	System Type SY1	System Type SY0	0	VME External Sample Flag	P2 INT Pending	VME IRQ Pending	APD Init Complete	Overtemp	FPGA DLL Locked	Reference PLL Locked	Reference Fiber Signal Present	Reference Tree Signal Present	Reference Signal Present	Power OK
01	02	R	Status Register 1	User P2d In	Comparator or State (raw)	Config 2	Config 1	Config 0	FIFO DAV	FIFO Overflow	0	0	0	0	Cmd Busy	Bias Calc Busy	Reserved	Measure Signal Present	Reset Complete
	CC	R	Switches	SW1-3	SW1-2	SW1-1	SW1-0	SW2-3	SW2-2	SW2-1	SW2-0	1	1	1	1	SW4-3	SW4-2	SW4-1	SW4-0

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	C0	W	Test Command 0	X	X	X	X	X	X	X	X	X	X	X	X	Reset Opt Power L2 Min/Max	Reset Sig RMS L2 Min/Max	Reset SSI Max/Min	Reset Phase Noise Peak
	A0	W	Test Command 1 (Axis 1 and 3 only)	Reset Controller ‡	X	X	X	X	X	X	X	X	X	X	Stop Diag FFT Data	Start Diag FFT Data	Clear EEPROM Error	Clear Ref ID ‡	Send Ref ID ‡
	C2	RW	Test Control 0	Disable Excess Velocity	Disable Error Hold	Enable SSI DAC Test Mode	Comparat or Test mode	Disab Diag RAM	Diag RAM stop on error	Diag Stop 0=VME 1=P2	Create Diag Data	#	Diag Data Sel 1=preset 0=pattern	#	Create Test Signal	Meas Error LED	Meas Err LED Test Mode	Meas Pres LED	Meas Pres LED Test Mode
	A2	RW	Test Control 1 (Axis 1 and 3 only)	Bias Supply Enab ‡	Bias Supply Test ‡	Bias Supply Override ‡	Config 10m	#	Ref Err LED	Ref Pres LED ‡	Ref LED Test Mode	#	#	#	ADC Mux AM4 §	ADC Mux AM3 §	ADC Mux AM2 §	ADC Mux AM1 §	ADC Mux AM0 §
	C0	R	Test Status 0	SW5-2	SW5-1	Meas State 3	Meas State 2	Meas State1	Meas State 0	0	Diag RAM busy	0	0	VME GAP	VME GA4	VME GA3	VME GA2	VME GA1	VME GA0
	A0	R	Test Status 1 (Axis 1 and 3 only)	0	0	0	0	EEPROM Error	Diag FFT Data Busy	EEPROM Busy ‡	A_PS_OK	SCLK1 Input Time SIT13	SCLK1 Input Time SIT12	SCLK1 Input Time SIT11	SCLK1 Input Time SIT10	SCLK0 Input Time SIT03	SCLK0 Input Time SIT02	SCLK0 Input Time SIT01	SCLK0 Input Time SIT00
	B6	R	Test Status 2 (Axis 1 and 3 only)	Bias Supply Enable	Bias Supply Test	0	0	0	**0**	0	0	0	0	0	0	0	0	HVPS Ok	LVPS Ok
19	32	RW	User Excess Velocity	UEV15 (1)	UEV14 (1)	UEV13 (1)	UEV12 (1)	UEV11 (1)	UEV10 (1)	UEV9 (1)	UEV8 (1)	UEV7 (1)	UEV6 (1)	UEV5 (1)	UEV4 (1)	UEV3 (1)	UEV2 (1)	UEV1 (1)	UEV0 (1)
	28	R	VME Absolute Phase	0	0	0	AP12	AP11	AP10	AP9	AP8	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
	00	W	VME Command Register	X	X	X	Load Position	Compar-ator Preset 1	Compar-ator Preset 0	Sample VME Position	FIFO Clear	X	Start Bias Calc	Reset Axis	Reset Position Quick	Reset Time	Reset Position	Reset P2 Errors	Reset VME Errors
	08	W	VME Error Clear 0	CEC Error	Phase Noise Error	Accelerati on Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
	0A	W	VME Error Clear 1	X	X	X	X	X	X	Reserved	VME External Sample (SCLK)	X	X	Compare	P2 32 bit Position Overflow	VME 32 bit Position Overflow	37 bit Position Overflow	User Velocity Error	Velocity Error
	1E	W	VME Error Clear 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	X	X	X	X	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error

P2	VME	R/W	DESCRIPTION	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	08	R	VME Error Status 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
	0A	R	VME Error Status 1	0	0	0	0	0	0	Reserved	VME External Sample (SCLK)	0	0	Compare	P2 32 bit Position Overflow	VME 32 bit Position Overflow	37 bit Position Overflow	User Velocity Error	Velocity Error
	1E	R	VME Error Status 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	0	0	0	0	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
	04	RW	VME Interrupt Enable 0	CEC Error	Phase Noise Error	Acceler-ation Error	Measure Signal Glitch	Measure Signal Dropout	SSI Max Limit	Measure Signal Saturated	Measure Signal Missing	Overtemp Error	FPGA Sync Error	Reset Failure	Reset Complete	Reference PLL Error	Reference Signal Missing	Write error	Power Error
	06	RW	VME Interrupt Enable 1	VME Interrupt Enable	#	#	#	#	#	Reserved	VME External Sample (SCLK)	#	#	Compare	P2 32 bit Position Overflow	VME 32 bit Position Overflow	37 bit Position Overflow	User Velocity Error	Velocity Error
	1C	RW	VME Interrupt Enable 2	Proc Init Busy	Proc Fail	Bias Supply Error	Write Protect Error	#	#	#	#	Sig Max	Sig Min	Bias Calc Complete	Bias Error	APD DC Error	APD Command Error	APD Fail Error	APD Temp Error
	B2	RW	VME Interrupt Vector (Axis 1 and 3 only)	X	#	#	#	#	VME Interrupt Level VIL2	VME Interrupt Level VIL1	VME Interrupt Level VIL0	VME Interrupt Vector VIV7	VME Interrupt Vector VIV6	VME Interrupt Vector VIV5	VME Interrupt Vector VIV4	VME Interrupt Vector VIV3	VME Interrupt Vector VIV2	VME Interrupt Vector VIV1	VME Interrupt Vector VIV0
	46	R	VME Position Errs	0	0	0	0	0	0	0	0	0	User P2d Out	User P2d In	Comparat or state	Meas Error	Meas Present	Ref Error	Ref Present
	44	R	VME Position Ext	0	0	0	0	0	VP1F	VP2F	VP3F	VP36	VP36	VP36	VP36	VP35	VP34	VP33	VP32
	82	R	VME Position FIFO LSB	VPF15	VPF14	VPF13	VPF12	VPF11	VPF10	VPF9	VPF8	VPF7	VPF6	VPF5	VPF4	VPF3	VPF2	VPF1	VPF0
	80	R	VME Position FIFO MSB	VPF31	VPF30	VPF29	VPF28	VPF27	VPF26	VPF25	VPF24	VPF23	VPF22	VPF21	VPF20	VPF19	VPF18	VPF17	VPF16
	42	R	VME Position LSB	VP15	VP14	VP13	VP12	VP11	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
	40	R	VME Position MSB	VP31	VP30	VP29	VP28	VP27	VP26	VP25	VP24	VP23	VP22	VP21	VP20	VP19	VP18	VP17	VP16
	4E	R	VME Sample Position Errs	0	0	0	0	0	0	0	0	0	User P2d Out ‡	User P2d In	Comparat or state	Meas Error	Meas Present	Ref Error	Ref Present
	4C	R	VME Sample Position Ext	0	0	0	0	0	VSP1F	VSP2F	VSP3F	VSP36	VSP36	VSP36	VSP36	VSP35	VSP34	VSP33	VSP32
	4A	R	VME Sample Position LSB	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0
	48	R	VME Sample Position MSB	VSP31	VSP30	VSP29	VSP28	VSP27	VSP26	VSP25	VSP24	VSP23	VSP22	VSP21	VSP20	VSP19	VSP18	VSP17	VSP16
	56	R	VME Time LSB	VT15	VT14	VT13	VT12	VT11	VT10	VT9	VT8	VT7	VT6	VT5	VT4	VT3	VT2	VT1	VT0
	54	R	VME Time MSB	VT31	VT30	VT29	VT28	VT27	VT26	VT25	VT24	VT23	VT22	VT21	VT20	VT19	VT18	VT17	VT16
	52	R	VME Velocity LSB	VV15	VV14	VV13	VV12	VV11	VV10	VV9	VV8	VV7	VV6	VV5	VV4	VV3	VV2	VV1	VV0
	50	R	VME Velocity MSB	VV31	VV30	VV29	VV28	VV27	VV26	VV25	VV24	VV23	VV22	VV21	VV20	VV19	VV18	VV17	VV16

Appendix C Manual Revisions

Revision A to B

Page No.	Change
General	Register names changes. APD Gain → APD Gain L2 APD Gain Set → APD Gain L2 Set APD Opt Pwr Set → APD Opt Pwr L2 Set APD Sig RMS Set → APD Sig RMS L2 Set Opt Power Max → Opt Power L2 Max Opt Power Min → Opt Power L2 Min Opt Power → Opt Power L2 Sig RMS → Sig RMS L2 Sig RMS Max Limit → Sig RMS L2 Max Lim Sig RMS Max → Sig RMS L2 Max Sig RMS Min Limit → Sig RMS L2 Min Lim Sig RMS Min → Sig RMS L2 Min
front matter	Update manual revision letter and date, and update contents.
1-8	Update specifications, operating temperature 15 to 50°C.
1-9	Change board version and revision tracking information; table made into two.
1-10	Add sentence regarding extended data age feature.
2-10	Change content related to FPGA temperature monitor, update LED description.
2-14	Update Signal Strength Measurement section.
3-24	Add note 8. APD Temperature values are degrees C * 256.
3-26	Table 3-21 revised.
Chapter 4 (various)	Add APD Gain L2, APD Temp, PROM Version, and PROM Revision register descriptions. Delete Kit Version and Kit Revision registers. Update Control Register 5, ADP Gain L2 Set, APD Opt Pwr L2 Set, APD Sig RMS L2 Set, Sig RMS L2 Min Lim, Sig RMS L2 Max Lim, and Test Command 1 register descriptions. Update chapter 4 page numbering.
4-7	Update error register 2, bits 2-5, and 12 descriptions.
4-52	Update Status Register 1 bits 3 and 4.
App. A and B	Update register maps with register changes.

Revision B to C

This revision covers changes for Firmware SPM8020-9276-01 Rev B, Software SPM8020-9277-01 Rev C, and PROM SPM8020-9277-03 Rev C, -05 Rev C.

Page No.	Change
General	New registers added- Opt Power DC L2, Phase Comp Bias, Phase Comp Control, and Phase Comp Diag. Structured numbering system added to headings.
front matter	Update manual revision letter and date, and update contents.
1-10	Optical Power Operating Range section added.
2-6	Reference Error LED description changed.
2-8, 3-15, 4-48, 4-49	Changed 1.24 V to 1.25 V.
2-8, 2-9	SSI (Signal Strength Indicator) Connector section updated.
2-15	7500 changed to 7200 and note added.
2-16	Signal Strength Measurement equations updated.
2-17	Measurement Performance section added.
3-24, 3-26	Note 9 added, Axis Data Format updated.
3-42	0.178 changed to 17.8.
4-4, 4-5, 4-6, 4-7	Error Status and Interrupt Enable Registers section updated. *APD Fail Error* bit added to table on page 4-7.
4-11 to 4-13	APD Error Code description updated.
4-14	APD Gain L2 description updated.
4-18	CE Status Register bit 0 and 1 changed to enabled.
4-25	Control Register 5, table 4-6 updated.
4-40	Opt Power DC L2 register added, Opt Power L2 description updated.
4-44	Phase Comp Bias, Phase Comp Control, and Phase Comp Diag description added.
Appendix A, Appendix B	Added Opt Power DC L2, Phase Comp Bias, Phase Comp Control, Phase Comp Diag registers. Added *APD Fail Error* bit in P2/VME Error Clear 2, Interrupt Enable 2, and Error Status 2 registers. Control Reg 5, bit 6 changed to Disab Auto Gain Reduction.
Appendix D	Register names corrected.

Revision C to D

Page No.	Change
General	Various small editorial corrections.
3-8 and 3-9	Added details to P2bus read and write timing.
3-12	Serial Interface description updated.
3-18	Signal propagation figure updated.
3-19	Reference propagation table updated.
3-21	Added note after bit window tables.
3-25	Revised EPROM Board Data table, offset words 0 and 18.
3-29	Figure reference in compensation algorithm fixed.
3-41	Instructions for clearing CE Error Status register updated.
3-42	Cyclic error ratio equations corrected. CE 0 and CE N Mag, Min, and Max registers description updated.
4-4	Fixed bit 2 and 3 type.
4-5	Fixed bit 7 type.
4-9	USFloat equation convert to real number corrected.
4-17	CE Error Status register address corrected. Section on clearing added.
4-47	Sample Timer register description revised.
4-53	Bits 9 and 10 descriptions added for Status Register 1.
4-61	Bit 8 description added for VME Command register.
4-63	VME Position FIFO register added.
Appendix A, Appendix B	Above mentioned bit descriptions, and VME Position FIFO LSB and VME Position FIFO MSB registers added.
Reference	Digital Filter Performance graphs added at end of manual as reference.

Revision D to E

Page No.	Change
3-12	Changed serial interface output rates.
3-15, 3-16	Revised section on Reset axis function; added *Disable Quick Reset* bit details.
3-26	EEPROM Board Data table updated.
4-4, 4-5	Updated error status register bits 2, 3, 6, 7, and 11 descriptions.
4-21	Updated Control Register 1 bit 12 description.
4-22	Updated Control Register 2 bits 13 and 14 descriptions.
4-23	Updated Control Register 3 bit 11 description.
4-26	Updated Control Register 15 bits 14 and 15 descriptions.
4-36	Diag SSI RAM register description updated.
4-37	Updated Diag Temp Monitor Control register description.
4-43	Updated P2 Command Register bit 4 description.
4-54	Updated Status Register 0 bit 6 description.
4-63	Updated VME Command Register bit 4 description.
Appendix A, Appendix B	Above mentioned bit changes added.
Appendix D	Updated.

Revision E to F

Page No.	Change
General	Removed mention of 4102 board.
1-1	Added new patent number.
1-11 to 1-13	Added section on mixing ZMI measurement boards.
3-6	Updated P2bus Signals description.
3-15, 3-16	Updated axis reset function description.
4-5	Updated bit 8 in Error Clear, Error Status and Interrupt Enable Register 0 table.
4-7	Updated Error Register 2 bit 2.
4-13	Updated axis error code 130.
4-14	Updated APD Gain L2 Set and APD Opt Pwr L2 Set register descriptions.
4-15	Updated APD Sig RMS L2 Set register description.
4-21	Updated Control Register 2 bit 14.
4-25	Updated bias control modes table.
4-48	Updated Sig RMS L2 Max Lim register description.
4-49	Updated Sig RMS L2 Min Lim register description.
4-52	Updated SSI Squelch register description.
4-53	Updated Status Register 1 bit 9.

Revision F to G

Page No.	Change
4-24	Note updated with reference to GSE registers.
4-39 to 4-40	Added GSE (Gain Set Error) registers.
4-46 to 4-48	Added PSD (Power Supply Diagnostic) registers.
D-3 to D-4	Table updated, notes 2, 3, and 4 added.

Revision G to H

Page No.	Change
1-8	Change CEC Initialization Time specification to 4.1 ms.
2-15	Notes added to Signal Strength Measurement table.
3-37	Added note to filter table.
3-41	Startup description updated.
4-41, 4-42	Notes added to Opt Power DC L2, Opt Power L2, Opt Power L2 Max, and Opt Power L2 Min registers.

Revision H to J

Page No.	Change
3-41	Changed Startup description.
4-18	Changed CE Status Register bit 5 description.

Revision J to K

Page No.	Change
2-2	Added details showing physical temp monitor locations.
3-24	Section on Position Output added.
3-25	Section on APD Controller Software Errors added.
3-34	Updated Selecting Kv and Kp Values section.
4-7	Updated Error Status 2 bit 8 description.
4-12	Updated System Error Codes table.
4-21	Added description to Control Register 1 bit 12.
4-55	Added Software Error ID register description.
A-10, B-8	Added Software Error ID register listings.
D-3	Added line 48.
D-4, D-5	Updated note 2 thru 4, and added note 5.

Revision K to L

Page No.	Change
1-8	Updated Measurement Axis Optical Input Power specification.

Revision L to M

Page No.	Change
1-8	Updated CEC Initialization Velocity specification.
4-22, 4-24	Update table reference for VME Bit Window and P2 Bit Window.
4-44, 4-53, 4054	Fixed Opt Power L2 Min/Max and Sig RMS L2 Min/Max register descriptions (not affected by axis reset).

Revision M to N

Page No.	Change
3-43	Update CEC section dealing with CE max/min velocity.
4-20, 4-22, 4-23	Remove all P3 references (not applicable).
4-26, 4-27, A-5, B-4, B-5	Add axis 3 only notation. Control Register 15, bits 7-4 are axis 3 only. Control Register 16, bits 5 and 6 are axis 3 only.

Revision N to P

Page No.	Change
3-9	Fixed subscript error in table.
4-6	Changed User Velocity Error to User Excess Velocity register.
4-41	Fixed addresses for GSE MeasDC High; fixed name of GSE Sig RMS register.
4-53	Fixed spelling error.
4-58	Updated Status Register 1 bit 1 description.
A-5	Fixed spelling error (SCLK).

Revision P to Q

Page No.	Change
1-2, 1-10, 1-12, 4-57	Removed reference to ZMI 4004CEC.
1-5	Removed ZMI 4102 from Figure 1-3.
2-4	Removed 4104 and 4102 from Figure 2-3.
2-10	Updated Laser Head Models.
3-18, 3-40	Removed HSP.
4-25, 4-58, A-3, A-5, B-4, B-8	Changed any HSP bits to Reserved in Control Register 15 and Status Register 1.

Revision Q to R

Page No.	Change
1-1	Update PCB Assembly and Kit P/Ns.
1-7	Update PCB Assembly and Kit P/Ns. Change HSSDC to HSSDC2.
1-10	Update Laser Head models and add information on 4100 board compatibility.
2-4	Update Figure 2-4 with HSSDC2 cables.
2-6	Update Front Panel and change HSSDC to HSSDC2.
2-8	Update Reference Tree Connectors.

Appendix D Firmware Revisions

ZMI 4000/4100 Firmware Revisions

The following table summarizes functional changes for the ZMI 4000/4100 firmware versions, and shows the applicable revisions for each.

Range	Example	Meaning
None	-	Does not apply
All	all	Applies to all revisions of the firmware
Added	B+	Applies to the noted revision, and all later revisions
Range	B-C	Applies to the noted range of revisions (inclusive)

Line	FW Src	4004 BC	4004	4104/ 4104C	Product
		CE!		**CE!**	
	-01	**-01**	**-01**	**-01**	**Firmware Source SPM8020-9275-xx**
	all	**-02**	**-09**		**Firmware SPM8020-9274-xx**
	All			**-01**	**Firmware SPM8020-9276-xx**
		7402	**7409**	**7601**	**Firmware Version Register (hex)**
					Hardware Compatibility
	A-C	-	-	-	PCB Assy 8020-0500-01 Rev A-C (Obsolete)
	all	all	all	-	PCB Assy 8020-0500-01 Rev D+ (4004)
	all	all	all	-	PCB Assy 8020-0500-02 Rev A+ (4002)
	C+	-	-	-	PCB Assy 8020-0500-03 Rev A+ (4004CEC)
	A-C	-	-	-	PCB Assy 8020-0500-07 Rev A+ (Obsolete)
	D+	-	-	all	PCB Assy 8020-0700-01 Rev A+ (4104/4104C)
		C+	A+	-	HSP Mezzanine board Rev A+

Line	FW Src	4004 BC	4004 -09	4104/ 4104C	Product Firmware Features and Changes
		CE!		CE!	
		7402	7409	7601	**Firmware Version Register (hex)**
1	A-C	-		-	Diag ADC Channel 12 = 1.8 V
2	all	all	all	-	Diag ADC Channel 12 = 1.5 V
3	all	all	all	all	Diag FFT Control register
4	all	all	all	all	Diag FFT RAM Data
5	all	all	all	all	Test Command 1, *Start Diag FFT Data*, *Stop Diag FFT Data*
6	all	all	all	all	Test Status 1, *Diag FFT Data Busy*
7	B+	B+	all	all	Control Register 2, *SSI DAC x16*
8	B+	B+	all	all	Control Register 16, 17, *SCLK Sample Time* default value = 3
9	B+	B+	all	all	Control Register 16, *SCLK Divider Enable*, *SCLK Divide by 2 Enable*
10	B+	B+	all	all	Control Register 17, *P2 IO Enable* default set by SW5-1
11	B+	B+	all	all	Control Register 17, *SCLK Divider*
12	B+	B+	all	all	Diag FFT Control, *Start On Input*, *Start on Compare*
13	B+	B+	all	all	SSI Min register
14	B+	B+	all	all	SSI Squelch register
15	C+	C+	all	all	Control Register 2, *VME Hold Sample Enable*
16	C+	C+	all	all	Data Age Extended range
17	C+	C+	all	all	*SSI Max Limit* (VME and P2 error 0)
18	C+	C+	all	all	Test Control 0, *Create Test Signal*
19	C+	C+	all	all	Test Control 1, *Config 10m*
20	C+	-	-	-/all	Cyclic Error Compensation
21	C+	-	-	all	Control Register 2 *Aux Reg Enable*
22	C+	-	-	-/all	*CEC Error* (VME and P2 error 0)
23	C+	-	-	-/all	Diag FFT Control, *Data Source*
24	C+	-	-	-/all	Cyclic Error Diagnostics
25	C+	-	-	all	Sig RMS L2 register
26	C+	-	-	all	APD control registers and control bits (See Note 1)

Line	FW Src	4004 BC	4004 -09	4104/ 4104C	Product Firmware Features and Changes
		CE!		CE!	
		7402	7409	7601	**Firmware Version Register (hex)**
28	D+	-	all	all	Data Age Pos Direction bug fixed
29	D+	D+	all	all	Diag FFT Control readback
30	D+	D+	all	all	P2_IOE latch position extension
31	D+	D+	all	all	VME Write timing correction
32	D+	D+	all	all	Powerup reset improvements
33	E+	D+	all	B+	Overtemp and Ref errors in P2 err out
34	-	-	-	B+	Opt Power DC L2 register
35	F+	-	-	C+	APD Phase Comp Tables, Phase Comp Bias, Phase Comp Control, Phase Comp Diag registers
36	F+	D+	all	C+	SSI DAC, Bias DAC hang fixed
37	G,J+	D+	-	-	Data Age Backward Compatible option
38	G,J+	D+	all	D,F+	P2 serial 37 bit 1.60 µs
39	G,J+	D+	all	D,F+	Ref err is fatal err
40	G,J+	D+	all	D,F+	VME Position FIFO register
41	G,J+	D+	all	D,F+	Reset Finds Velocity fast mode
41	H+	-	-	-/E+	CEC Init Compete bug fixed
42	J+	E+	B+	F+	Disable Quick Reset
43	J+	E+	B+	F+	Overtemp alarm reset and local alarm 80°C
44	J+	E+	B+	F+	Reset failure threshold SSI < 0.5*SSI Squelch
45	J+	-	-	F+	Gain Set Error Diagnostic Registers (See Note 2)
46	J+	-	-	F+	Power Supply Error Diagnostic Registers (See Note 3)
47	J+	-	-	F+	APD Bias Calculation Improvement to SigRMS Mode (See Note 4)
48	J+	-	-	F+	Master/Slave communication bug fixes (See Note 5).

Note 1: The ZMI 4100 has the following register changes for APD control:

New registers:
APD Bias DAC
Control Register 5
Test Status 2
P2 Error Clear 2, P2 Error Status 2, P2 Interrupt Enable 2
VME Error Clear 2, VME Error Status 2, VME Interrupt Enable 2
Aux Registers (0x180-0x1FE) *Kit Version, Kit Revision, Software Version, Software Revision, Software Detail, MB APD Error Code, MB APD Gain Set, MB APD Opt Pwr Set, MB APD Sig RMS Set, MB Opt Power, MB Sig RMS Min, MB Sig RMS Max, MB Sig RMS Min Limit, MB Sig RMS Max Limit, MB Opt Power Min, MB Opt Power Max.*

New register bits:
Status Register 1 *Cmd Busy*, *Bias Calc Busy*
Status Register 0 *APD Init Complete*
P2 Command Register, VME Command Register *Start Bias Calc*
Test Command 1 *Reset Controller*
Test Control 1 *Bias Supply Enab, Bias Supply Test, Bias Supply Override*
Test Command 0 *Reset Opt Power Min/Max, Reset Sig RMS Min/Max*

Note 2 (Microcontroller software SPM8020-9277-01 Rev H):
The ZMI 4100 has the following registers to assist in diagnosing errors related to setting APD gain for SigRMS Adjust, Constant Optical Power and Constant Gain Modes:

GSE Target Gain
GSE Actual Gain
GSE SigRMS Gain
GSE MeasDC Low
GSE MeasDC High

Note 3 (Microcontroller software SPM8020-9277-01 Rev H):
The ZMI 4100 has the following registers to assist in diagnosing errors related to the power supply errors:

PSD LVPS Error ID
PSD LVPS First Err V
PSD LVPS First Err Max V
PSD LVPS First Err Min V
PSD LVPS First Err VCC In
PSD VCC In Fault V
PSD VCC In Max V
PSD VCC In Min V
PSD HVPS Error
PSD HV Bias Err Meas
PSD HV Bias Err Exp

Note 4 (Microcontroller software SPM8020-9277-01 Rev H):
APD Bias Calculation Improvement to SigRMS Mode.
The SigRMS calibration was changed to wait for gain to be within 50 L2 counts rather than wait for a specified delay. The calibration timeout is set to 300 ms, coinciding with the issue of the *Start Bias Calc* command in the VME Command register to the receipt of *Bias Calc Complete* in Error Register 2. If the gain is not achieved for either initial default or target gain within 300 ms, a *Gain Set Error* (GSE) bit is set in the APD Error Code Register and the *Bias Error* is set in Error Register 2.

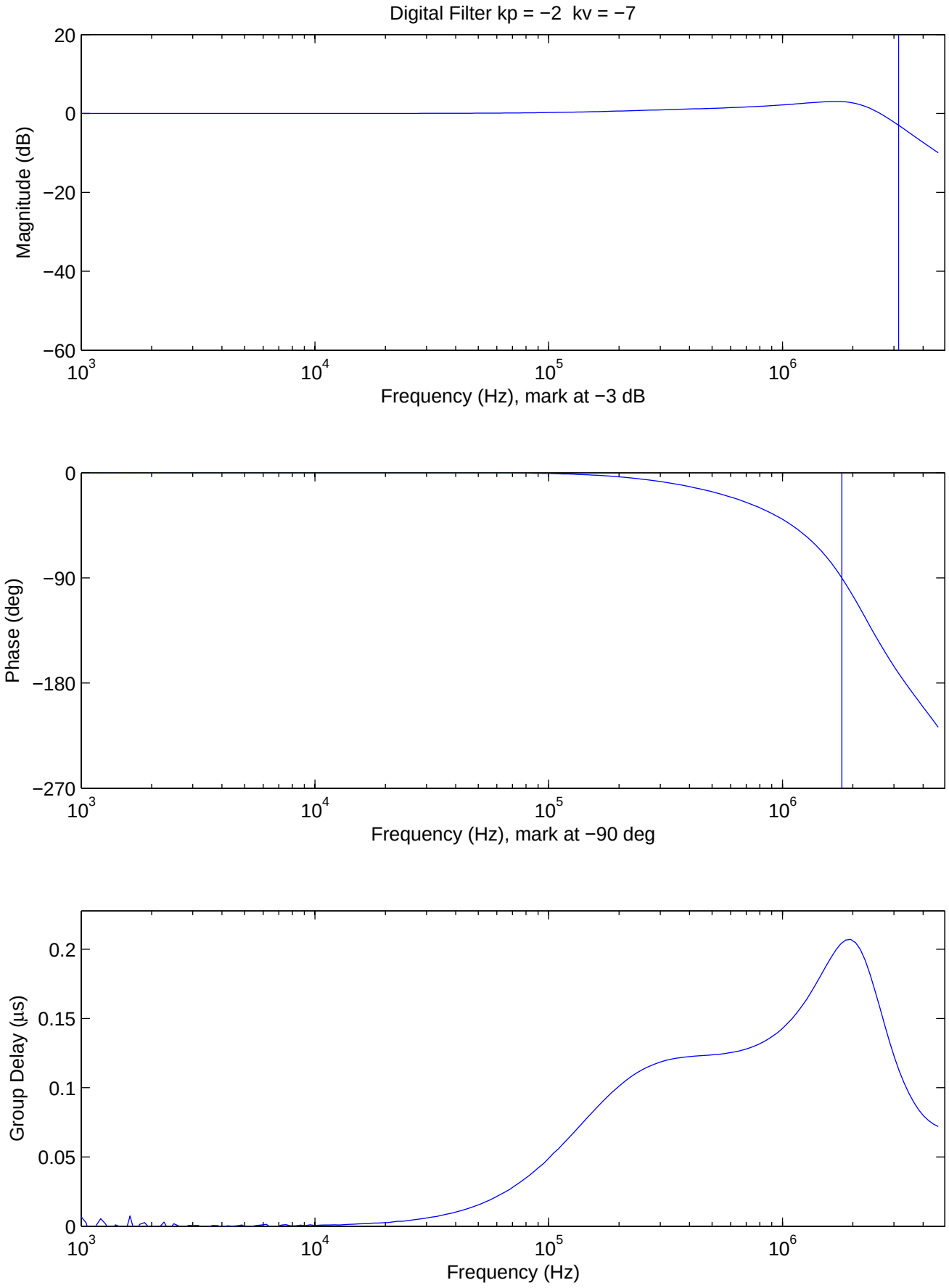
Note 5 (Microcontroller software SPM8020-9277-01 Rev J):
Some APD power errors were falsely reported. The communication between microcontrollers in the master and slave FPGA was revised to correct this and several related problems.

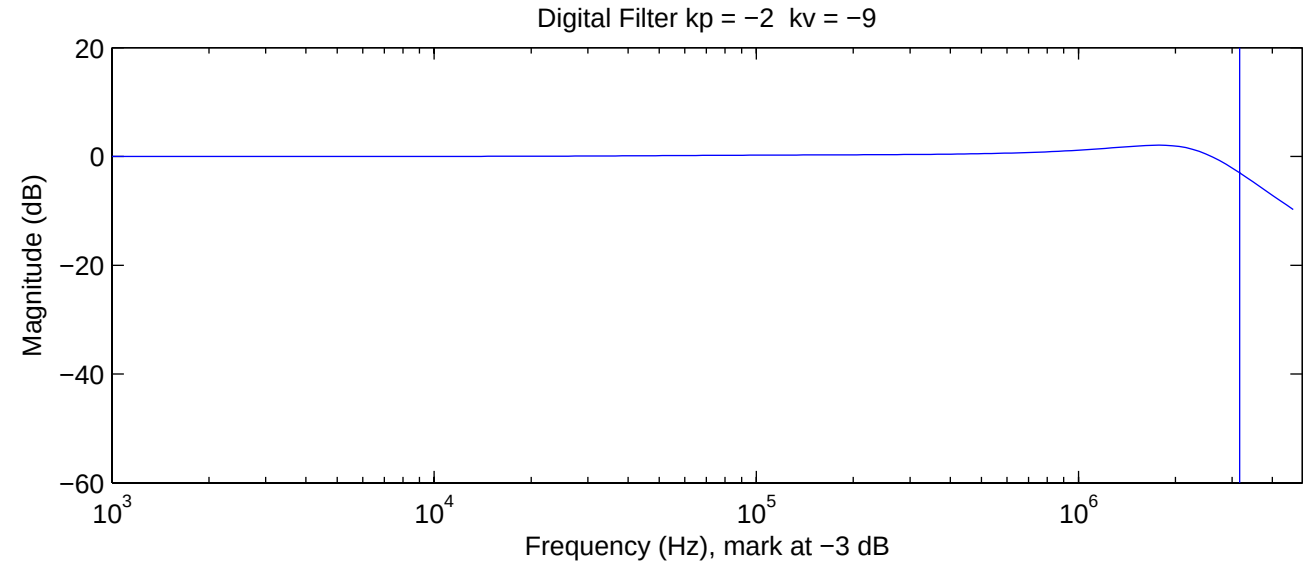
Reference Digital Filter Performance

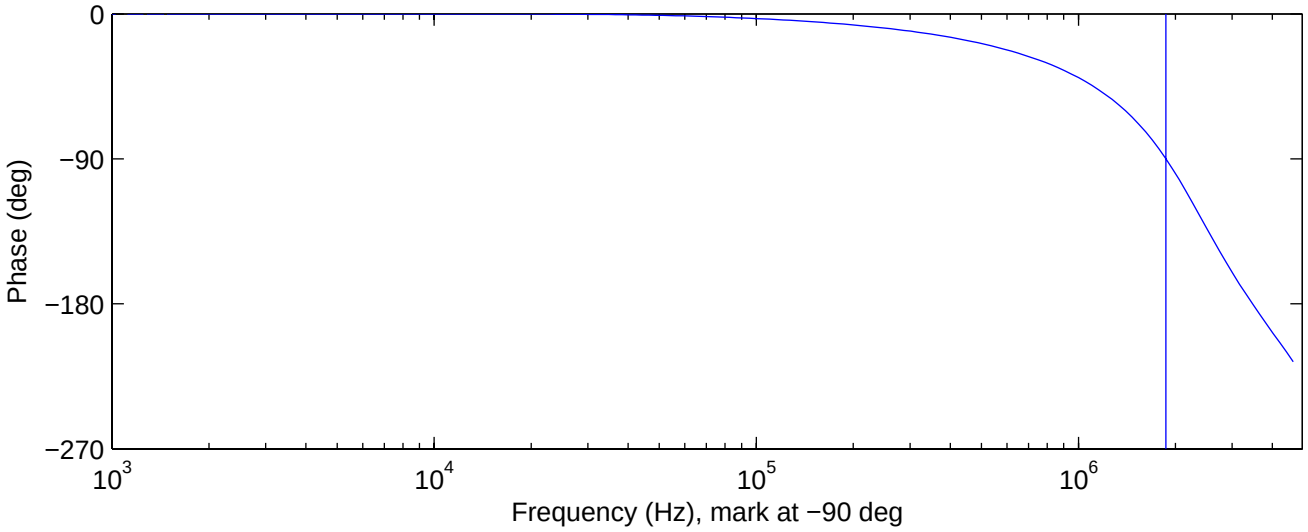
This reference contains graphs of digital filter performance for each filter setting (Kp and Kv). Each page corresponds to one filter setting and contains three graphs.

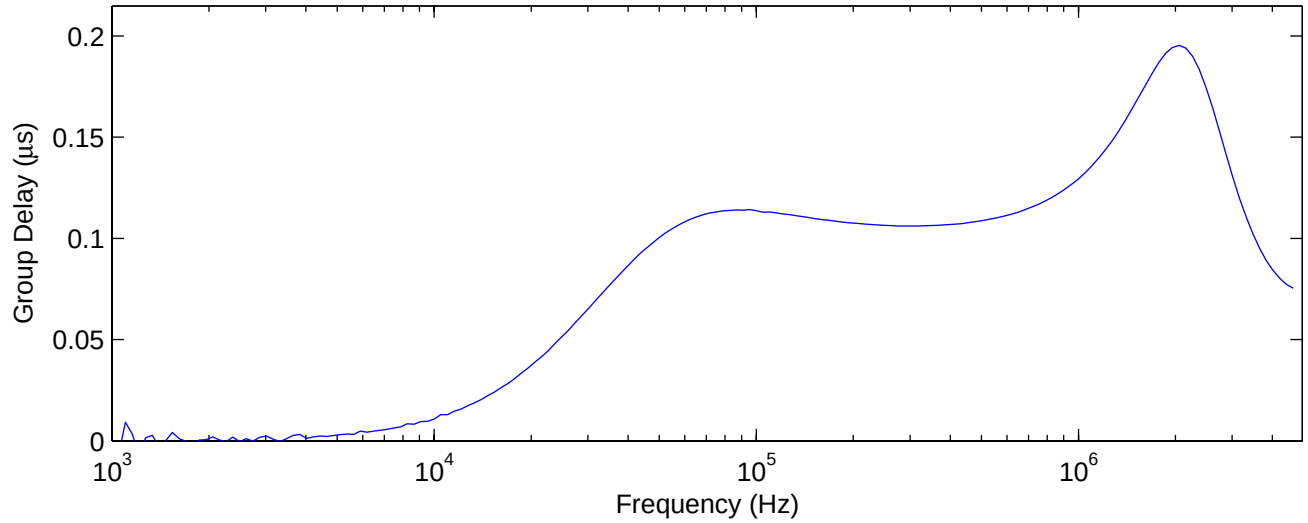
Graph	*Description*
Magnitude vs Frequency	Indicates how variations in the measured position are attenuated at higher frequencies.
Phase vs Frequency	This is the phase of the digital filter transfer function.
Group Delay vs Frequency	This is the group delay of the digital filter versus frequency. Group Delay is calculated as $-d\phi/dF$, and represents the delay of a signal passing through the filter.

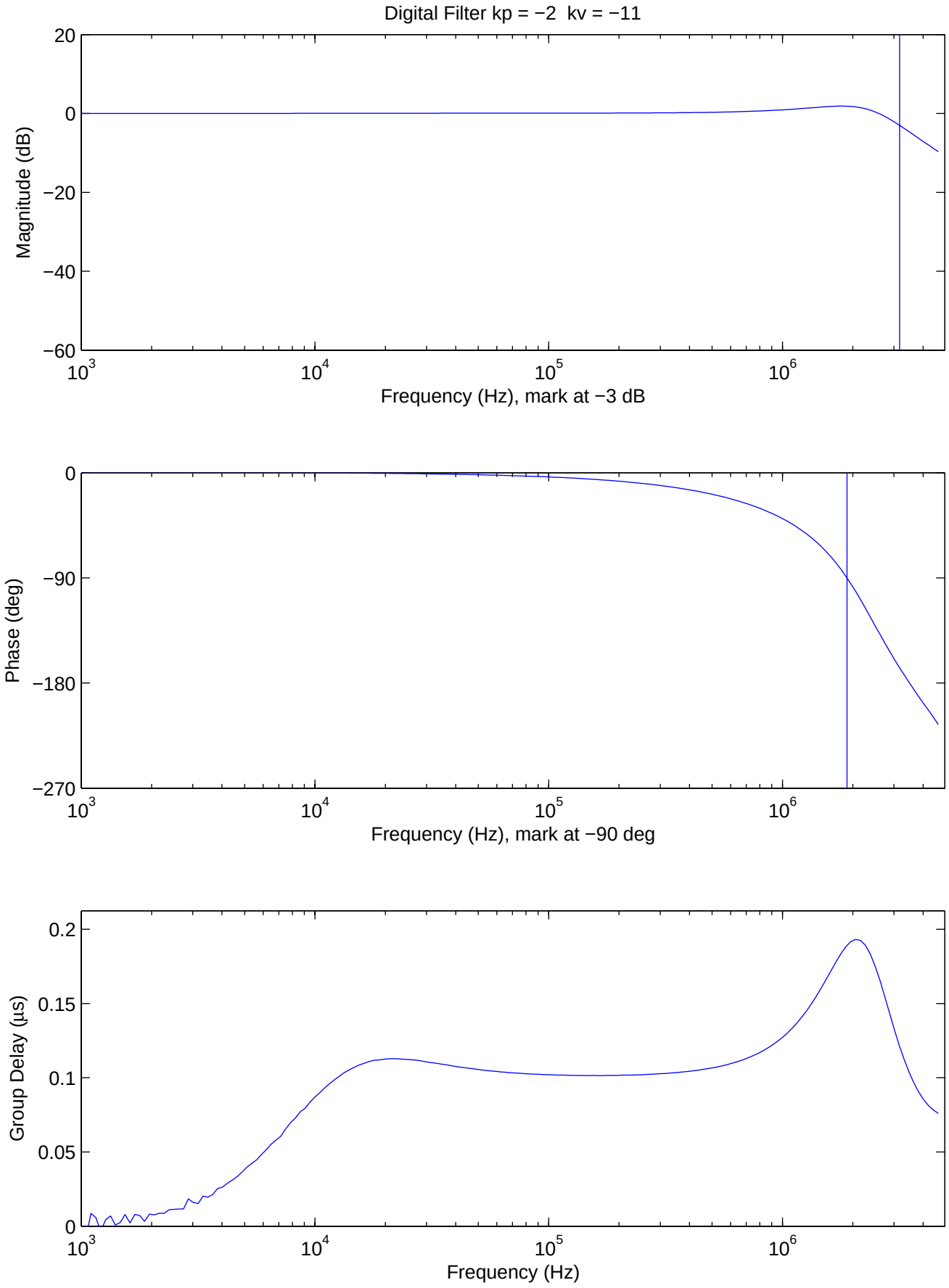
Digital Filter Graphs *page*

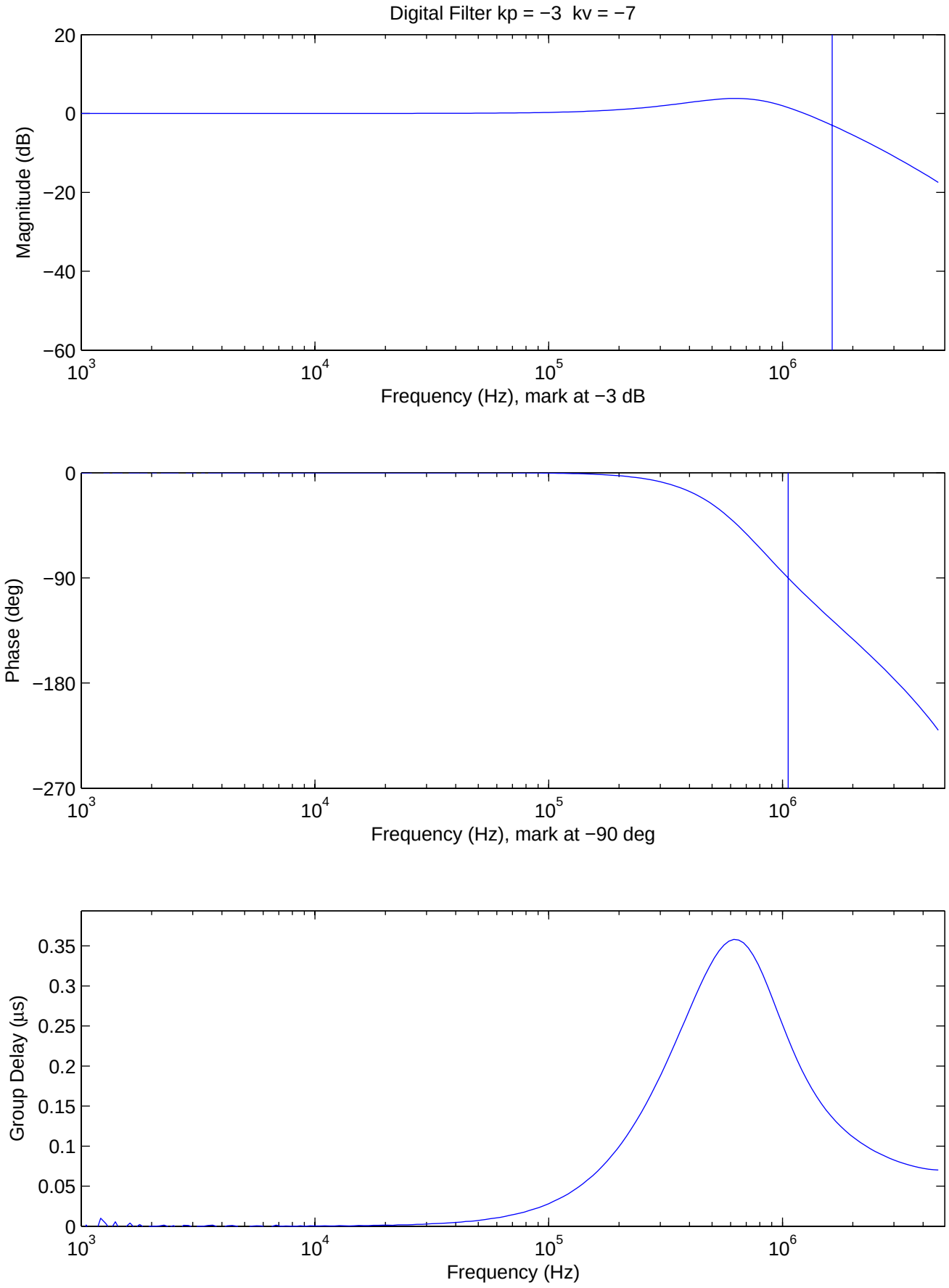

Digital Filter kp = −2 kv = −7
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.2
0.15
0.1
0.05
0
Frequency (Hz)

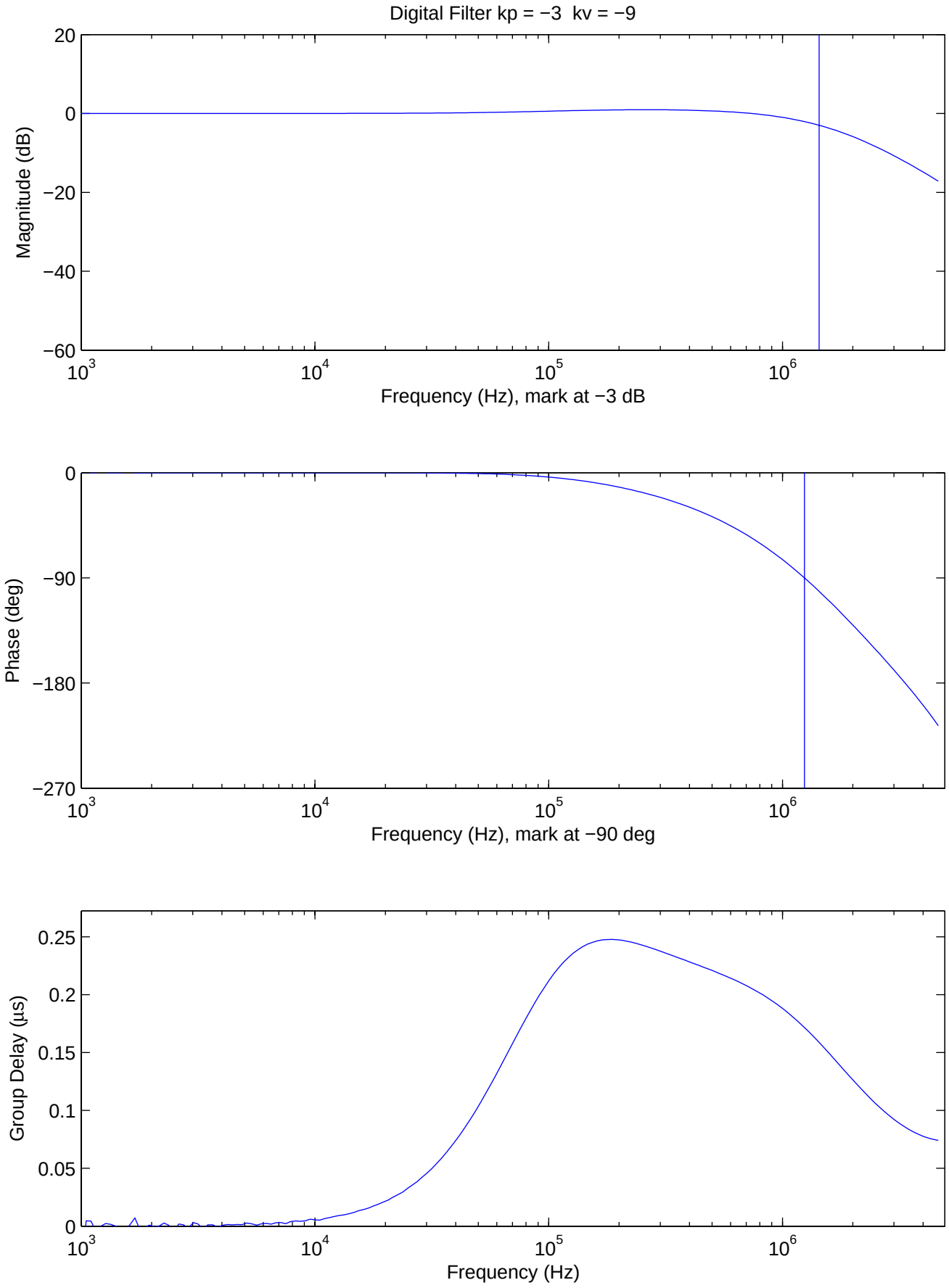

Digital Filter kp = −2 kv = −9
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB

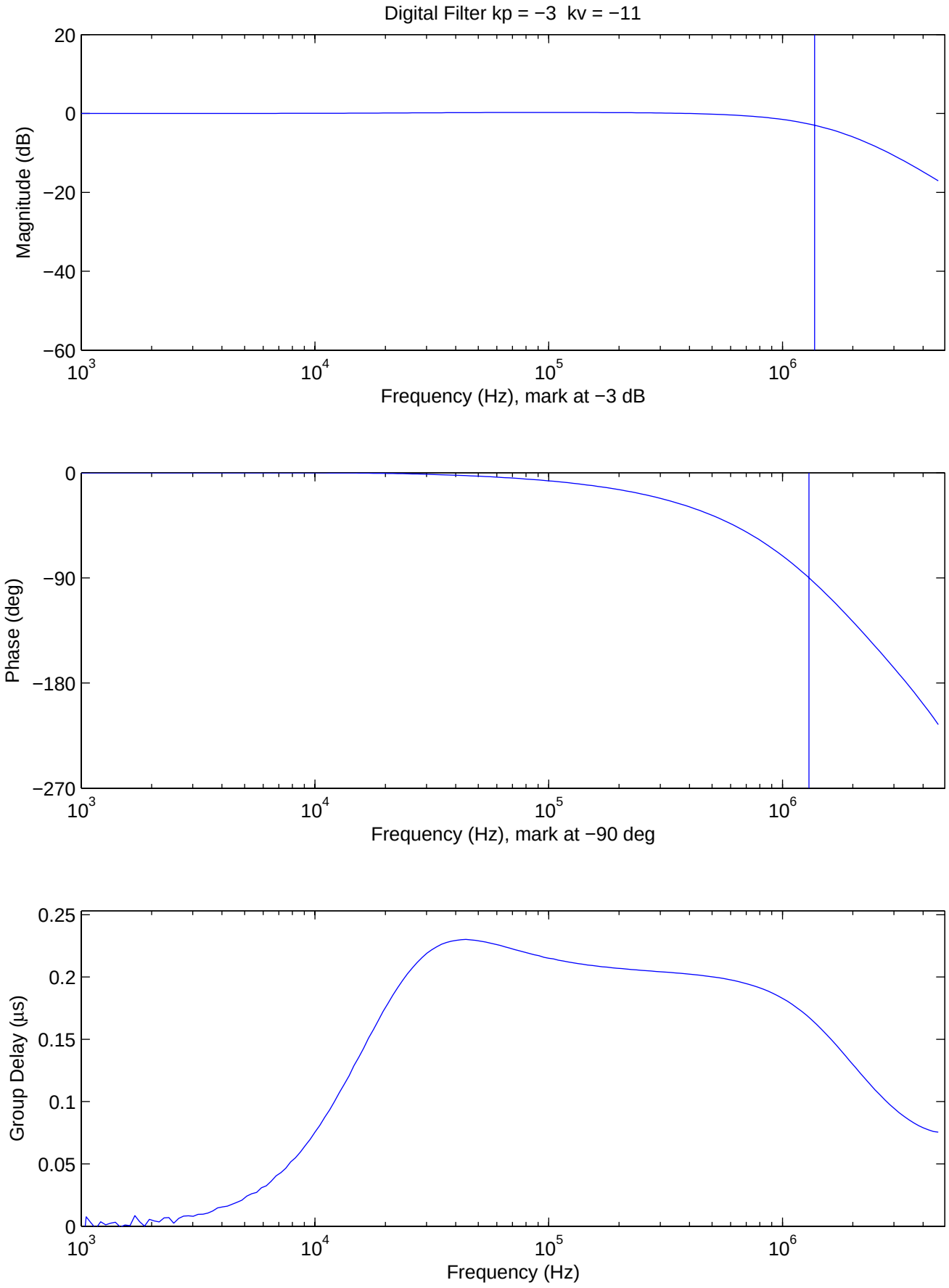

Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg

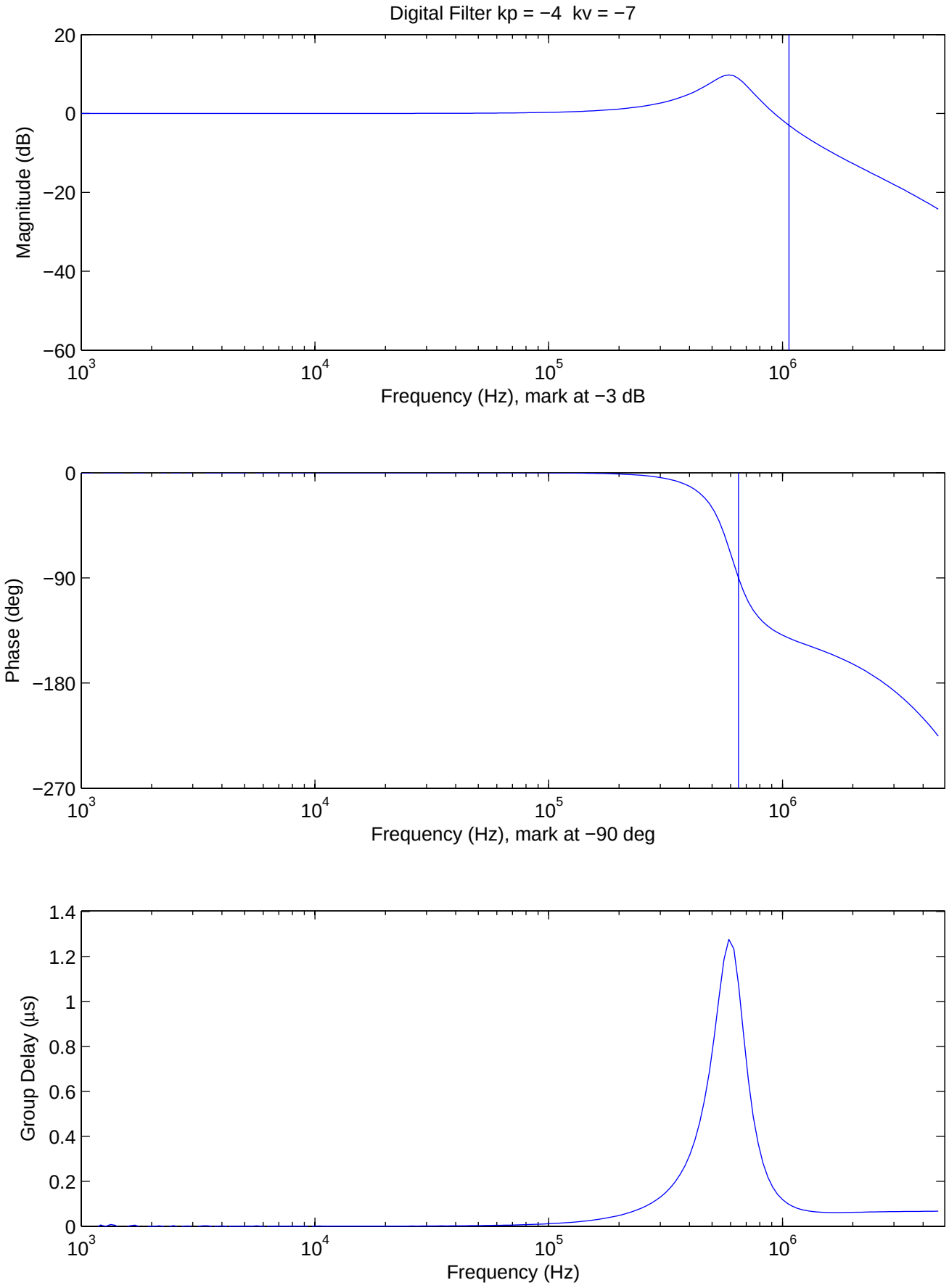

Group Delay (µs)
0.2
0.15
0.1
0.05
0
10^3
10^4
10^5
10^6
Frequency (Hz)

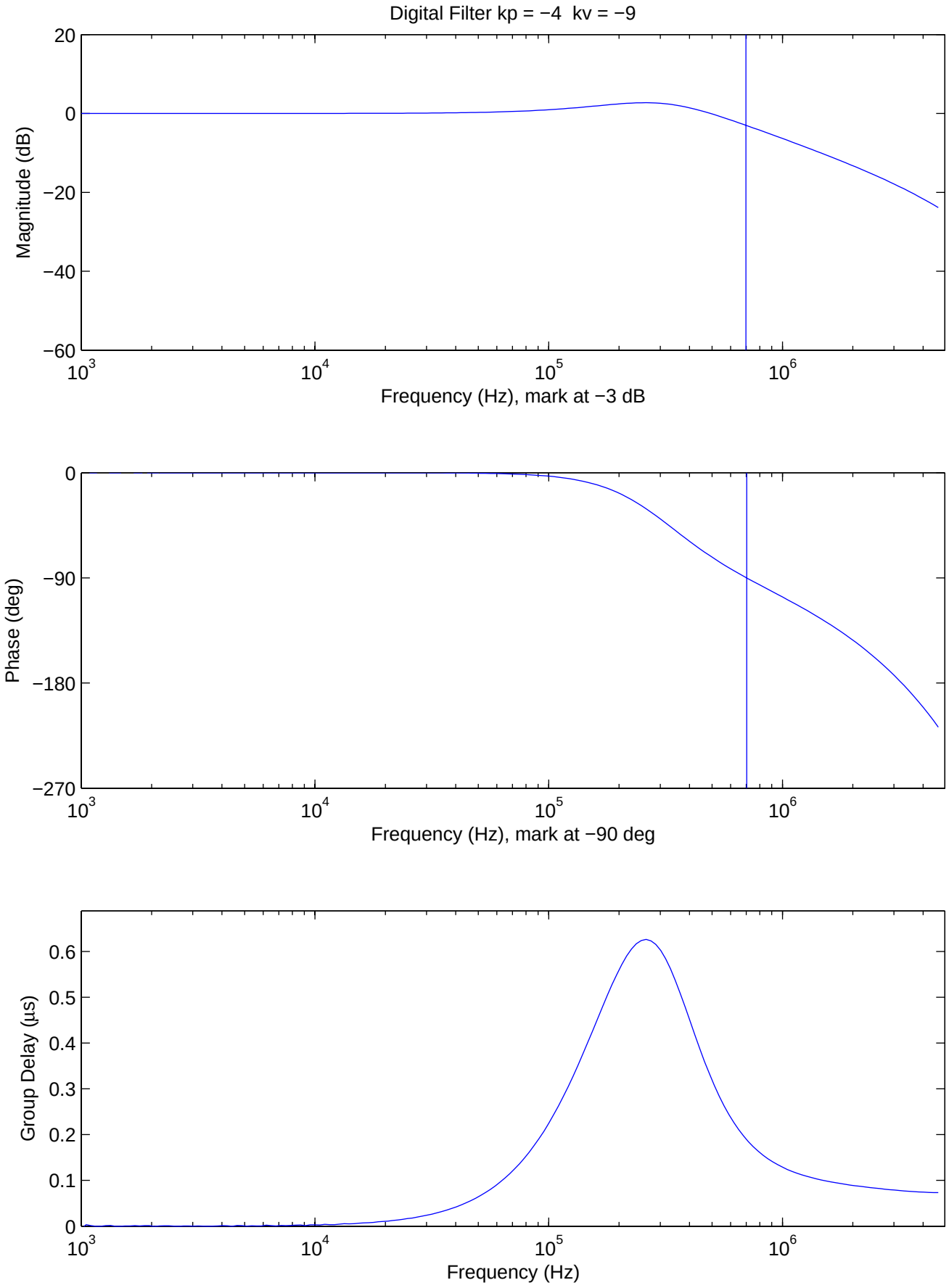

Digital Filter kp = −2 kv = −11
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.2
0.15
0.1
0.05
0
10^3
10^4
10^5
10^6
Frequency (Hz)

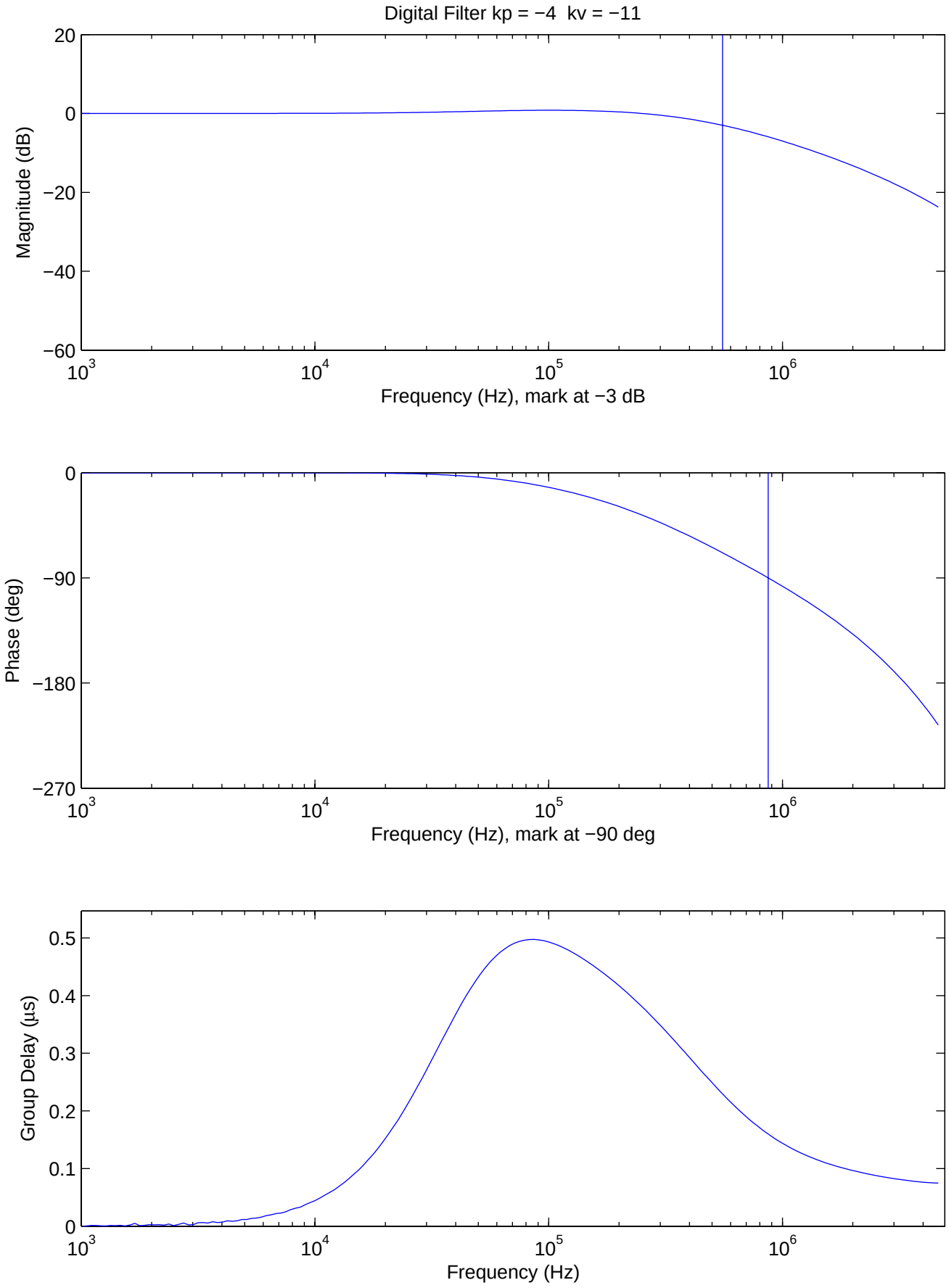

Digital Filter kp = −3 kv = −7
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
10^3
10^4
10^5
10^6
Frequency (Hz)

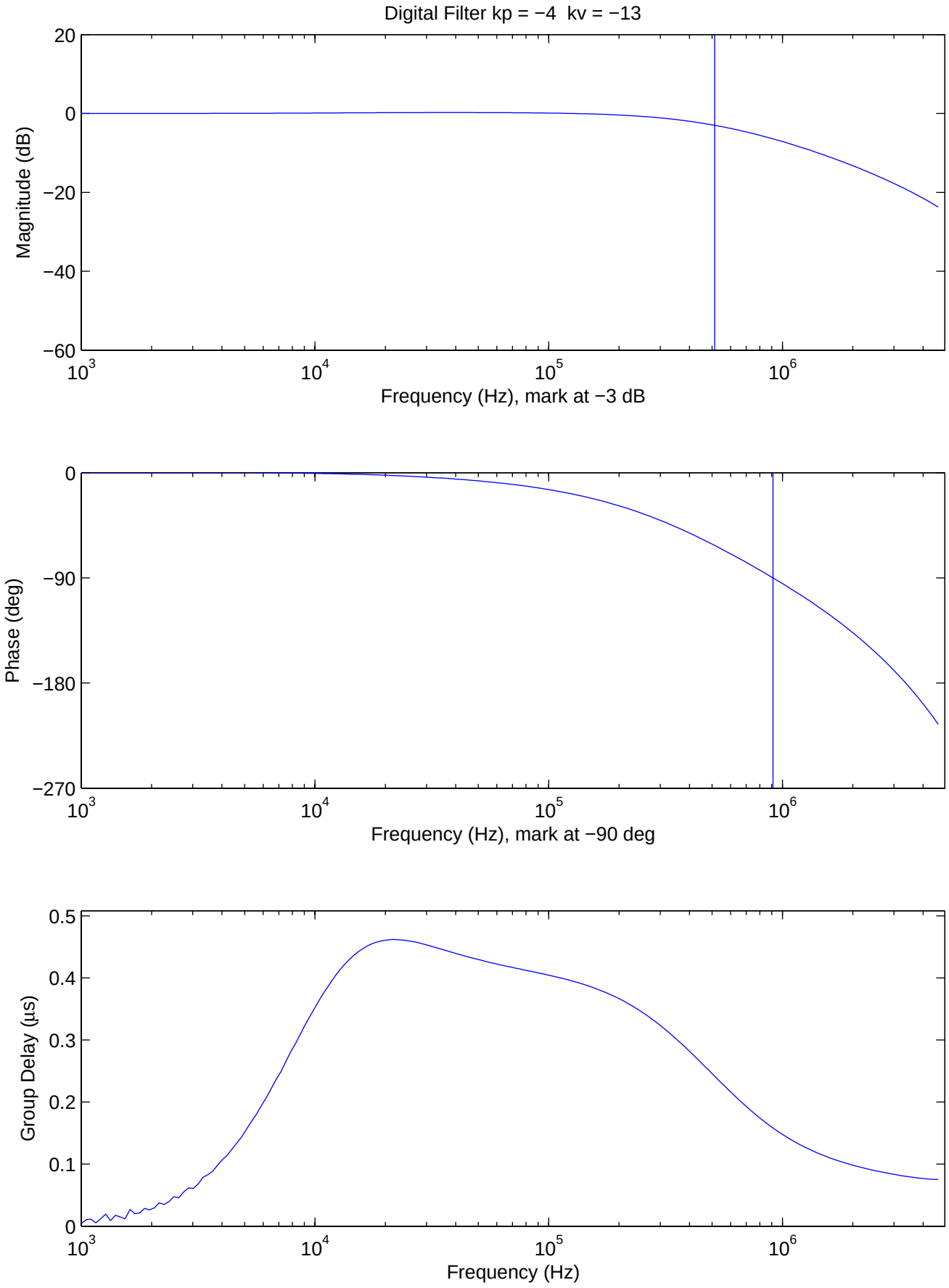

Digital Filter kp = −3 kv = −9
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.25
0.2
0.15
0.1
0.05
0
Frequency (Hz)

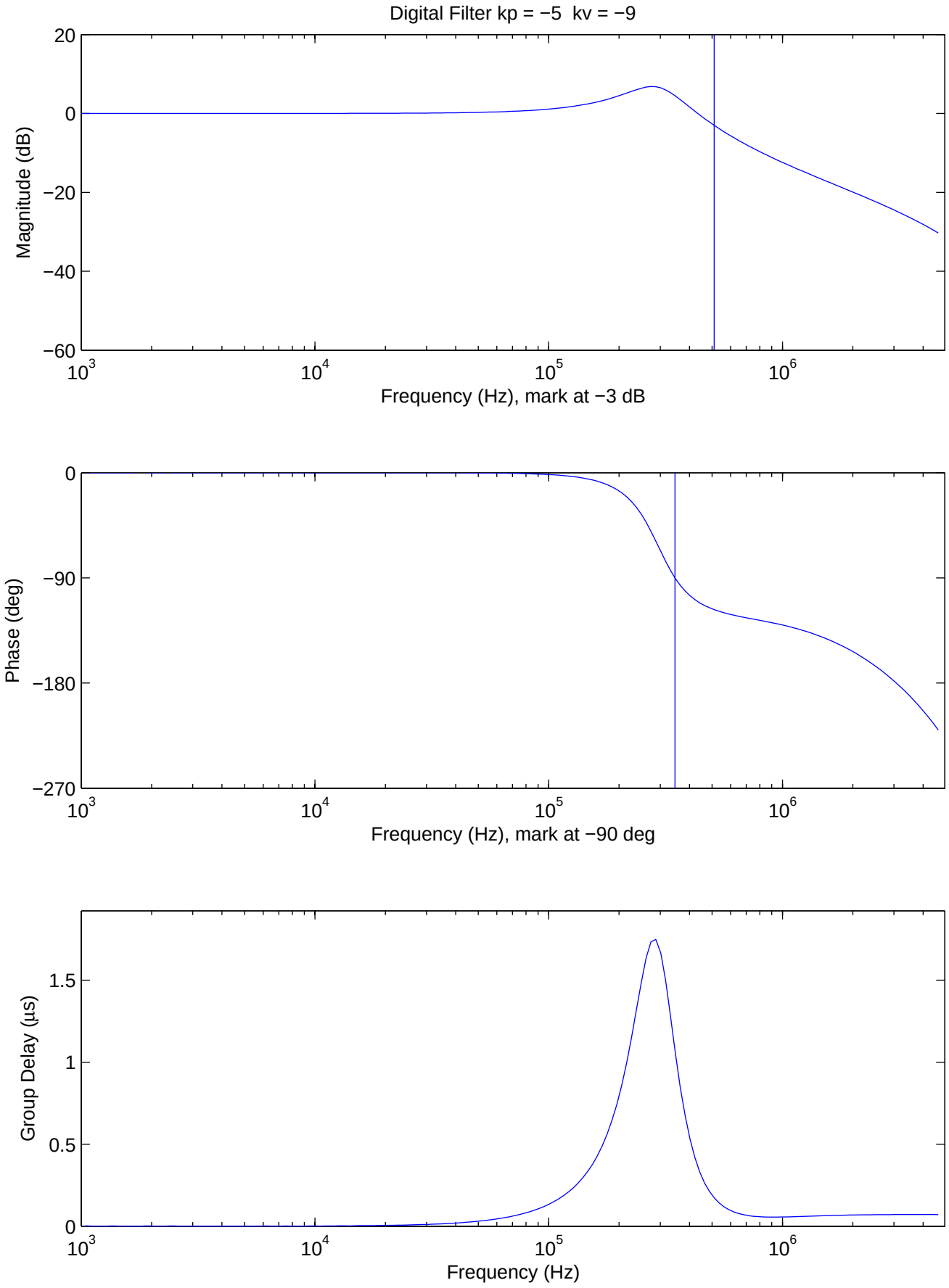

Digital Filter kp = −3 kv = −11
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.25
0.2
0.15
0.1
0.05
0
Frequency (Hz)

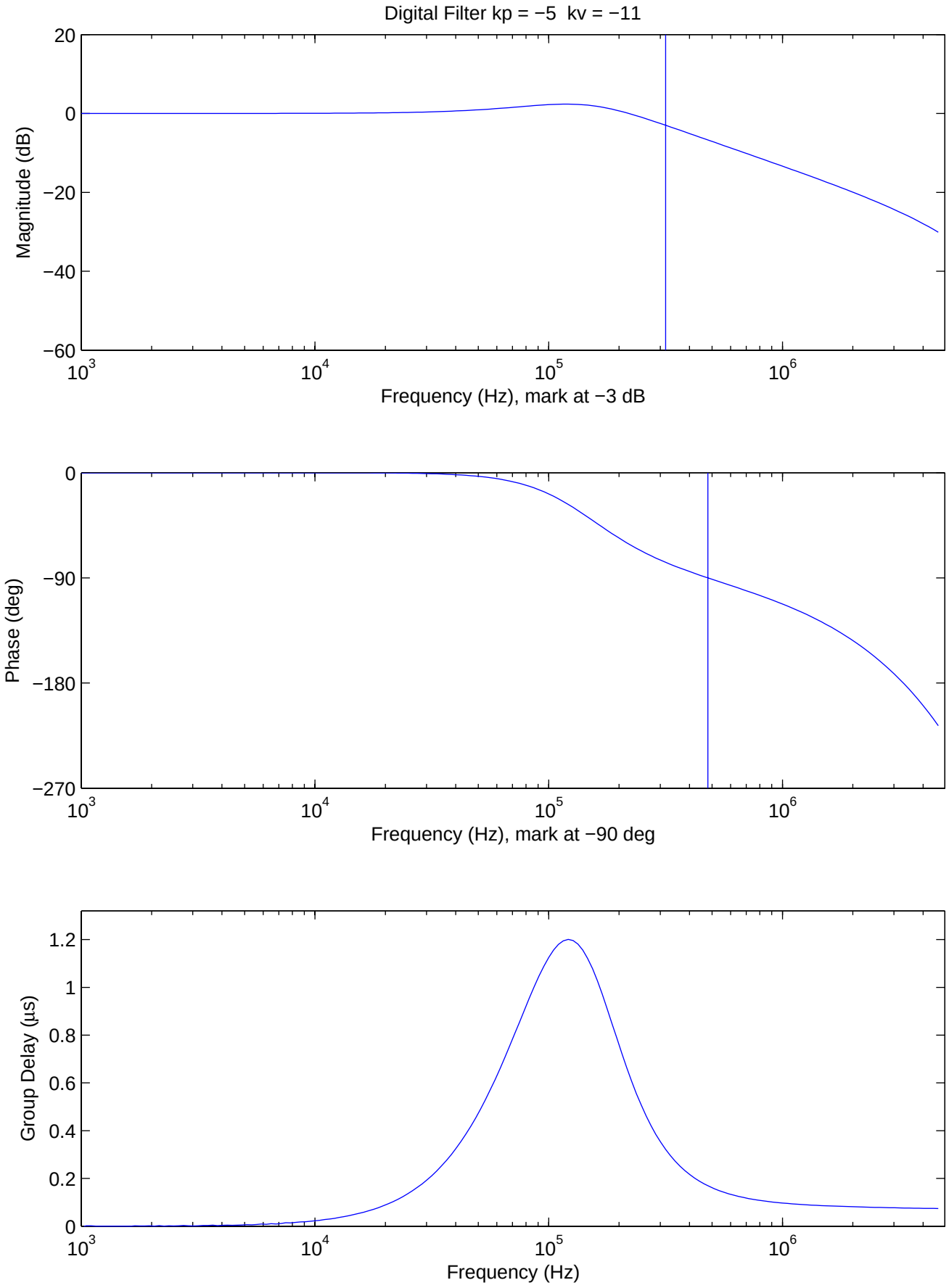

Digital Filter kp = −4 kv = −7
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
1.4
1.2
1
0.8
0.6
0.4
0.2
0
10^3
10^4
10^5
10^6
Frequency (Hz)

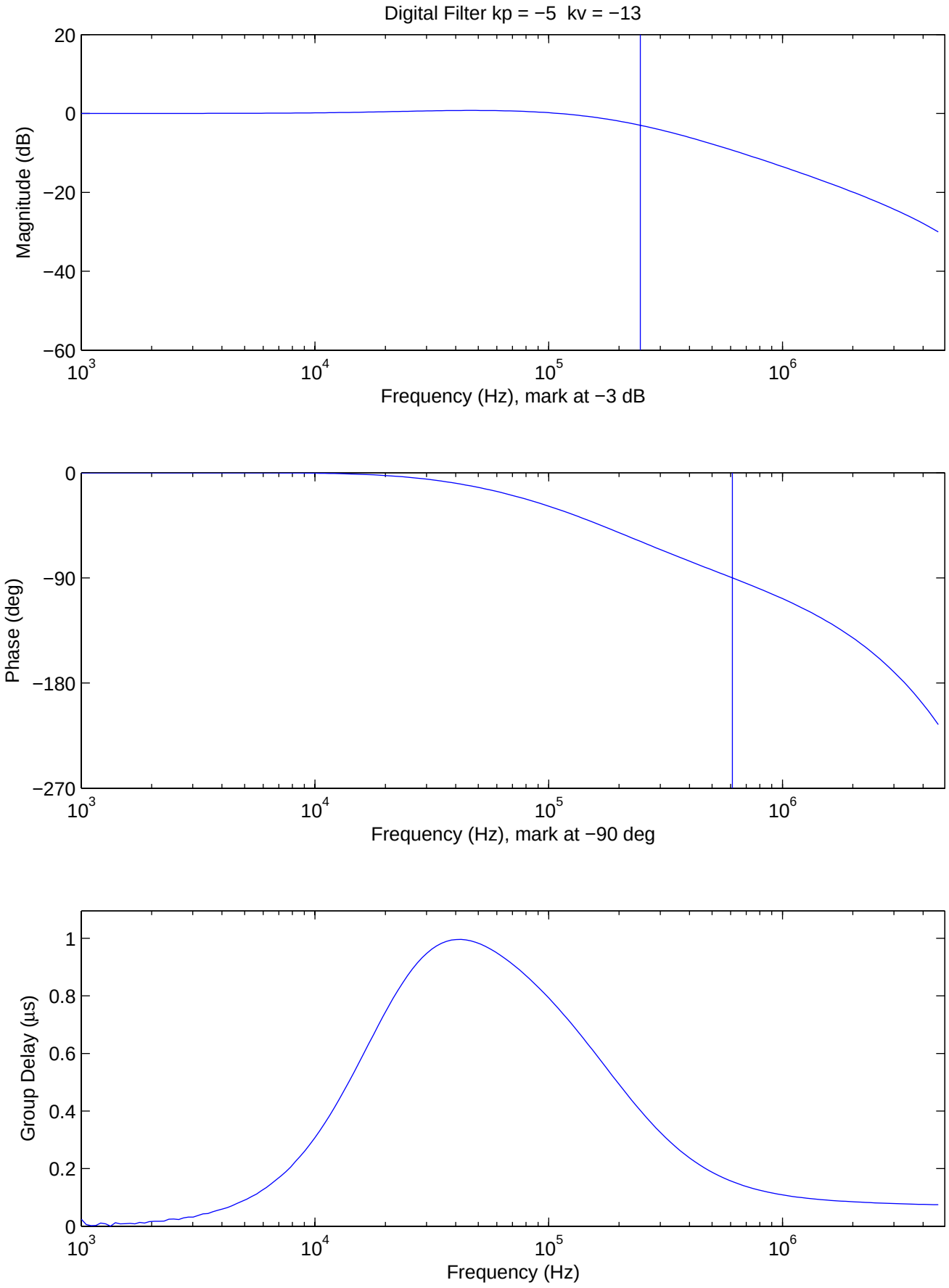

Digital Filter kp = −4 kv = −9
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.6
0.5
0.4
0.3
0.2
0.1
0
10^3
10^4
10^5
10^6
Frequency (Hz)

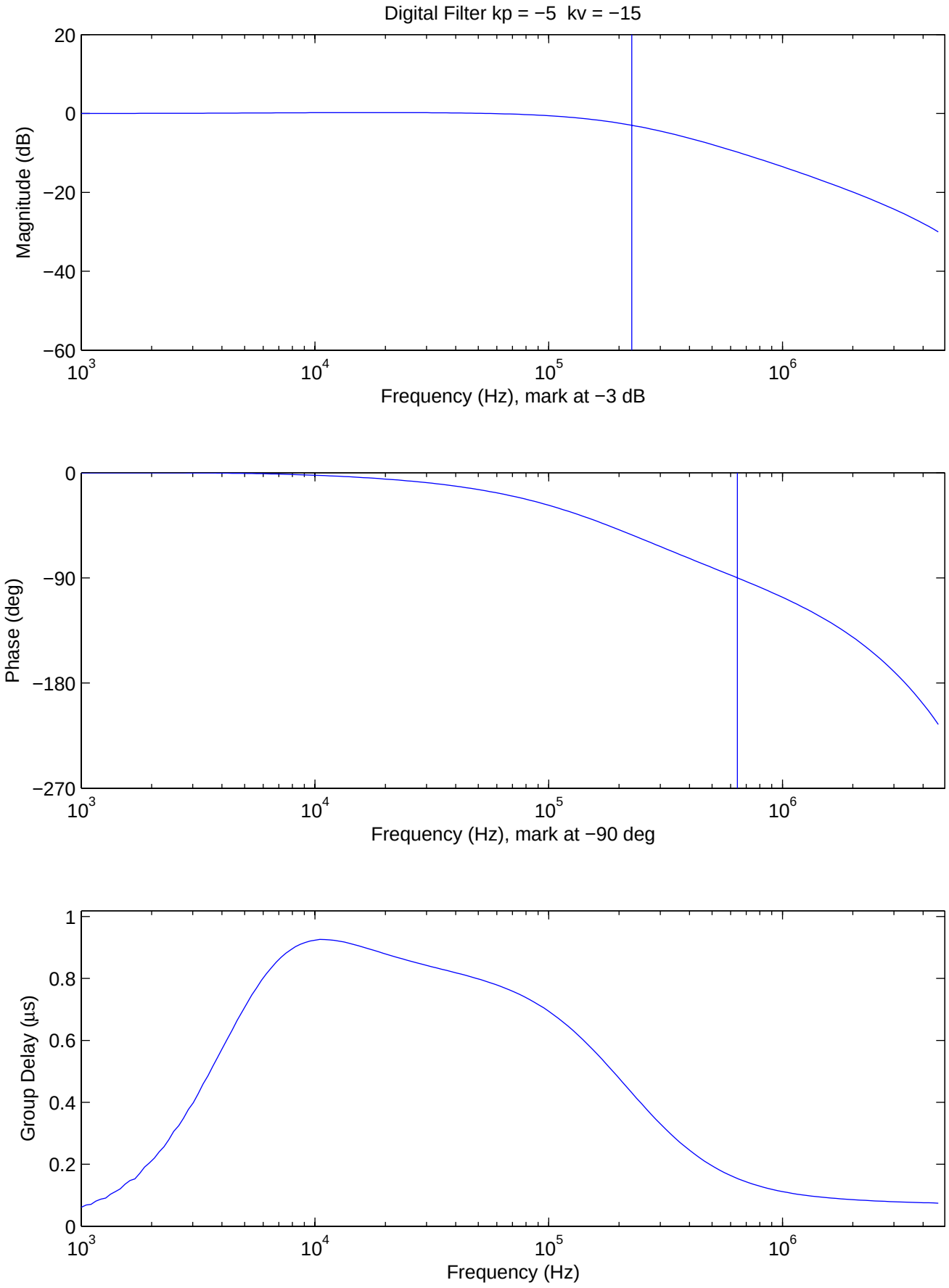

Digital Filter kp = −4 kv = −11
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.5
0.4
0.3
0.2
0.1
0
10^3
10^4
10^5
10^6
Frequency (Hz)

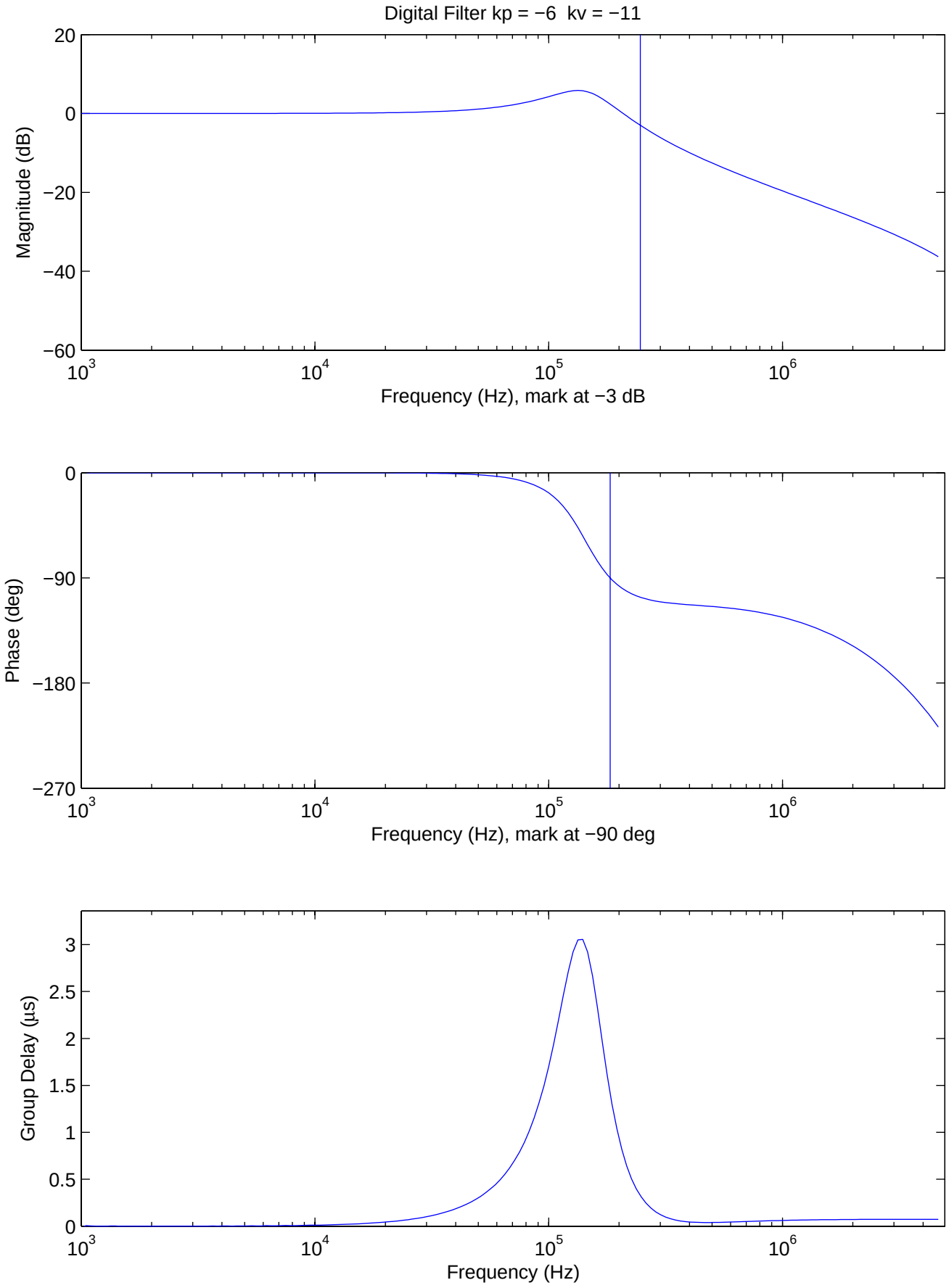

Digital Filter kp = −4 kv = −13
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
0.5
0.4
0.3
0.2
0.1
0
Frequency (Hz)

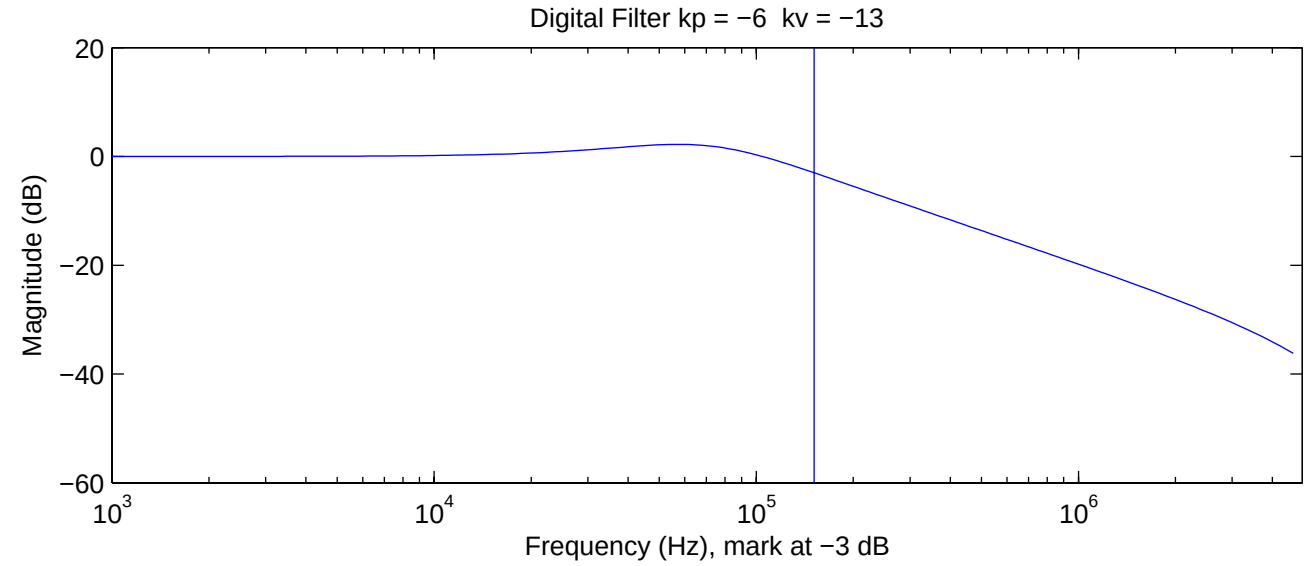

Digital Filter kp = −5 kv = −9
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
1.5
1
0.5
0
Frequency (Hz)

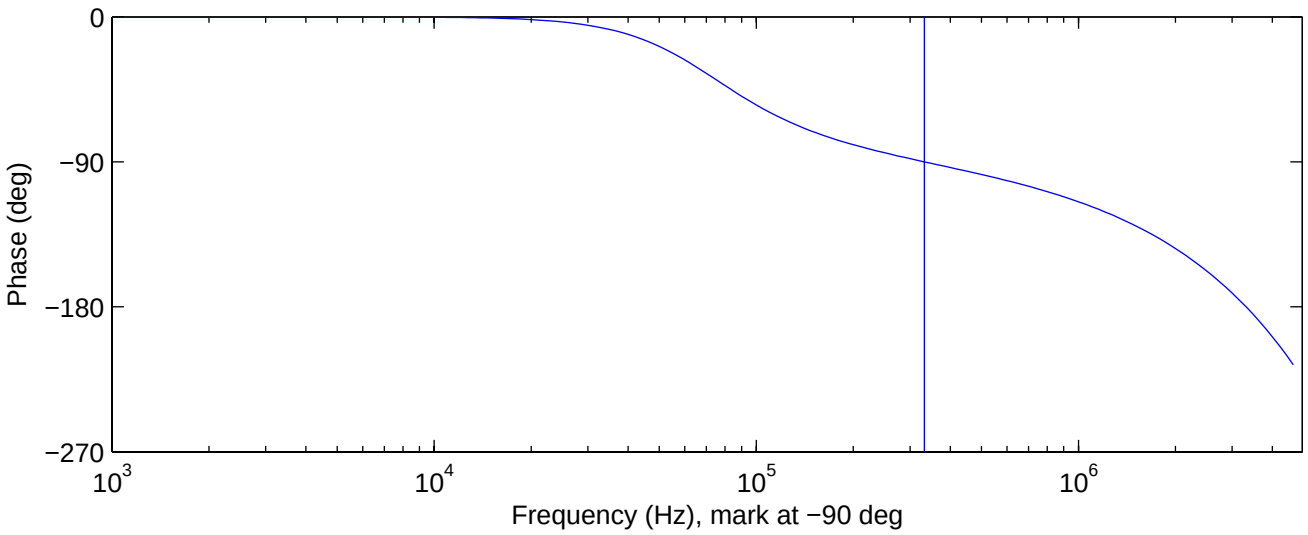

Digital Filter kp = −5 kv = −11
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
1.2
1
0.8
0.6
0.4
0.2
0
10^3
10^4
10^5
10^6
Frequency (Hz)

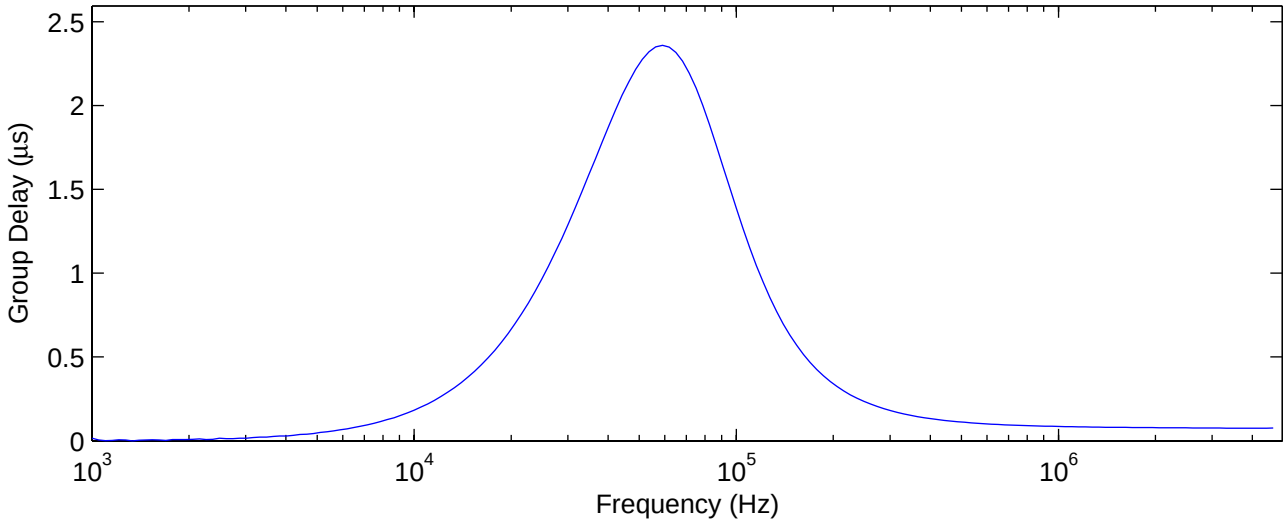

Digital Filter kp = −5 kv = −13
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
1
0.8
0.6
0.4
0.2
0
10^3
10^4
10^5
10^6
Frequency (Hz)

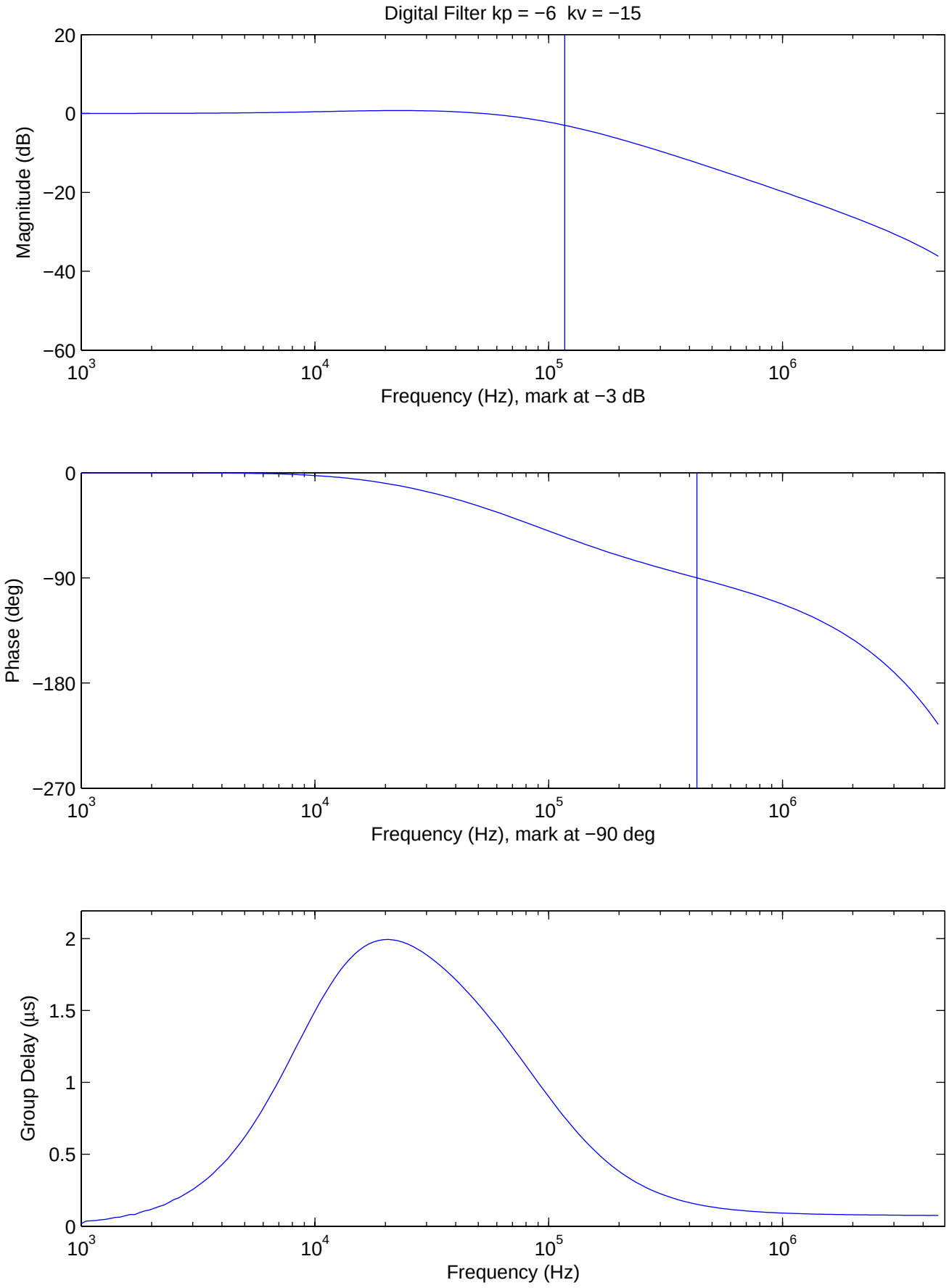

Digital Filter kp = −5 kv = −15
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
1
0.8
0.6
0.4
0.2
0
10^3
10^4
10^5
10^6
Frequency (Hz)

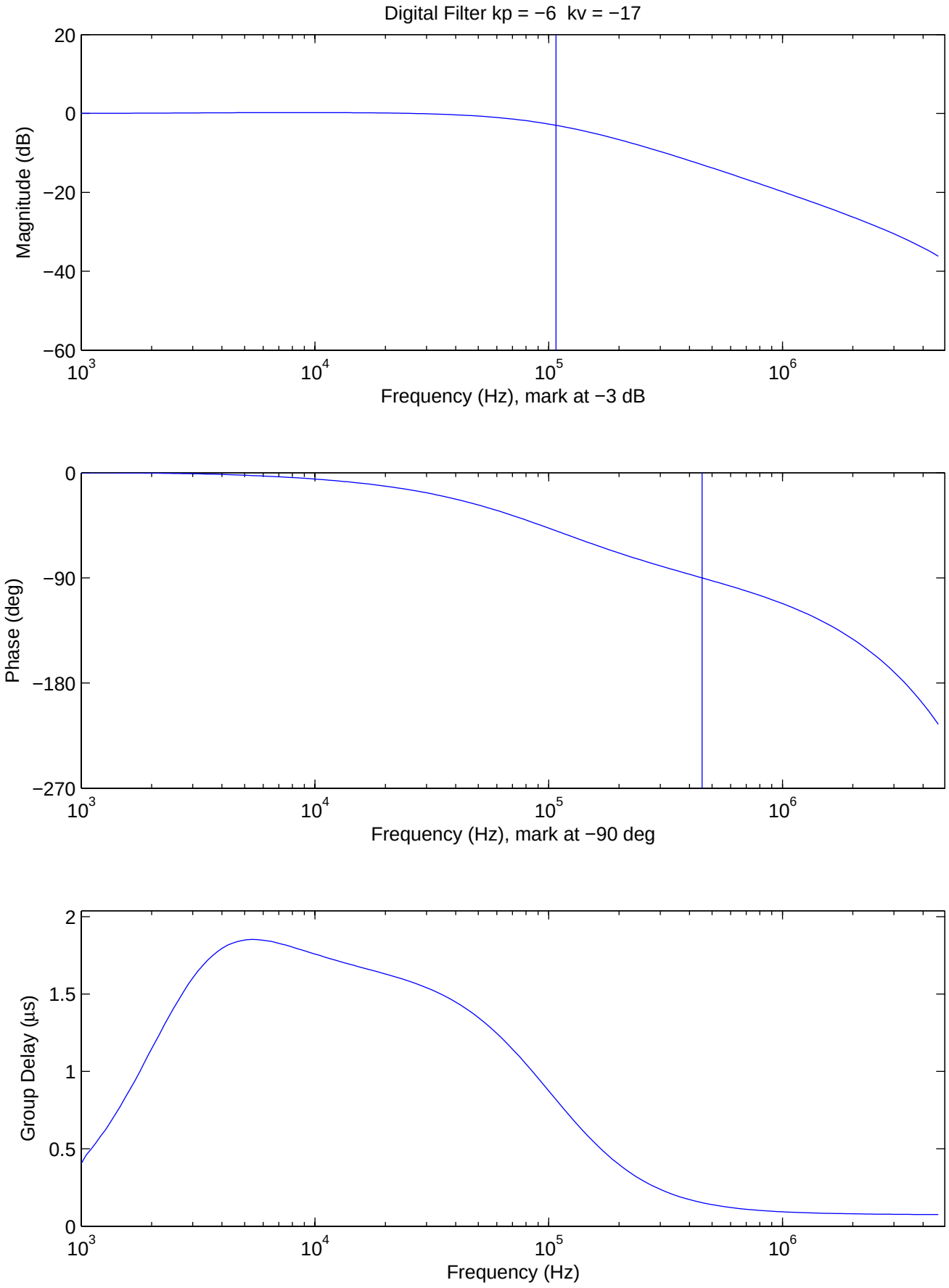

Digital Filter kp = −6 kv = −11
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
3
2.5
2
1.5
1
0.5
0
Frequency (Hz)

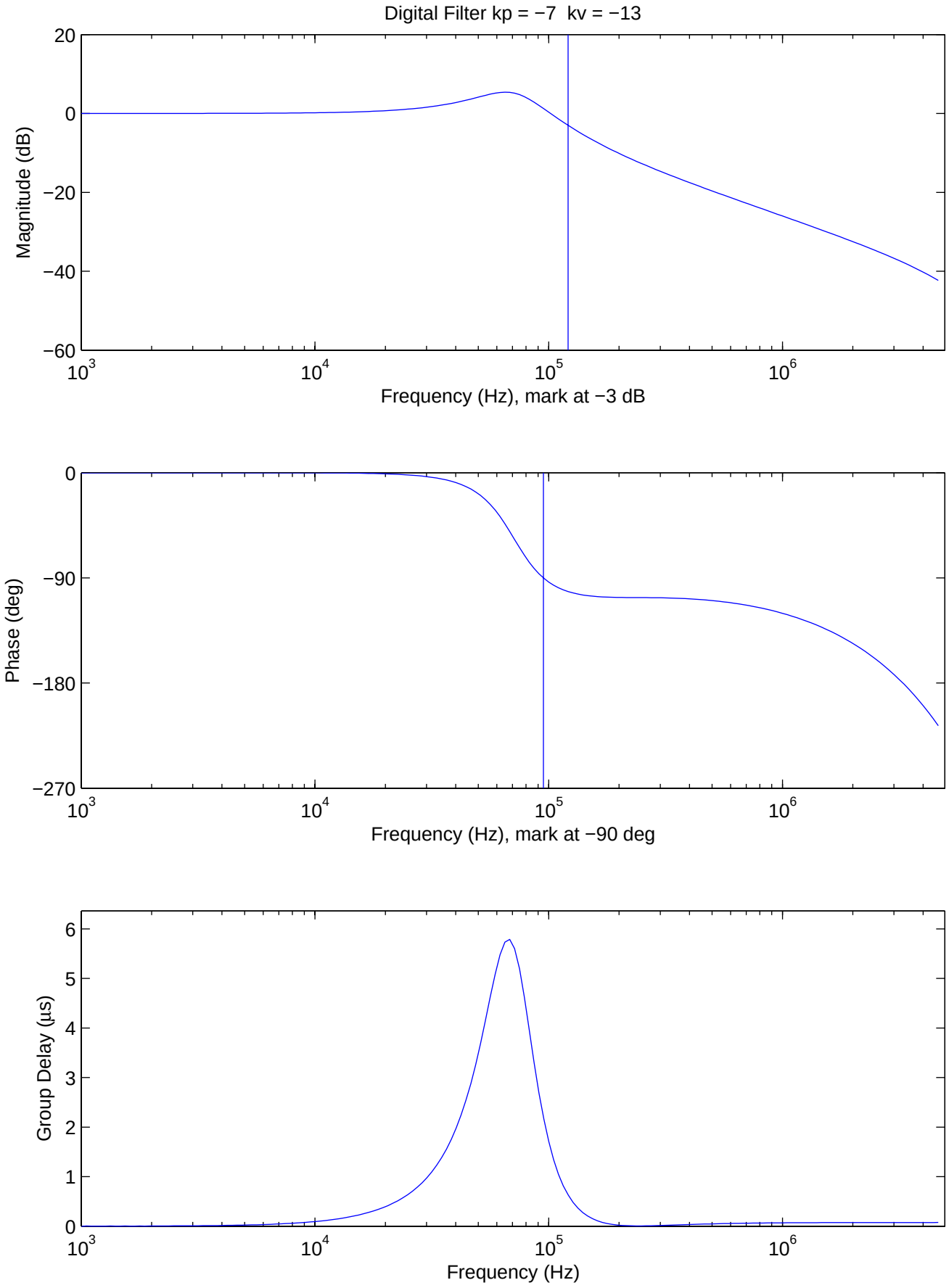

Digital Filter kp = −6 kv = −13
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB

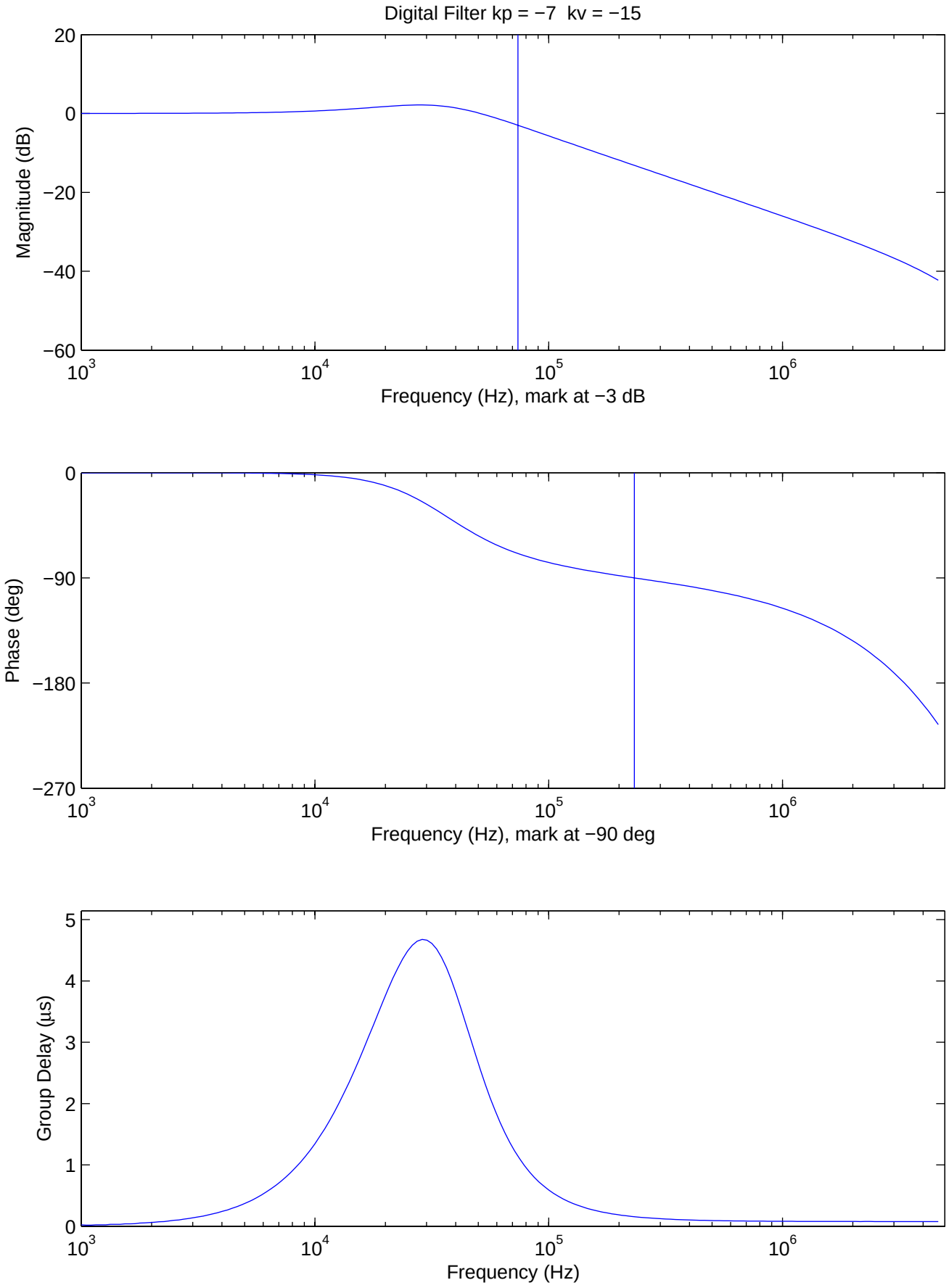

Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg

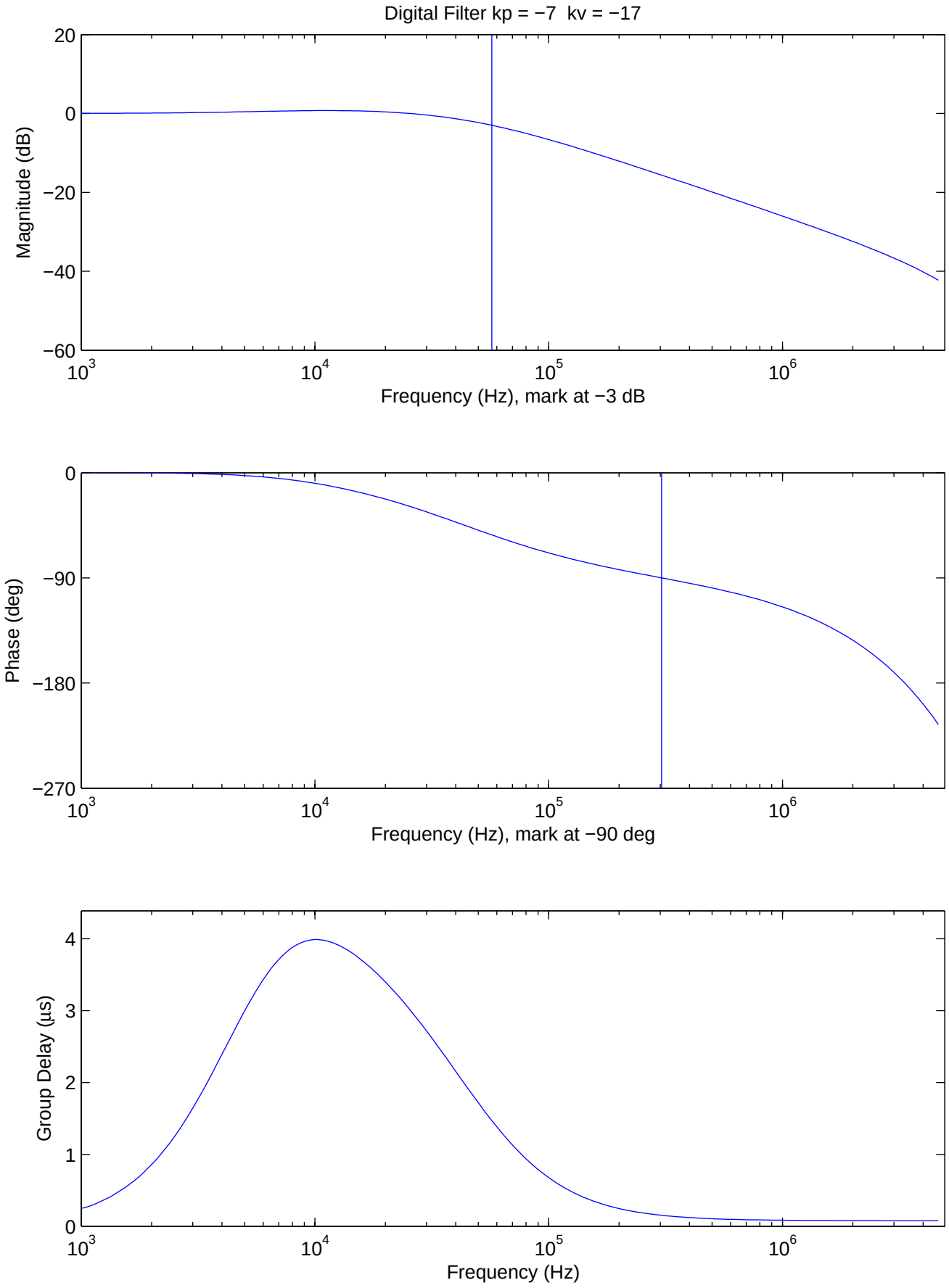

Group Delay (µs)
2.5
2
1.5
1
0.5
0
10^3
10^4
10^5
10^6
Frequency (Hz)

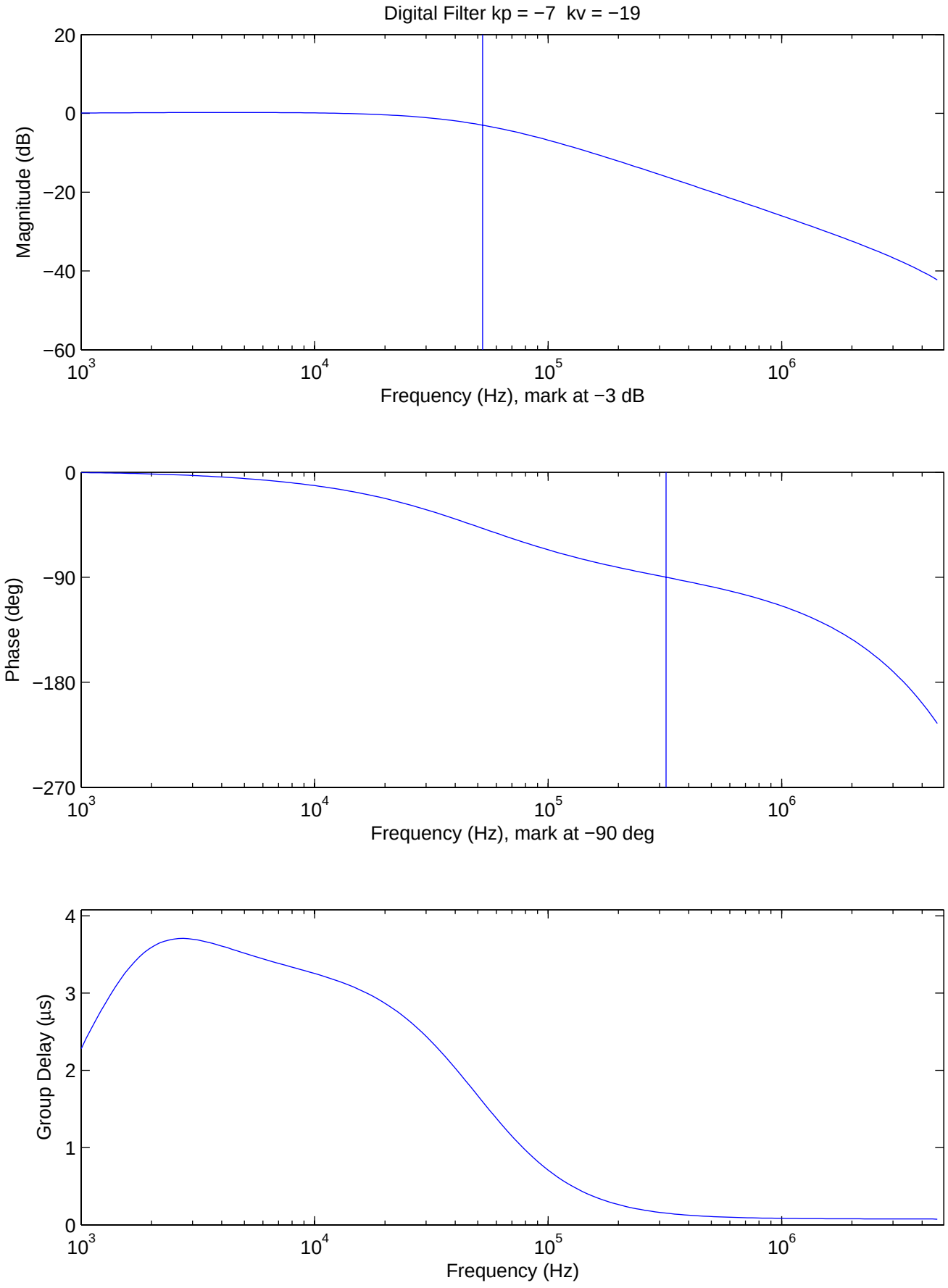

Digital Filter kp = −6 kv = −15
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
2
1.5
1
0.5
0
Frequency (Hz)

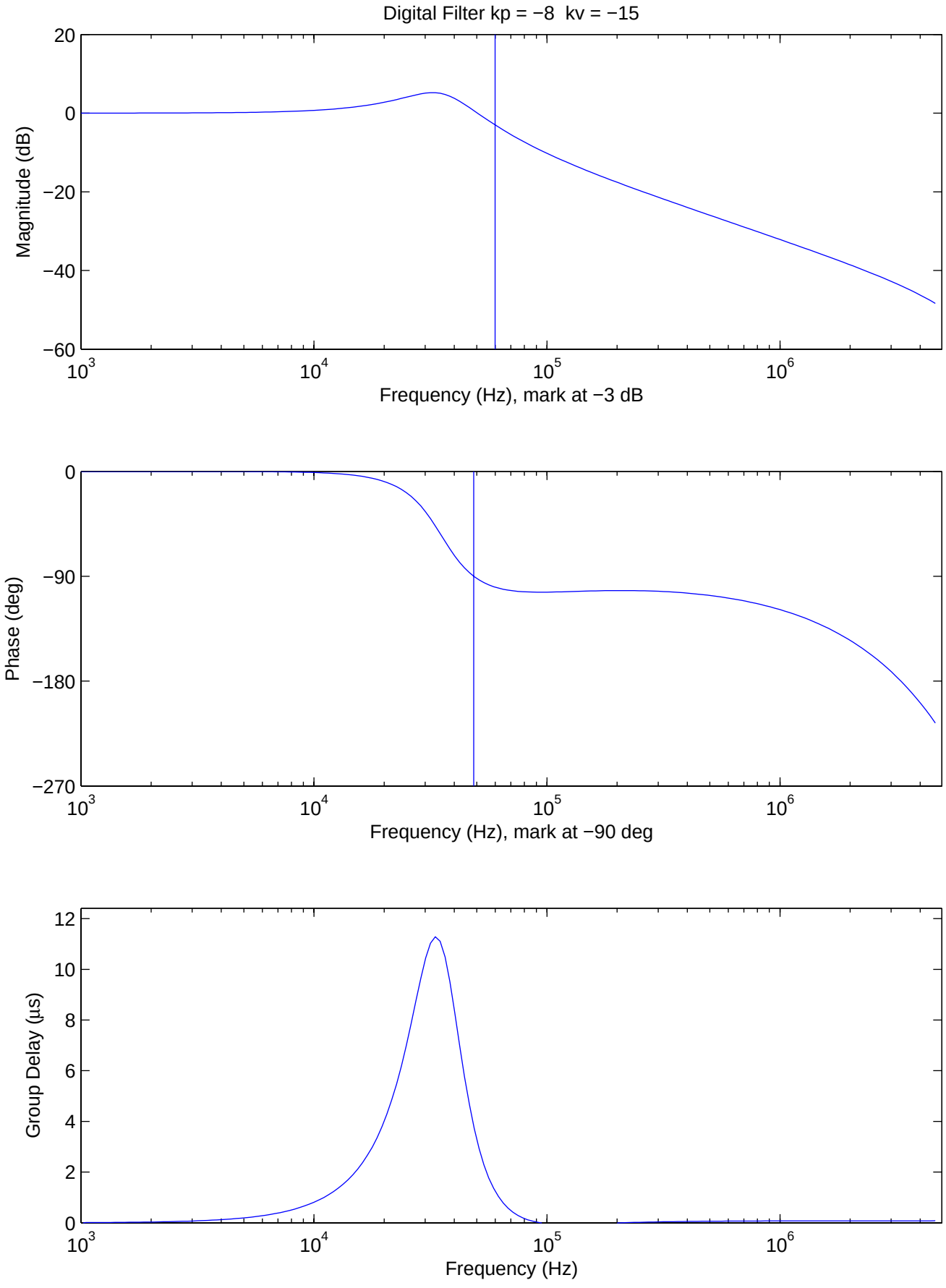

Digital Filter kp = −6 kv = −17
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
2
1.5
1
0.5
0
Frequency (Hz)

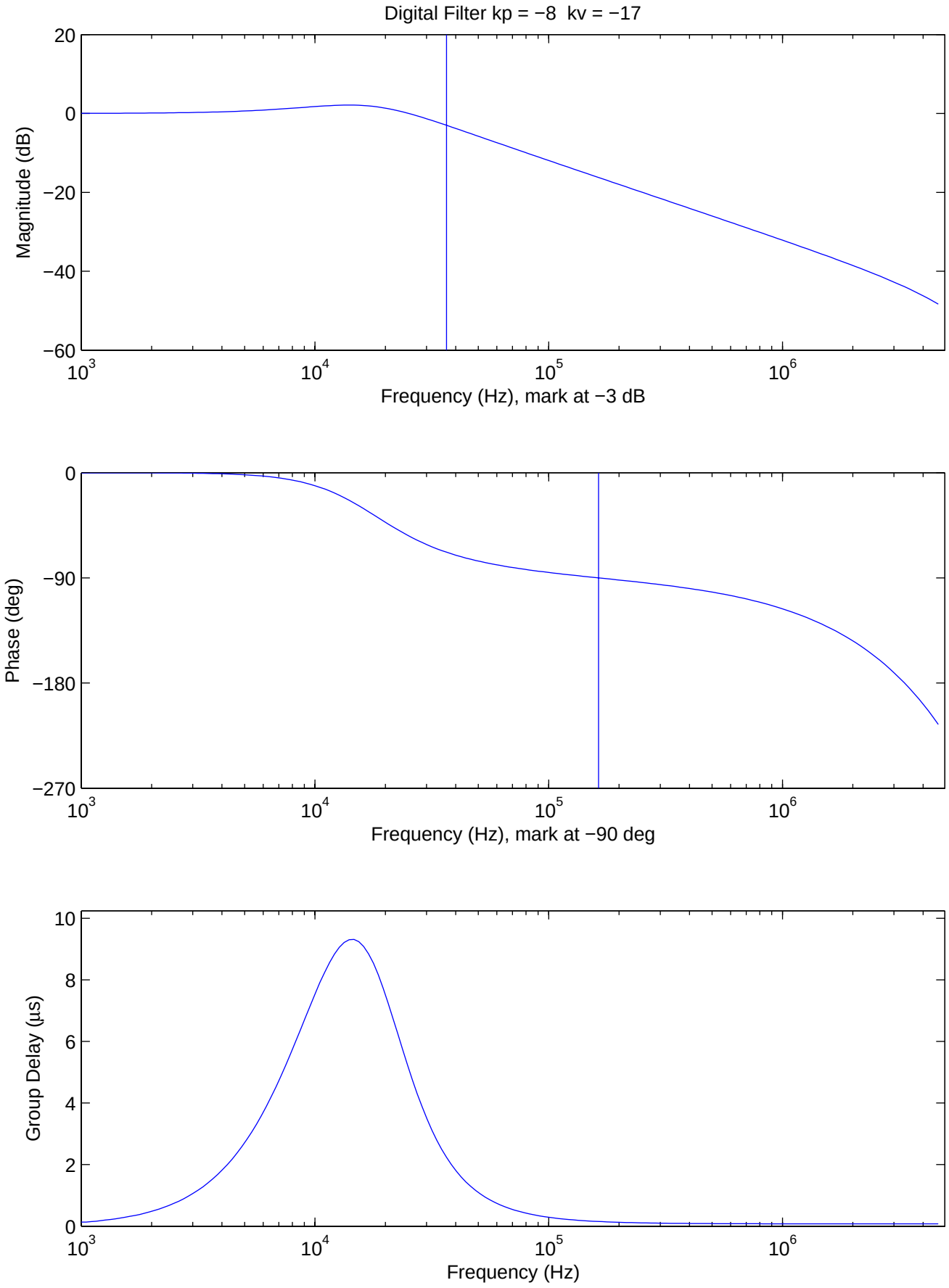

Digital Filter kp = −7 kv = −13
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
6
5
4
3
2
1
0
10^3
10^4
10^5
10^6
Frequency (Hz)

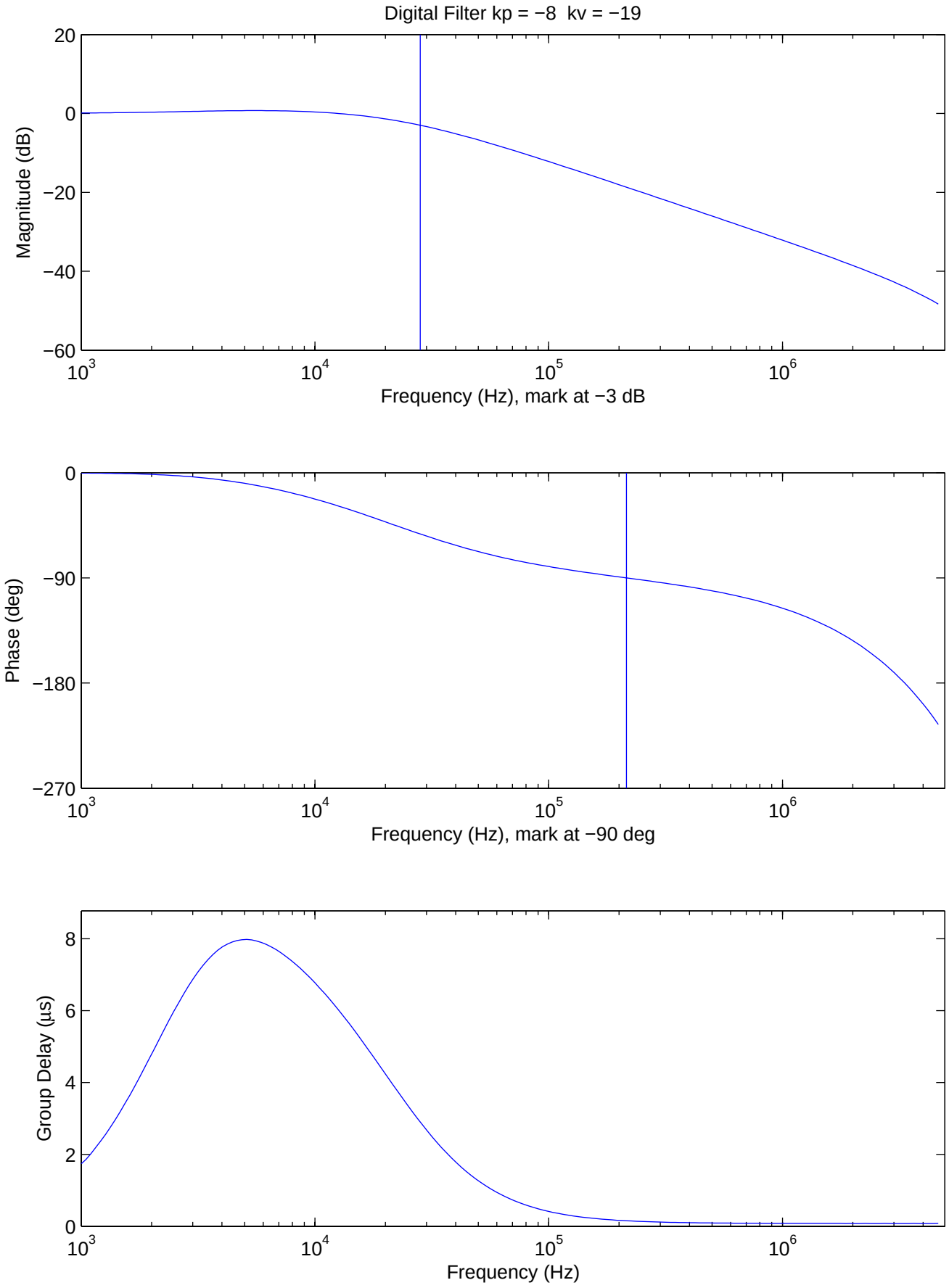

Digital Filter kp = −7 kv = −15
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
5
4
3
2
1
0
10^3
10^4
10^5
10^6
Frequency (Hz)

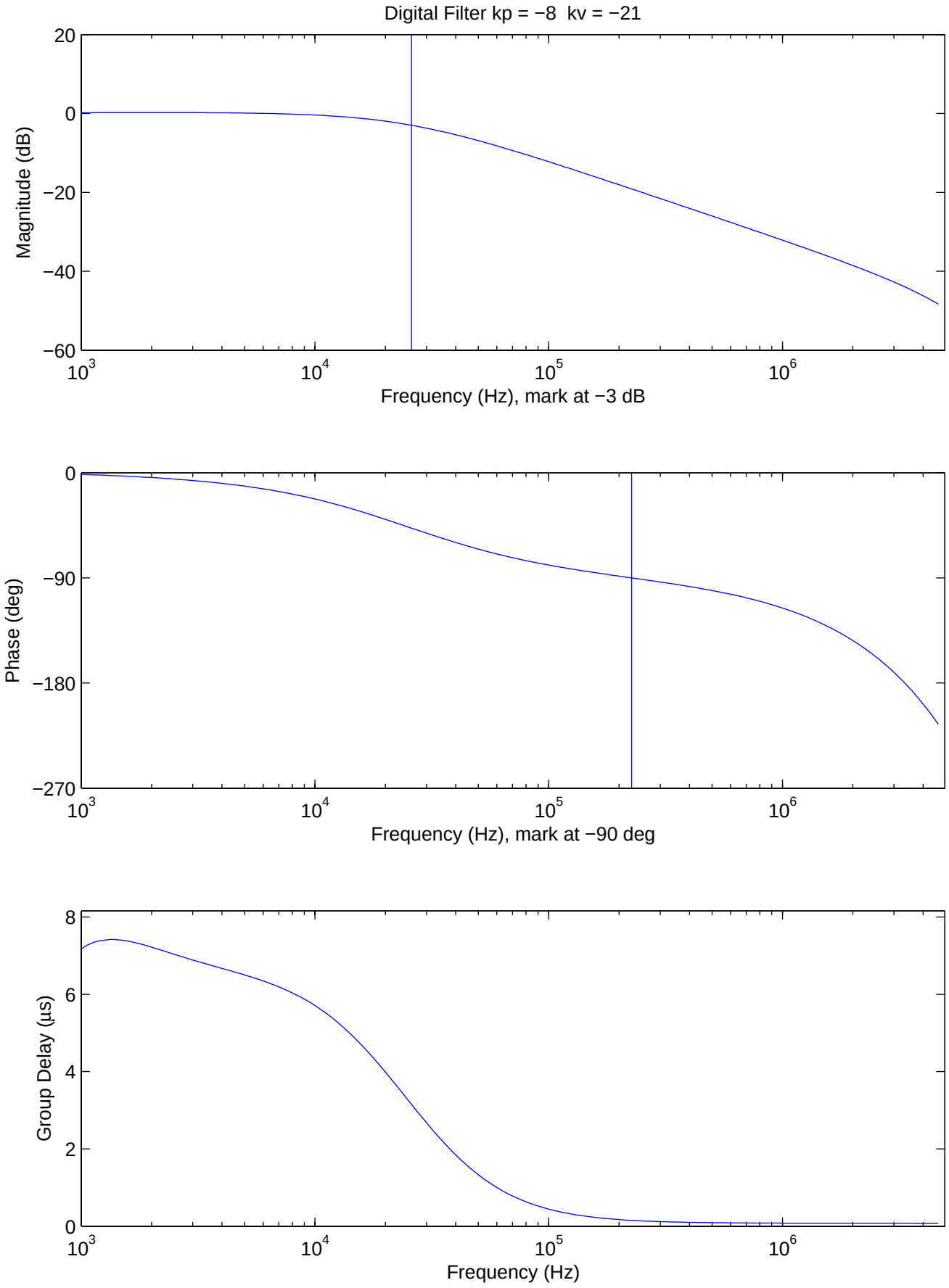

Digital Filter kp = −7 kv = −17
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
4
3
2
1
0
10^3
10^4
10^5
10^6
Frequency (Hz)

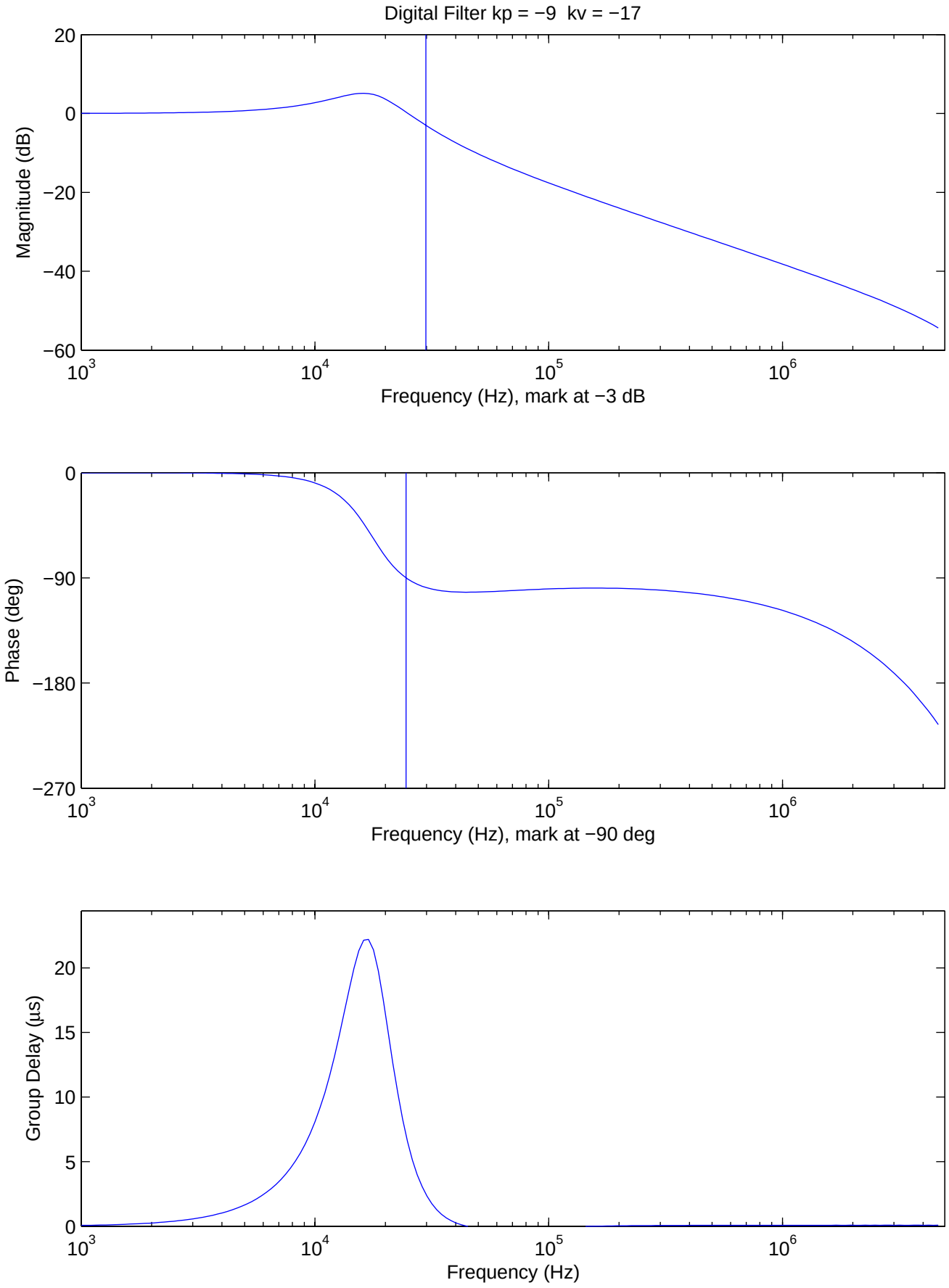

Digital Filter kp = −7 kv = −19
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
4
3
2
1
0
Frequency (Hz)

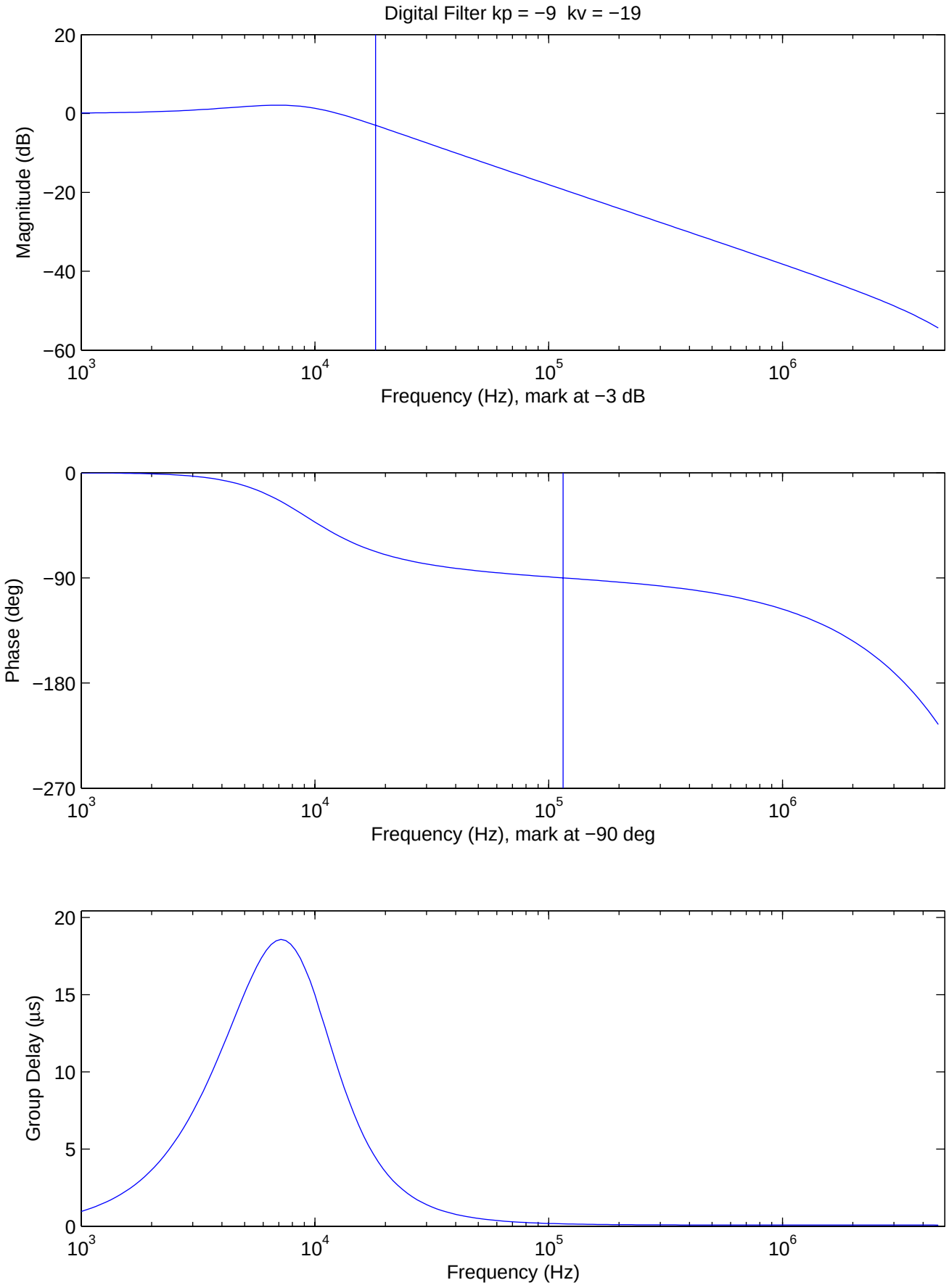

Digital Filter kp = −8 kv = −15
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
12
10
8
6
4
2
0
10^3
10^4
10^5
10^6
Frequency (Hz)

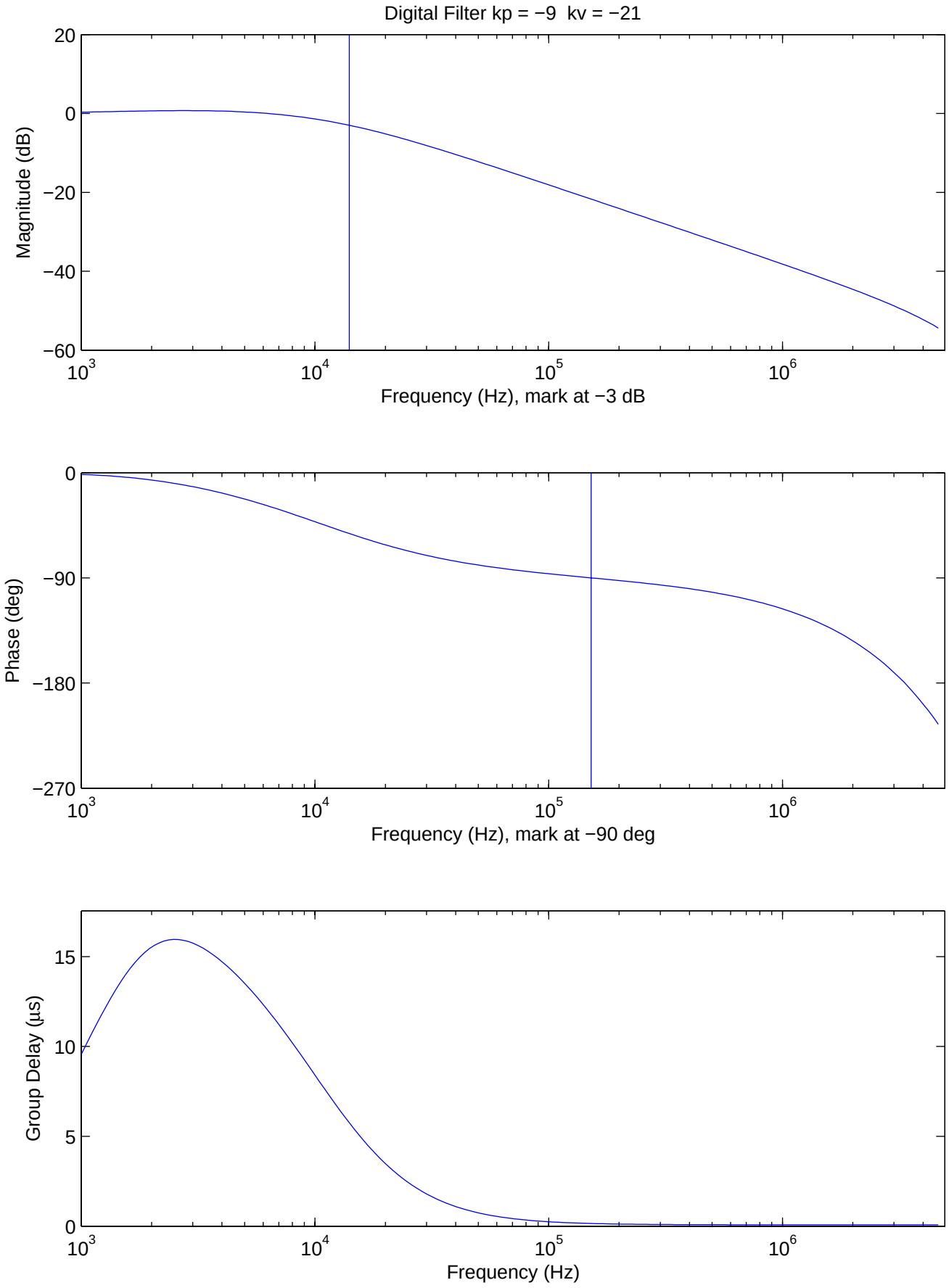

Digital Filter kp = −8 kv = −17
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
10
8
6
4
2
0
10^3
10^4
10^5
10^6
Frequency (Hz)


Digital Filter kp = −8 kv = −19
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
8
6
4
2
0
10^3
10^4
10^5
10^6
Frequency (Hz)


Digital Filter kp = −8 kv = −21
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
8
6
4
2
0
10^3
10^4
10^5
10^6
Frequency (Hz)


Digital Filter kp = −9 kv = −17
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
20
15
10
5
0
Frequency (Hz)


Digital Filter kp = −9 kv = −19
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −90 deg
Group Delay (µs)
20
15
10
5
0
10^3
10^4
10^5
10^6
Frequency (Hz)


Digital Filter kp = −9 kv = −21
Magnitude (dB)
20
0
−20
−40
−60
10^3
10^4
10^5
10^6
Frequency (Hz), mark at −3 dB
Phase (deg)
0
−90
−180
−270
Frequency (Hz), mark at −90 deg
Group Delay (µs)
15
10
5
0
Frequency (Hz)

Zygo Corporation
Laurel Brook Road
Middlefield, Connecticut 06455
USA

Phone: 860-347-8506 or 800-994-6669

See www.zygo.com for a complete list of locations.