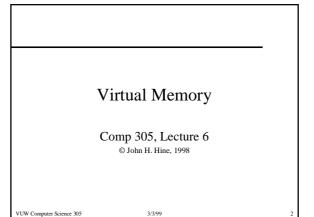
This Week

- ◆ Easter Help Desk Hours
 - 10-17 April No Help Desk
 - 20-24 April 10-12AM, C405
 - 27 April Normal hours resume
- ◆ No tutorial
- ◆ No homework

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This Week

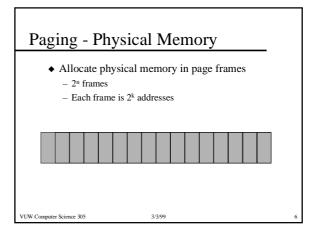
- ◆ Paging
- **◆** Segmentation
- ◆ Translation Lookaside Buffers

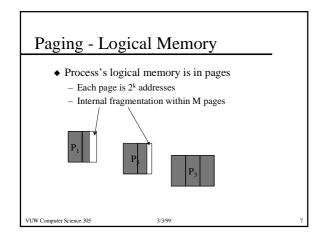
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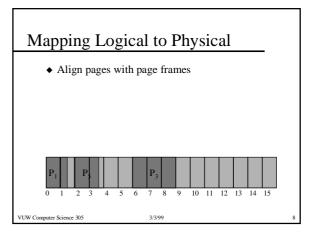
3/3/99

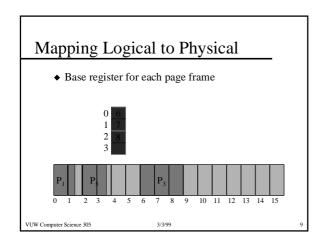
Logical v. Physical Address ♦ Logical address instruction generated by logical 1352 instruction ◆ Physical address relocation register passed to memory unit ♦ Virtual address physical logical address in address 13352 systems where logical memory unit and physical differ

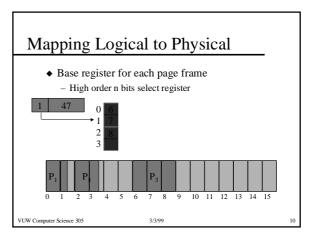
Fragmentation P₁ P₂ P₃ P₁ P₄ P₅ P₃ P₁ P₅ P₃ External fragmentation P₆ VUW Computer Science 305 3/3/99 5

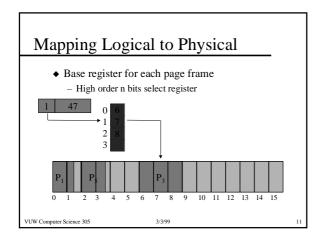


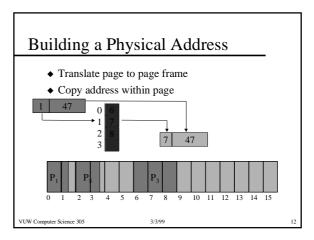


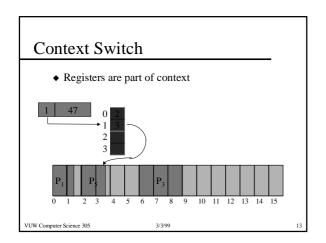


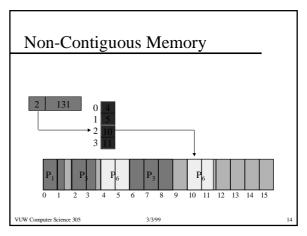








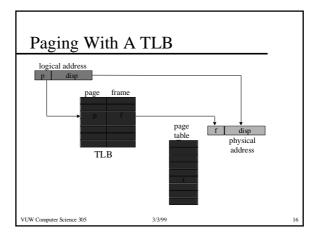


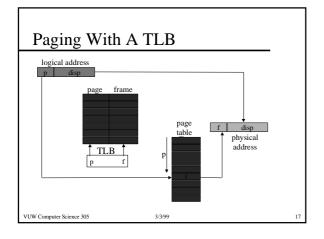


Performance Considerations

- ◆ Every access must go through page table
- ◆ Small page table → registers
- ◆ Large page table → table in memory
 - Access requires indexing page table
 - Then accessing memory
- ◆ Translation look aside buffer
 - "Associative cache"

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TLB Performance ◆ Assumptions memory access 100 nsec TLB access 20 nsec ◆ 90% "hit rate" .90 x (20 + 100) + .10 x (20 + 100 + 100) = 130 nsec ◆ Context switch

