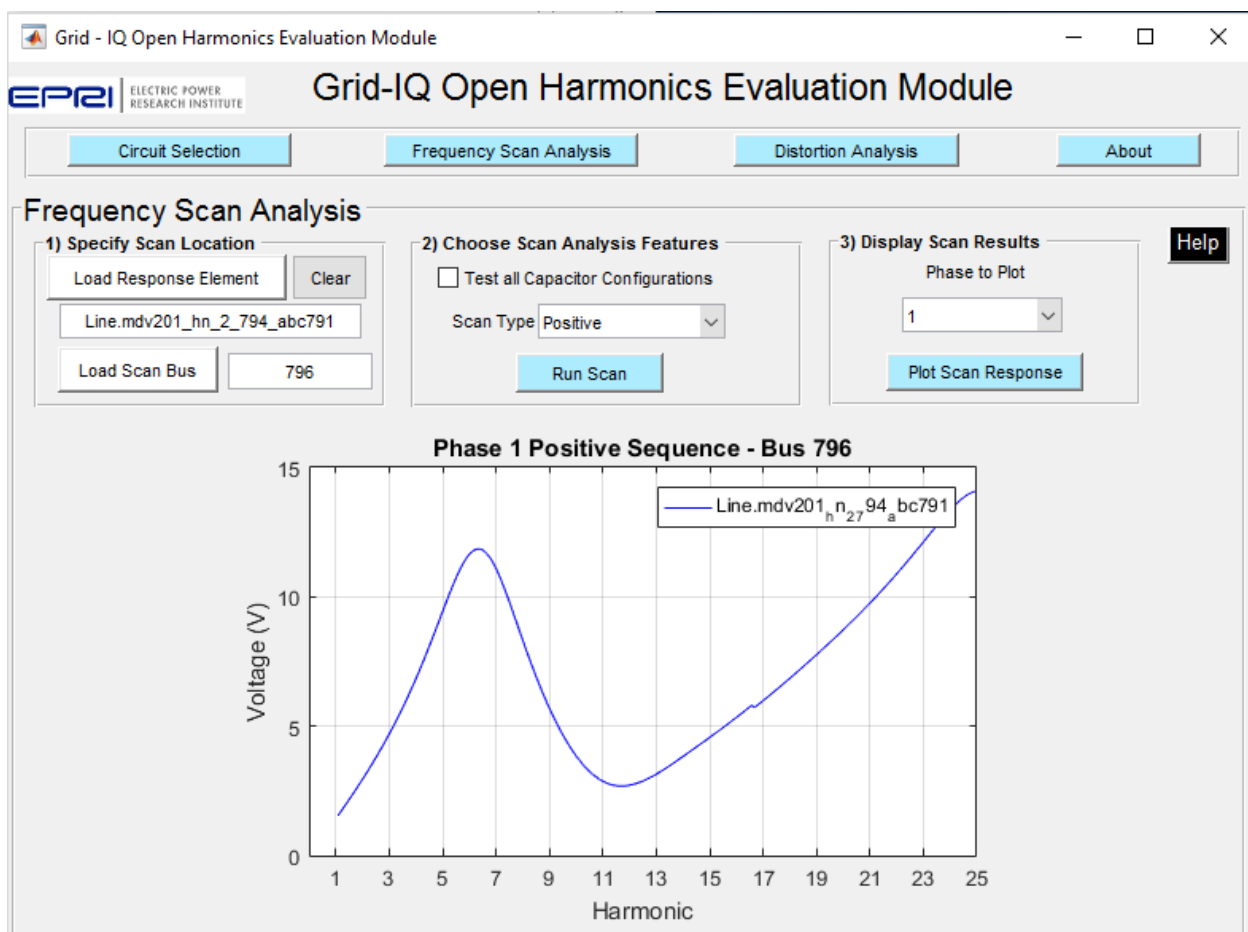


## Frequency Scan Analysis

Frequency scans give general information about frequency response characteristics. For current scans, all voltage sources are shorted, and all current sources (other than the current source being used for the scan) are open-circuited. Unity ampere current is injected at different frequencies at the desired bus. The resultant voltages at all of the injection frequencies are then plotted to get the frequency response of the system. The voltages at the point of injection represent the system impedance versus the frequency (voltage resulting from a 1-amp source is the same as the impedance). Voltages at other system buses represent a transfer characteristic in units of volts per amp injected at the source location.

This section describes the process of conducting frequency scans on the circuit that has been loaded from the library. The screenshot of this particular tab that can be activated by clicking on the “Frequency Scan Analysis” button at the top of the interface is shown in Figure 1-6.



**Figure 1-1**  
**Frequency Scan Analysis tab**

### **1) Specify Scan Location**

The location for a unity ampere current source is specified by clicking on the desired location on circuit plot to be followed by clicking on the “Load Scan Bus” button. This will cause the name of the injection node to populate the text box that is placed next to the “Load scan bus” button. If the “Load Scan Bus” name is known, the name may be manually added by placing the cursor in the box and then typing the scan bus name.

The bus where the resultant frequency response is desired is specified by clicking on the desired location on circuit plot to be followed by clicking on the “Load Response Element” button. This will cause the name of the response element to populate the text box that is placed below the “Load Response Element” button. In most cases, scan bus and response element location are the same. It may be noted that multiple elements can be specified for this field by repeating this procedure. In the case where the scan needs to be performed at new bus location, the “load response element” field needs to be cleared first by clicking on the “Clear” button. Multiple elements can be monitored. If the “Load Response Element” name is known, the name may be manually added by placing the cursor in the box and then typing the name.

### **2) Choose Scan Analysis Features**

The user can select to perform positive or zero sequence scan by making the appropriate selection from the dropdown list labeled as “Scan Type.”

Clicking on the “Run Scan” button will prompt the solution engine to perform the scan. During this simulation, a progress window will pop up and close once the scan is completed.

The user can also opt to perform scans for all the different capacitor bank configurations that are possible by checking the “Test all capacitor configurations” checkbox on the interface.

### **3) Display Scan Results**

The results can be viewed once the progress window is closed by clicking on the “Plot Scan Response” button. The example plot for the positive sequence scan for Phase 1 (Phase A) is also shown in Figure 1-7. The plots for other phases can be viewed by making the appropriate selection in the dropdown list titled “Phase to Plot.”

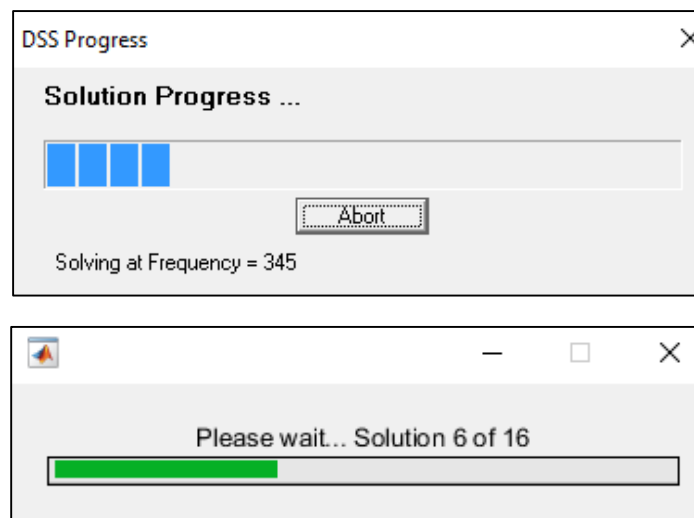
If the “Test all capacitor configurations” option is selected, the result output also includes a table indicating the capacitor configuration that leads to the worst-case resonance for each harmonic at each monitored element. An illustration of the results table is included in Figure 1-8.

If the circuit has many elements and multiple capacitors, it can take several minutes for the results to become available. If it is desired to know how many solutions have been completed out of how many solutions that will be completed, as shown in Figure 1-9, the user may use the mouse to move the DSS Progress (blue segmented bar) window to reveal the solution count (red bar) window to read the solution count statistics.

Figure 21: Cap Status for worst harmonic magnification at Line.mdv201\_hn\_2\_794\_abc791

	H3	H5	H7	H9	H11	H13	H15
Capacitor.mdv201_hn_2_116_abc28285-1	1	1	1	0	0	0	0
Capacitor.mdv201_hn_2_818_abc63707-1	1	1	1	1	1	1	1
Capacitor.mdv201_hn_2_345_abc8081-1	1	1	1	1	1	0	0
Capacitor.mdv201_da_8_153_abc74433-1	1	1	0	0	0	0	0

**Figure 1-2**  
Sample worst-case capacitor configuration for each harmonic at scan bus



**Figure 1-3**  
DSS Progress window moved to reveal the solution statistics window