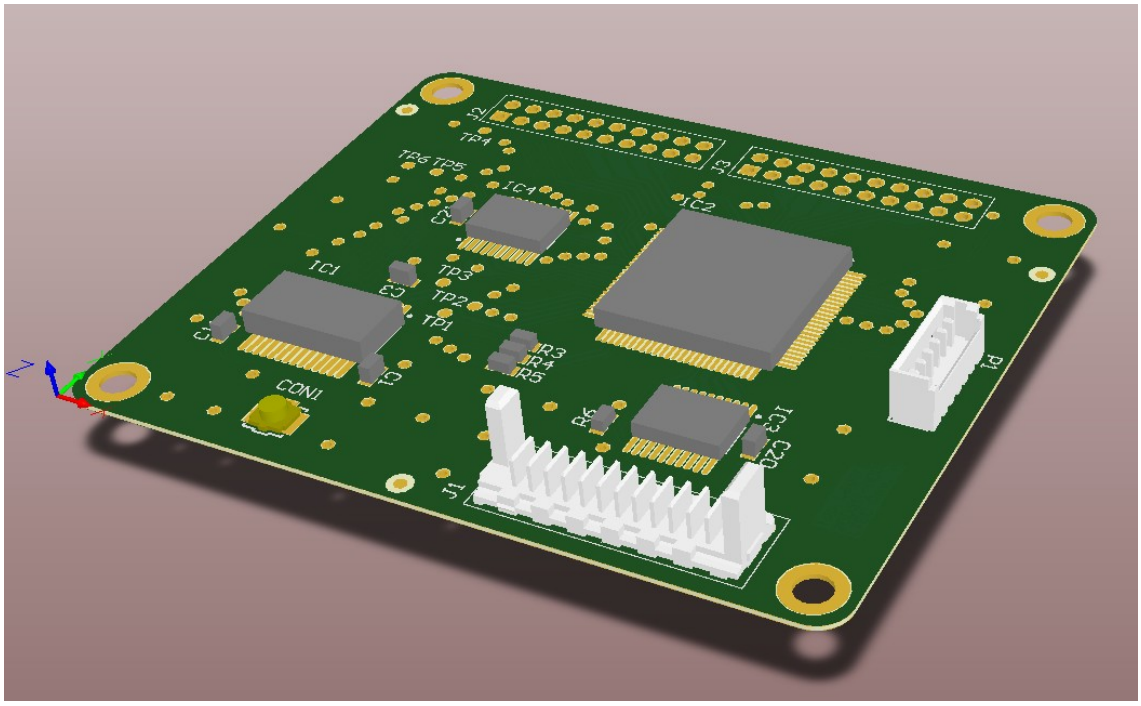
Line Image Sensor Controller (LISC)



1 Short Description

The Line Image Sensor Controller (LISC) is a universal electronics board that contains readout electronics for various linear image sensors (CCD, CMOS APS, FPA). It can be connected to a data acquisition controller (e. g. microcontroller) for further data processing and transmission. The LISC's main applications are optical spectrometers and industrial linear camera systems.

The LISC contains following parts:

- Analog-Frontend:
    - High resolution: 16 Bit AD-Converter
    - Dynamic area: >12 Bit (with adjusted gain)
    - Correlated Double Sampling/Sample and Hold circuity
    - Programmable gain: 1x to 6x
    - Programmable offset. ±300mV
- Fast Readout Logic with Parallel Digital Camera Interface
    - Max. readout speed: 2000 kPixels/s
    - 4 programmable readout speeds: (500, 1000, 1500 und 2000 kPixel/s)
    - Programmable integration time (1,05ms to 60s --> depending on applied line image sensor)
    - 8-bit parallel synchronous digital camera interface

2 Detailed Specification

2.1 Line Image Sensor Controller (LISC)

The Line Image Sensor Controller (LISC) consists of two subsystems: an analog front end and a fast readout logic.

The analog front end contains a video signal processor with analog signal preprocessing and a 16-bit AD converter.

The readout logic is implemented on a CPLD and is used to generate clock signals for various line sensors (tested with CCD line sensors from Sony: ILX511, ILX554). Additionally, the logic takes over the configuration and control of the analog signal preprocessing and the AD conversion. The video data is output via 8-bit parallel (pixel by pixel) synchronous digital camera interface.

The interface to the line image sensor consists of a 12-pin male connector for supply and clock control signals as well a U.FL connector for the analog video signal.

The data interface consists of an 8-bit digital camera interface for video data and a serial interface for configuration of the LISC. The system can be controlled directly via 4 additional inputs. (The data interface can be adapted to use the LISC as a stand-alone module. 8 additional GPIOs are reserved for this purpose.)

LISC Specification	
AD-Converter	16Bit
Converion rate	500, 1000, 1500, 2000kSps
Video signal input	0V bis 4V
Input capacity	10pF
Programmable gain	0dB bis 16dB (1x bis 6x)
Programmable offset	±300 mV (**tbd** (counts))
Elctrical distortion/non-linearity	**tbd (**counts)
Temperature drift	**tbd (**counts/°C)
Max. readout speed	2000kPixel/s
Programmable integration time	1,05ms to 60ms
Power consumption (w/o sensor)	1,1W

LISC Line Image Sensor Interface			
Pin number	**Pin name**	**I/O**	**Function**
Analog Video Input			
CON1-1	AI1	IN	Analog video signal
CON1-2	GND	PWR	analog ground
Line Image Sensor Control Interface			
J1-1	GND	PWR	reserved
J1-2	SCL	OUT	reserved for I2C
J1-3	SDA	IN/OUT	reserved for I2C
J1-4	3V3	PWR	reserved
J1-5	5V	PWR	supply line sensor
J1-6	GND	PWR	supply line sensor
J1-7	RESET1	OUT	ROG/START – readout start
J1-8	SENCLK1	OUT	CLK – readout clock
J1-9	ADCTRIG	IN	reserved
J1-10	SENCLK3	OUT	reserved
J1-11	RESET2	OUT	reserved
J1-12	SENCLK2	OUT	reserved

LISC Data and Configuration Interface			
Pin number	**Pin name**	**I/O**	**Function**
Serial Config Interface			
J2-2	SCLK	IN	serial clock
J2-4	MOSI	IN/OUT	serial data
J2-6	MISO	IN/OUT	serial data
J2-8	CS	IN	chip select
Parallel Digital Camera Interface			
J2-13	PIXCLK	OUT	pixel clock
J2-15	VSYNC	OUT	vertical synchronisation
J2-17	HSYNC	OUT	horizontal synchronisation
J3-4	DA[0]	OUT	data bit 0
J3-6	DA[1]	OUT	data bit 1
J3-8	DA[2]	OUT	data bit 2
J3-10	DA[3]	OUT	data bit 3
J3-12	DA[4]	OUT	data bit 4
J3-14	DA[5]	OUT	data bit 5
J3-16	DA[6]	OUT	data bit 6
J3-18	DA[7]	OUT	data bit 7
4 Control-I/Os			
Pin number	**Pin name**	**I/O**	**Function**
J2-12	RESET	IN	digital camera reset
J2-14	START	IN	exteral trigger/start readout
J2-16	EXTCLK	IN	digital camera main clock
J2-18	READY	OUT	readout ready
J2-20	RST	IN	system reset
8x DATA I/Os reserved for alternative interface			
Pin number	**Pin name**	**I/O**	**Function**
J3-3	DB[0]	IN/OUT	reserved
J3-5	DB[1]	IN/OUT	reserved
J3-7	DB[2]	IN/OUT	reserved
J3-9	DB[3]	IN/OUT	reserved
J3-11	DB[4]	IN/OUT	reserved
J3-13	DB[5]	IN/OUT	reserved
J3-15	DB[6]	IN/OUT	reserved
J3-17	DB[7]	IN/OUT	reserved

2.2 Power Supply (PWS)

The Line Image Sensor Controller (LISC) requires stable filtered power supply of 5V from a higher-level system. It has a linear converter on board to create 3.3V for local supply and feeds 5V through to supply line image sensor.

PWS Specification	
Voltage input	5V
Voltage output	5V
Power consumption max.	>2.5W (**tbd)**

PWS Connector			
P3			
Pin number	**Pin name**	**I/O**	**Function**
J2-1	5V	PWR	5V Supply
J2-2	GND	PWR	ground

2.3 General

The Line Image Sensor Controller (LISC) is implemented on a Printed Circuit Board with the size of 60mmx50mm. The maximum height of populated board is equal or smaller than 12mm.

Storage temperature: -65°C to 150°C

Operating temperature: 0°C to 70°C

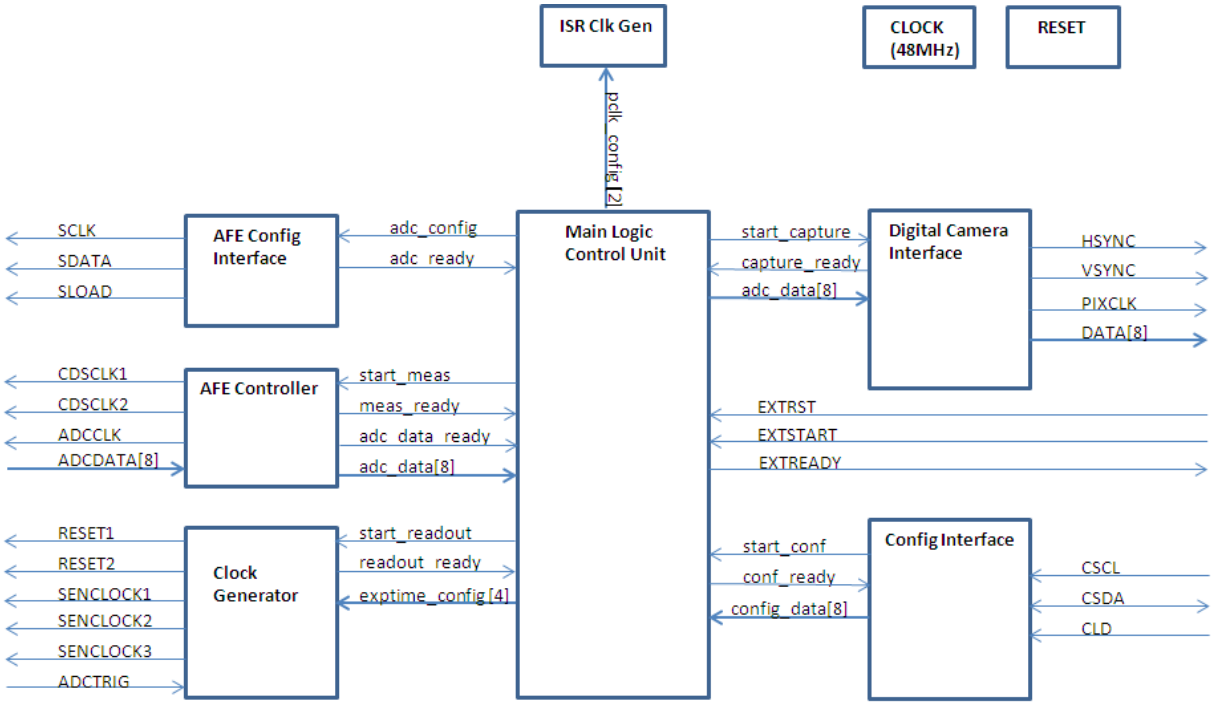
3 System Description Readout Logic

The readout logic is the main component of the LISC. It is implemented as VHDL code on a CPLD so that the electronic card can be used with different line sensors (CCD, CMOS APS or FPA) by making minor adjustments to the firmware. (the function was tested with ILX511 / ILX554 of CCD line sensors from Sony.)

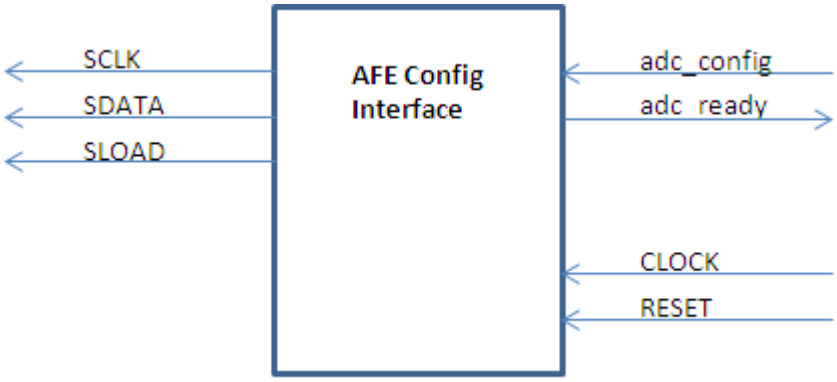
The readout logic configures and controls the analog signal preprocessing and digitization of sensor data. It also controls the reading of the line sensor and the transmission of the data to a microcontroller.

The readout logic can be controlled directly via three lines. Various parameters (such as readout speed, integration time, etc.) can be set on a register basis via a serial interface.

The readout logic consists of several VHDL modules that implement various functions. The individual modules are briefly described below.



3.1 AFE Config Interface

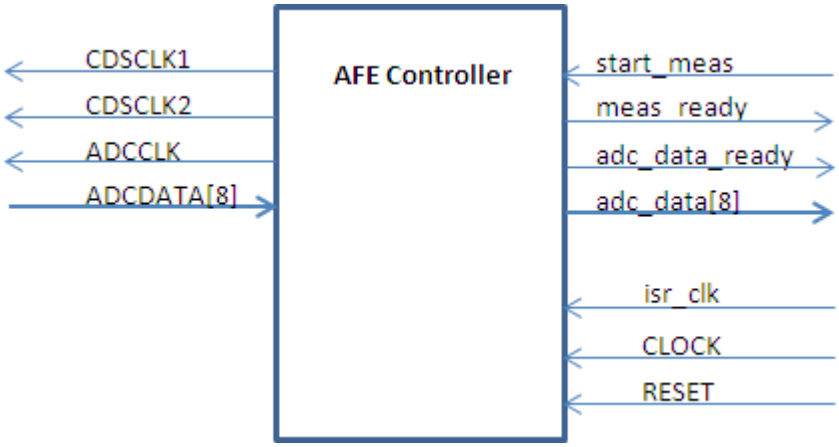


The AFE-Config Interface (Analog Front-End Config Interface) module configures the AD-converter at every start / reset, or if configuration parameters have been changed via the serial interface of the AD-converter. 8 registers are written to in the AD-converter.

Configuration data of the AD-Converter (AD9826):

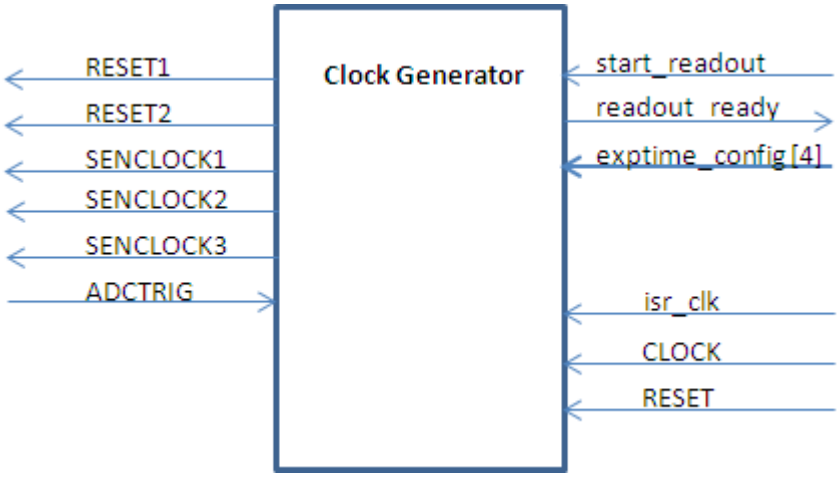
- Signal input range (4V or 2V)
- Internal reference (on/off)
- 3-channel-/2- channel -/1- channel -mode (adjustable)
- Analog readout configuration (“correlated double sampling” or “sample and hold“)
- Input clamp bias (4V/3V)
- Sleep mode (on/off)
- Output mode (16Bit/8Bit)
- Multiplexer config (RBG/BGR)
- Channel selection (R/G/B)
- PGA gain (1 bis 6)
- Offset (-300mV bis +300mV)

3.2 AFE Controller



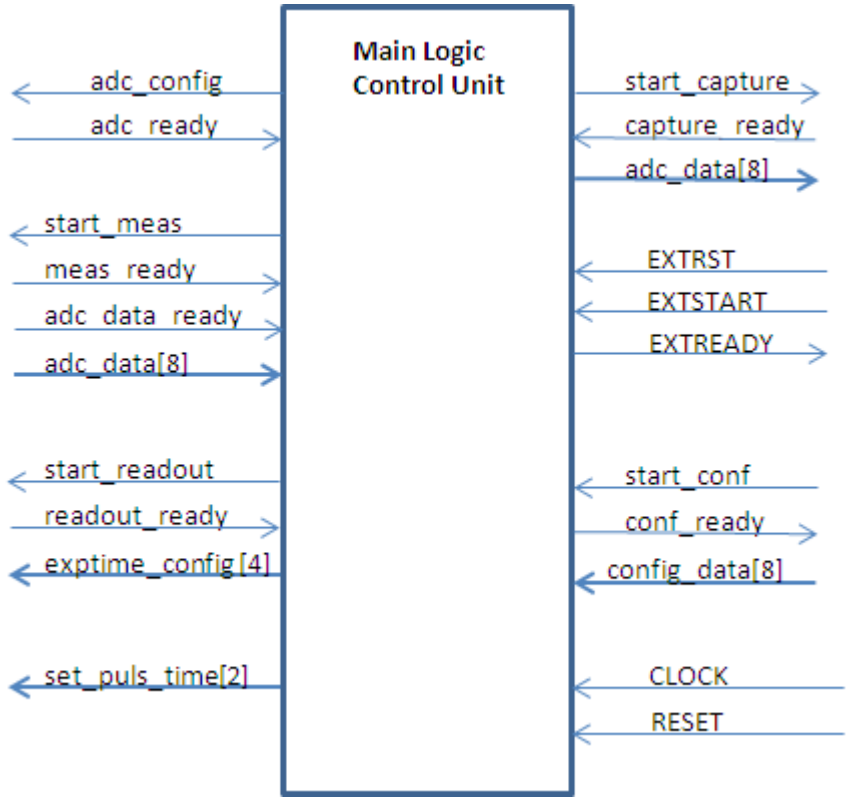
This module generates signals for sampling (CDS or SHA) and for digitizing the video signal. The signals are then applied to the outputs at the specified times via two control lines. Every time a data item is present at the AD converter output, the adc_data_ready signal is set. The module works synchronously with isr_clk.

3.3 Clock Generator



The clock generator module runs synchronously with isr_clk and generates clock and reset signals for the readout of the line sensor. A different clock generator can be used depending on the line sensor type. The integration time is selected via a 4-bit line.

3.4 Main Logic Control Unit

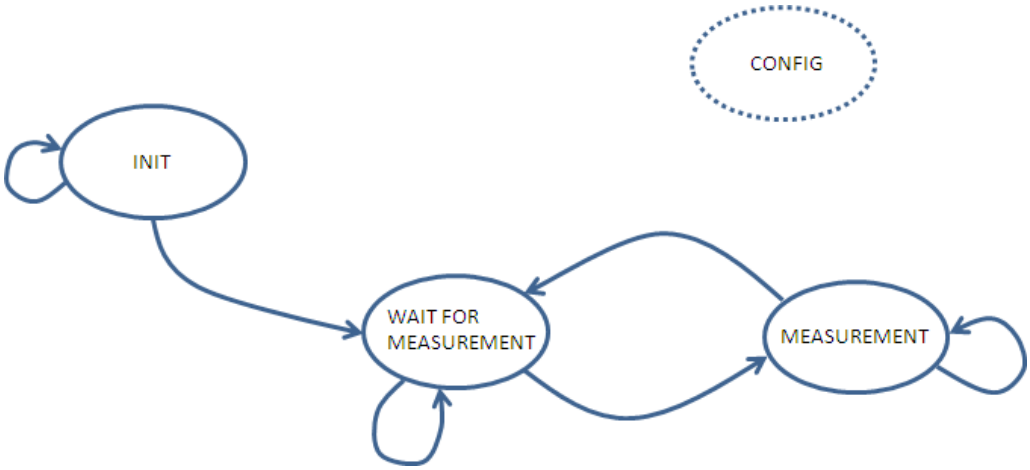


This module controls all processes (reading, sampling, digitizing, transferring) of the entire readout logic, configures the AD converter, and sets the readout and integration time according to the specified values.

The module is based on a state machine with 3 states:

1. ***Init:*** State after switching on / resetting. The system starts the configuration of the AD converter with the existing configuration data. After the successful configuration, the system changes to the second state.
2. ***Wait for Measurement:*** The readout process is started in this state. The reading of the line sensor takes place periodically until an external measurement is triggered. The system then changes to the "Measurement" state.
3. ***Measurement:*** After triggering, a measurement is carried out. After the configured integration time the digitized data is transmitted to the digital camera output. The system then returns to state 2. If a continuous measurement has been set via the config register, the system remains in that state and continuously sends measurement data to the host. The continuous measurement can only be stopped by an external reset signal.

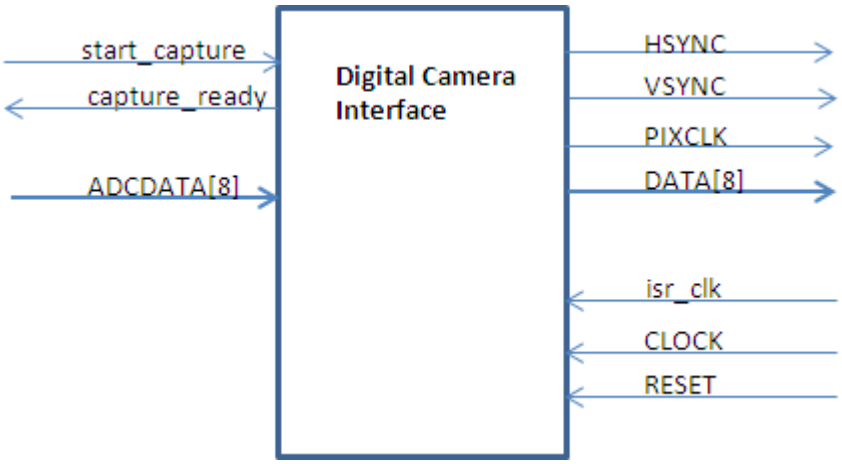
In the fourth state „CONFIG“ (not implemented yet) the global configuration data (e.g. integration time) are read in and all registers of the readout logic are loaded accordingly.



Higher Level configuration data for Readout Logic von Auslese-Logik:

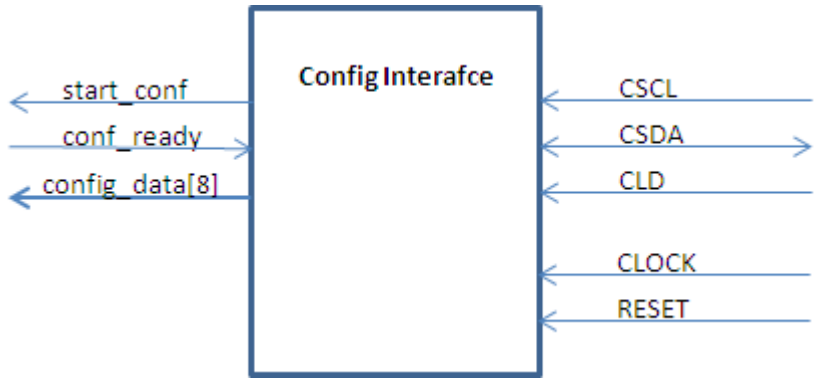
- Integration time (1,05ms bis 60s)
- Readout speed (0,5MHz bis 2MHz)
- Measurement mode (Einzelmessung/Dauermessung)
- Analog frontend configuration (gain, offset, output mode (8Bit/16Bit))

3.5 Digital Camera Interface



This module serves as an interface to the host system (e.g. to a microcontroller). It is based on a parallel synchronous digital camera interface with 8-bit data width. For the test system an STM32F407 microcontroller was used. This microcontroller can receive the data via its DCMI interface using Direct Memory Access (DMA) and store or process it further.

3.6 Config Interface



This module contains a serial interface for higher level configuration of the readout logic. The configuration interface module has not been implemented yet since it requires a more precise specification first.

3.7 ISR-Clock Generator

The ISR clock generator module generates the isr_clk signal from the 48Mhz oscillator, which is used as the main clock for the AFE controller and clock generator as well as for the digital camera interface. The input set_puls_time is used to select the readout speed that was configured on startup.