EMILY WOOD

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EDUCATION

B.A.Sc Computer Engineering, Minor in Honours Mathematics Graduating April 2027
University of British Columbia, Vancouver, BC GPA: 87.5%

Relevant coursework: Microcomputer System Design, Computer Architecture, Operating Systems, Digital Systems Design 1 & 2, Computer Communications, Circuit Analysis

TECHNICAL SKILLS

Programming: C, C++, Verilog, SystemVerilog, ARM, MIPS, Python, Bash,
Software & Tools: Git, Linux, Quartus, ModelSim, Vim, GCC, GDB

WORK EXPERIENCE

Software Development Engineering Intern - Amazon Web Services May 2025 - July 2025

- Designed and implemented an internal tool to automate data migrations within Amazon S3, improving load distibution across nodes in a large-scale distributed system

Full Stack Developer - Ensemble Scientific February 2025 - Present

- Developed embedded C++ code using the lvgl embedded graphics library for an ESP32 touch screen interface, enabling control of an autonomous irrigation system while offline
- Used Django and React.js to develop a web-based interface for autonomous irrigation systems

Developer Intern - Terra Dygital January 2024 - December 2024

- Developed a timesheet and billing system using the .NET framework, SQL, and React.js, reducing the time required to prepare customer invoices by 2 weeks per month

TECHNICAL PROJECTS

Motorola 68000 Microcomputer System January 2025 - April 2025

- Built a M68k-based microcomputer system with integrated SRAM, DRAM and EEPROM
- Implemented a DRAM cache controller in Verilog to manage read, write and refresh cycles
- Designed and verified Verilog and VHDL modules for an 8-way set associative cache to improve DRAM access time by 1.7x
- Wrote embedded software in C for I2C and SPI interfaces to communicate with peripheral EEPROM and I/O devices

Embedded Deep Neural Network Accelerator November 2024

- Built a Nios II-based hardware accelerator in Quartus Platform Designer to run a neural network for handwritten digit recognition
- Wrote a SystemVerilog module to perform matrix-vector multiplication, reducing the computational load on the CPU and improving digit recognition times by 30%

Operating System Kernel September 2023 - December 2023

- Implemented a simple operating system targetting the MIPS architecture
- Added UNIX syscalls to support execution of user programs
- Designed and implemented a virtual memory system that reduced RAM usage by 75%

RISC Processor October 2022 - December 2022

- Used SystemVerilog to build a 16-bit RISC processor capable of executing a subset of the ARM ISA
- Optimized control and data paths for each instruction to maximize throughput