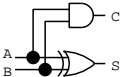


$\begin{array}{r} \text{A} \\ + \text{B} \\ \hline \end{array}$	$\begin{array}{r} 0 \\ + 0 \\ \hline \end{array}$	$\begin{array}{r} 0 \\ + 1 \\ \hline \end{array}$	$\begin{array}{r} 1 \\ + 0 \\ \hline \end{array}$	$\begin{array}{r} 1 \\ + 1 \\ \hline \end{array}$
C S	0 0	0 1	0 1	1 0

入力		出力	
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



半加算器の真理値表

半加算器の回路図