Features

- Contactless Power Supply
- Contactless Read/Write Data Transmission
- Radio Frequency f_{RF} from 100 kHz to 150 kHz
- Basic Mode or Extended Mode
- Compatible with T5557, ATA5567
- Replacement for e5551/T5551 in Most Common Operation Modes
- Configurable for ISO/IEC 11784/785 Compatibility
- Total 363 Bits EEPROM Memory: 11 Blocks (32 Bits + 1 Lock Bit)
  - 7 × 32 Bits EEPROM User Memory Including 32-bit Password Memory
  - 2 × 32 Bits for Unique ID
  - 1 × 32-bit Option Register in EEPROM to Set Up the Analog Front End:
    - Clock and Gap Detection Level
    - Improved Downlink Timing
    - Clamp and Modulation Voltage
    - Soft Modulation Switching
    - Write Damping like the T5557/ATA5567 or with Resistor
    - Downlink Protocol
  - 1 × 32-bit Configuration Register in EEPROM to Setup:
    - Data Rate:
      - RF/2 to RF/128, Binary Selectable or
      - Fixed Basic Mode Rates
    - Modulation/Coding:
      - Bi-phase, Manchester, FSK, PSK, NRZ
    - Other Options:
      - Password Mode
      - Max Block Feature
      - Direct Access Mode
      - Sequence Terminator(s)
      - Blockwise Write Protection (Lock Bit)
      - Answer-On-Request (AOR) Mode
      - Inverse Data Output
      - Disable Test Mode Access
      - Fast Downlink (~6 Kbits/s versus ~3 Kbits/s)
      - OTP Functionality
      - Init Delay (~67 ms)
- High Q-antenna Tolerance Due to Build in Options
- Adaptable to Different Applications: Access Control, Animal ID and Waste Management
- On-chip Trimmed Antenna Capacitor:
  - 250 pF/330 pF (±3%)
  - 75 pF/130 pF (On Request)
  - Without On-chip Capacitor (On Request)
- Pad Options
  - ATA5577M1
    - 100 µm × 100 µm for Wire Bonding or Flip Chip
  - ATA5577M2
    - 200 µm × 400 µm for Direct Coil Bonding

Read/Write LF RFID IDIC 100 to 150 kHz

ATA5577

Preliminary

4967CX–RFID–12/08

1. Description

The ATA5577 is a contactless read/write **id**entification **IC** (IDIC®) for applications in the 125-kHz or 134-kHz frequency band. A single coil connected to the chip serves as the IC's power supply and bi-directional communication interface. The antenna and chip together form a transponder or tag.

The on-chip 363-bit EEPROM (11 blocks with 33 bits each) can be read and written block-wise from a base station (reader).

Data is transmitted from the IDIC (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes serial base station commands (downlink), which are encoded as 100% amplitude modulated (OOK) pulse-interval-encoded bit streams.

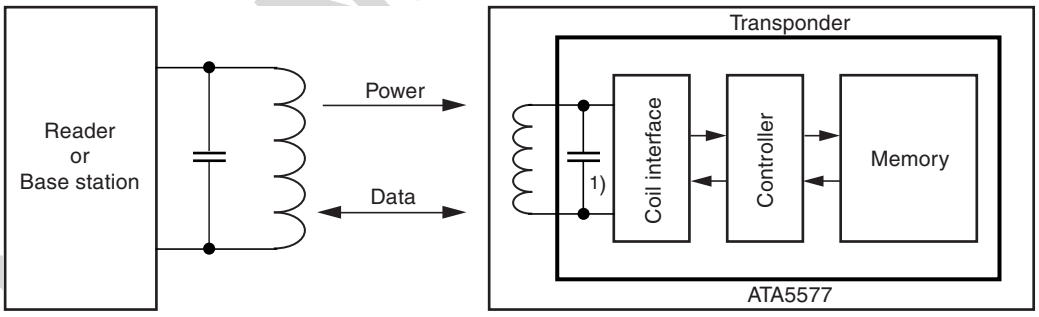
2. Compatibility

The ATA5577 is designed to be compatible with the T5557/ATA5567. The structure of the configuration register is identical. The two modes, Basic mode and Extended mode, are also available. The ATA5577 is able to replace the e5551/T5551 in most common operation modes. In all applications, the correct functionality of the replacements must be evaluated and proved.

For further details, refer to Atmel®'s web site for product-relevant application notes.

3. System Block Diagram

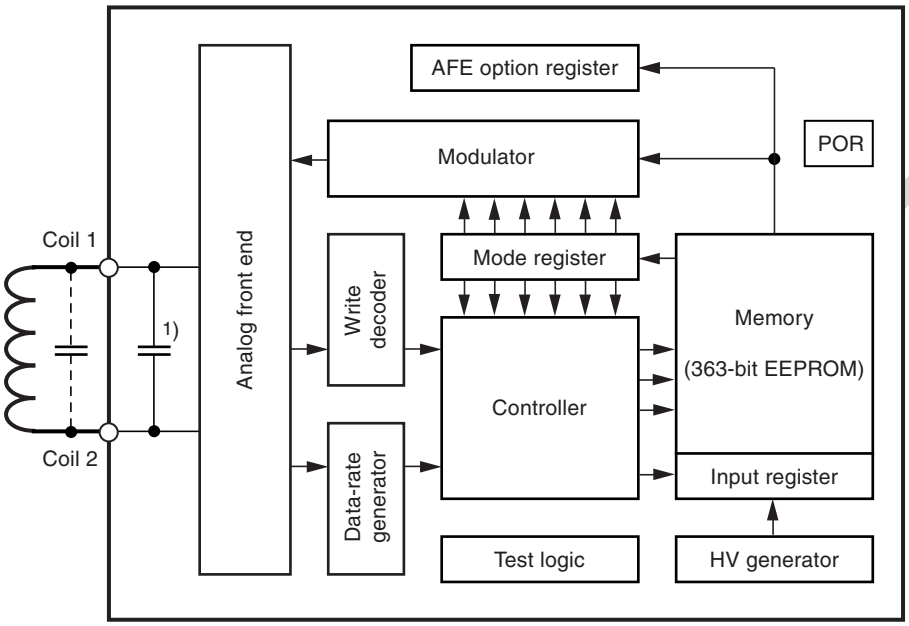
Figure 3-1. RFID System Using ATA5577 Tag



1) Mask option

4. ATA5577 - Functional Blocks

Figure 4-1. Block Diagram



1) Mask option

4.1 Analog Front End (AFE)

The AFE includes all circuits that are directly connected to the coil terminals. It generates the IC's power supply and handles the bi-directional data communication with the reader. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1 and Coil 2 for data transmission from the tag to the reader
- Field-gap detector for data transmission from the base station to the tag
- ESD-protection circuitry

4.2 AFE Option Register

The option register maintains a readable shadow copy of the data held in the EEPROM block 3 page 1. This contains the analog front end's level and threshold settings, as well as enhanced downlink protocol selection with which the device can be fine tuned for perfect operation and all application environments. It is continually refreshed during read-mode operation and (re-)loaded after every POR event or reset command. By default the option register is pre-programmed according to Table 10-1 on page 40.

4.3 Data-rate Generator

The data rate is binary programmable to operate at any even-numbered data rate between RF/2 and RF/128 or to any of the fixed Basic mode data rates (RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100 and RF/128).

4.4 Write Decoder

The write decoder detects the write gaps and verifies the validity of the data stream according to the Atmel e555x downlink protocol (pulse interval encoding).

4.5 HV Generator

This on-chip charge pump circuit generates the high voltage required to program the EEPROM.

4.6 DC Supply

Power is externally supplied to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

4.7 Power-On Reset (POR)

The power-on reset circuit blocks the voltage supply to the IDIC until an acceptable voltage threshold has been reached.

4.8 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

4.9 Controller

The control logic module executes the following functions:

- Load mode register with configuration data from EEPROM block 0 after power-on and during reading
- Load option register with the settings for the analog front end stored in EEPROM page 1 block 3 after power-on and during reading
- Control all EEPROM memory read/write access and data protection
- Handles the downlink command decoding detecting protocol violations and error conditions

4.10 Mode Register

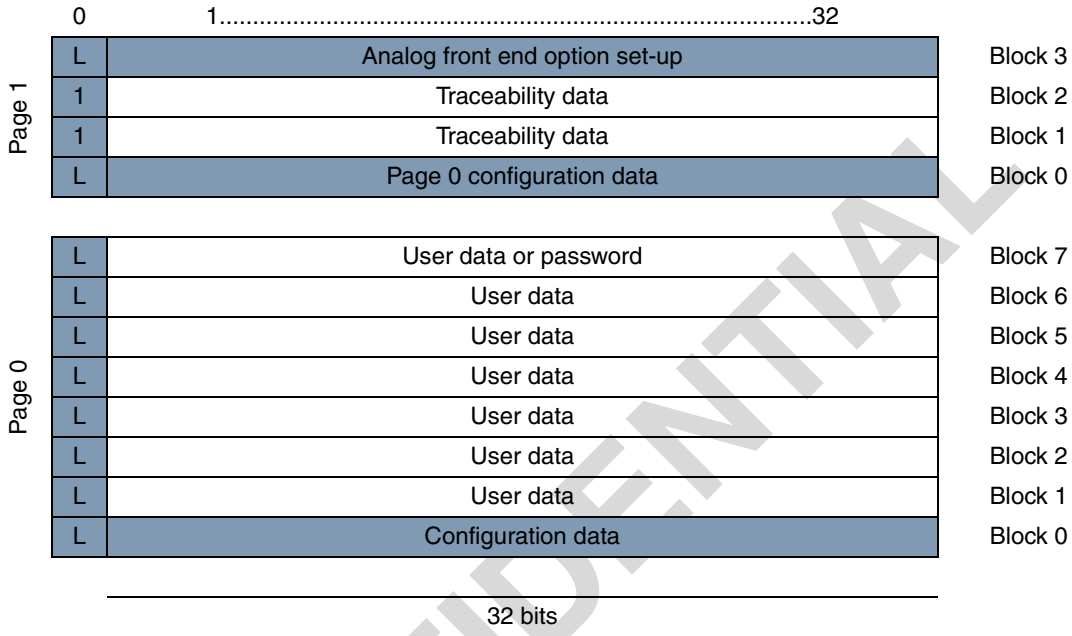
The mode register maintains a readable shadow copy of the configuration data held in block 0 of the EEPROM. It is continually refreshed during read mode and (re-)loaded after every POR event or reset command. On delivery, the mode register is pre-programmed according to Table 10-1 on page 40.

4.11 Modulator

The modulator encodes the serialized EEPROM data for transmission to a tag reader or base station. Several types of modulation are available including Manchester, bi-phase, FSK, PSK, and NRZ.

4.12 Memory

Figure 4-2. Memory Map



Not transmitted

The memory is a 363-bit EEPROM, which is arranged in 11 blocks of 33 bits each. Each block includes a single *Lock* bit, which is responsible for write-protecting the associated block. Programming takes place on a block basis, so a complete block (including lock bit) can be programmed with a single command. The memory is subdivided into two page areas. Page 0 contains 8 blocks and page 1 contains 3 blocks. All 33 bits of a block, including the lock bit, are programmed simultaneously.

Block 0 of page 0 contains the mode/configuration data, which is not transmitted during regular read operations. Addressing block 0 will always affect block 0 of page 0 regardless of the page selector. Block 7 of page 0 may be used as a protection password.

Block 3 of page 1 contains the analog front end option register, which is also not transmitted during regular-read operation.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lock bit itself) is not re-programmable via the RF field.

Blocks 1 and 2 of page 1 contain traceability data and are transmitted with the modulation parameters defined in the configuration register after the opcode “11” is issued by the reader (see Figure 5-10 and Figure 5-11 on page 21). The traceability data blocks are programmed and locked by Atmel.

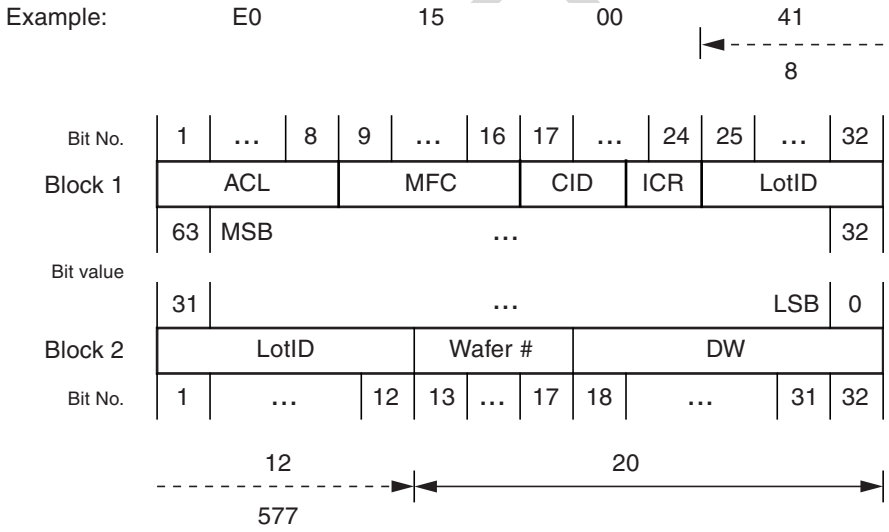
4.13 Traceability Data Structure/Unique ID

Blocks 1 and 2 of page 1 contain the traceability data and are programmed and locked by Atmel during production testing(1). The most significant byte of block 1 is fixed to E0h, the allocation class (ACL) as defined in ISO/IEC 15963-1. The second byte is therefore defined in ISO/IEC 7816-6 as Atmel's manufacturer ID (15h). The following 8 bits could be used as user ID (UID Bit 47 to 40). If not otherwise requested, the 5 most significant bits (customer identification CID) are by default reset (set to 00) as the Atmel standard value (other values may be assigned on request for high-volume customers) and the 3 least significant bits (IC revision, ICR) are used by Atmel for the IC and/or foundry version of the ATA5577.

The lower 40 bits of the data encode Atmel's traceability information and conform to a unique numbering system (unique ID). These 40 data bits are divided in two sub-groups, a 5-digit BCD-coded lot-ID number (LotID, 20 bits) and the binary wafer number (wafer#, 5 bits) concatenated with the sequential die number on wafer (DW,15 bits).

Note: 1. This is only valid for sawn wafer on foil delivery.

Figure 4-3. ATA5577 Traceability Data Structure



ACL	Allocation class as defined in ISO/IEC 15963-1 = E0h
MFC	Atmel Corporation's manufacturer code as defined in ISO/IEC 7816-6 = 15h
UID	User ID, on request (otherwise 5-bit CID and 3-bit ICR)
LotID	5-digit BCD encoded lot number, e.g., '41577'
Wafer#	5 bits for wafer number
DW	15 bits designating sequential die number on wafer

5. Operating the ATA5577

5.1 Configuring the ATA5577

Table 5-1. Block 3 Page 1– Analog Front End Option Set-up

L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
																							0	0	0	0	0	0	0	0	0	0

Lock Bit

0	Unlocked
1	Locked

Option Key[1]

Soft Modulation

Off	0	0	0
One pulse weak	0	1	0
One pulse strong	1	0	0
Two pulses	1	1	0
Smooth	1	1	1

Clamp Voltage

Clamp med typ[2]. 6 V_p	0	0
RFU	0	1
Clamp low typ[2]. 5 V_p	1	0
Clamp high typ[2]. 8 V_p	1	1

Modulation Voltage

Mod med typ[2]. 2 V_p	0	0
RFU	0	1
Mod low typ[2]. 1 V_p	1	0
Mod high typ[2]. 3 V_p	1	1

Clock-detection Threshold

Clkdet med typ. 550 mVp	0	0
RFU	0	1
Clkdet low typ. 250 mV_p	1	0
Clkdet high typ. 800 mV_p	1	1

Gap-detection Threshold

Gapdet med typ. 550 mV_p	0	0
RFU	0	1
Gapdet low typ. 250 mV_p	1	0
Gapdet high typ. 850 mV_p	1	1

Write Damping

0	0	0	WD + low att.
0	0	1	WD + high att.
0	1	0	Low att.
0	1	1	High att.
1	0	0	WD only
1	0	1	Off
1	1	0	RFU
1	1	1	RFU

Demod Delay

0	0	None
0	1	One pulse
1	0	Two pulses
1	1	RFU

Downlink Protocol

0	0	Fixed Bit Length
0	1	Long Leading Reference
1	0	Leading Zero Reference
1	1	1 of 4 Coding Reference

Reserved for Future Use (RFU)

Notes: 1. If *Option Key* is 6 or 9, the front end options are activated; for all other values they take on the default state (all 0). If *Option Key* is 6 then the complete page 1 (i.e., option register and traceability data) cannot be overwritten by any Test Write Command. This means, if the *Lock* bits of the three blocks of page 1 are set and the *Option Key* is 6, then all of page 1's blocks are locked against change.

2. Weak field condition

Table 5-2. Block 0 Page 0 – Configuration Mapping in Basic Mode

L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
					0	0	0	0	0	0	0				0									0						0	0	
Lock Bit	Master Key (1), (2)											Data Bit Rate					Modulation				PSKCF		AOR		MAX BLOCK			PWD	ST Sequence Terminator			Init Delay

Lock Bit	
0	Unlocked
1	Locked

Data Bit Rate			
RF/8	0	0	0
RF/16	0	0	1
RF/32	0	1	0
RF/40	0	1	1
RF/50	1	0	0
RF/64	1	0	1
RF/100	1	1	0
RF/128	1	1	1

PSKCF		AOR
0	0	RF/2
0	1	RF/4
1	0	RF/8
1	1	Res.

Modulation					
0	0	0	0	0	Direct
0	0	0	0	1	PSK1
0	0	0	1	0	PSK2
0	0	0	1	1	PSK3
0	0	1	0	0	FSK1
0	0	1	0	1	FSK2
0	0	1	1	0	FSK1a
0	0	1	1	1	FSK2a
0	1	0	0	0	Manchester
1	0	0	0	0	Bi-phase
1	1	0	0	0	Reserved

Notes: 1. If *Master Key* is 6 the test mode access is disabled
2. If *Master Key* is neither 6 nor 9, the extended function mode and *Init Delay* are disabled

Table 5-3. Block 0 Page 0 – Configuration Map in Extended Mode (*X-mode*)

L	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
					0	0	0	0							1																	
Lock Bit	Master Key(1), (2)								n5	n4	n3	n2	n1	n0	X-mode	Modulation					PSK-CF		AOR	OTP	MAX-BLOCK			PWD	Seq. Start Marker	Fast Downlink	Inverse Data	Init Delay
									Data Bit Rate RF/(2n+2)																							

Lock Bit	
0	Unlocked
1	Locked

Modulation					
0	0	0	0	0	Direct
0	0	0	0	1	PSK1
0	0	0	1	0	PSK2
0	0	0	1	1	PSK3
0	0	1	0	0	FSK1
0	0	1	0	1	FSK2
0	1	0	0	0	Manchester
1	0	0	0	0	Bi-phase
1	1	0	0	0	Differential bi-phase

PSK-CF		AOR
0	0	RF/2
0	1	RF/4
1	0	RF/8
1	1	Res.

Note: 1. If *Master Key* is 6 and bit 15 is set, the test mode access is disabled and the extended mode is active
2. If *Master Key* is 9 and bit 15 is set, the extended mode is enabled

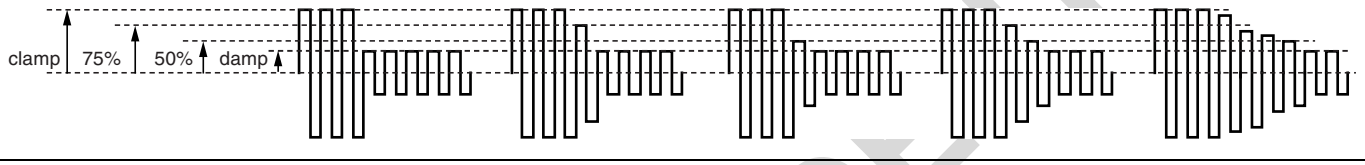
5.2 Soft Modulation Switching

Abrupt rise of the modulation signal at the beginning of modulation - especially in applications with high quality antennas - could lead to clock losses and therefore timing violations. To prevent this, several *soft modulation* settings can be chosen for a soft transition into the modulation state.

Soft modulation should only be used in combination with modulation schemes and data rates which do not involve high frequency modulation changes.

Table 5-4. Soft Modulation Switching Scheme

Bit 5-7 (bl3 p1)	000	010	100	110	111
Description	No soft modulation	One pulse weak	One pulse strong	Two pulses	Smooth

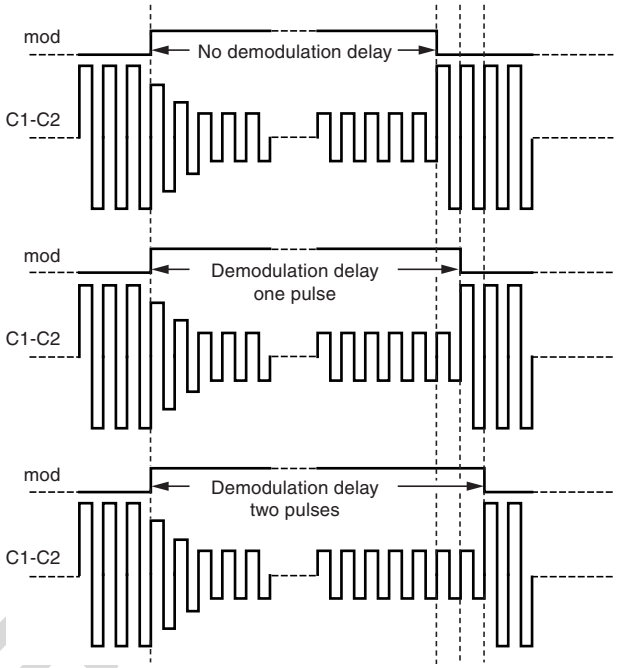


5.3 Demodulation Delay

Soft modulation will cause imbalance in modulated and unmodulated phases. Depending on the soft-modulation setting, the unmodulated phase can be longer than the modulated. To balance out this mismatch, the switch-point from the modulated to the unmodulated phase can be delayed for one or two pulses.

These delays and soft modulation switching should only be used in combination with modulation schemes and data rates which do not involve high frequency-modulation changes.

Table 5-5. Demodulation Delay Scheme

Bits 19 and 20 (bl3 p1)	Description
00	
01	
10	

5.4 Write Damping

Reader to Tag communication is initialized by sending a start-gap from the reader station. To ease gap detection respective to detect subsequent field-gaps reliably by default the receive damping and the low attenuation is activated.

Especially in combination with high quality coils a higher attenuation factor can be switched on, to fasten the relaxation time.

Using antenna-coils with low Q-factor it might be feasible to switch off the write damping. This results to better energy balance and therefore improved write distance.

5.5 Initialization and Init-Delay

The Power-On-Reset (POR) circuit remains active until an adequate voltage threshold has been reached. This, in turn, triggers the default initialization delay sequence. During this configuration period of about 192 field clocks, the ATA5577 is initialized with the configuration data stored in EEPROM block 0 and with the options stored in block 3 page 1. There are two variants of the ATA5577 implemented (see Section 10. “Ordering Information” on page 39). The variant of the ATA5577 with *damping during initialization* shows permanent damping during initialization (see Figure 5-9 on page 20). This prevents the tag from generating a power on reset at the edge of operating distance. This improves the stability of operation in all applications where maximum read range is not required. The ATA5577 types without damping achieve a longer read range based on the lower activation field strength.

Tag modulation in regular-read mode will be observed about 3 ms after entering the RF field. If the *Init-delay* bit is set, the ATA5577 variant with *damping during initialization* remains in a permanent damping state for t ~ 69 ms at f = 125 kHz. The ATA5577 variant without damping will start modulation after t ~ 69 ms without damping.

- Init-delay = 0: $T_{INIT} = 192 \times T_C + T_{POR}$ ~ 3 ms; T_C = 8 µs at f = 125 kHz (T_{POR} denotes delay for POR and depends on environmental conditions)
- Init-delay = 1: $T_{INIT} = (192 + 8192) \times T_C + T_{POR}$ ~ 69 ms;

Any field gap occurring during this initialization phase will restart the complete sequence. After this initialization time, the ATA5577 enters regular-read mode and modulation starts automatically using the parameters defined in the configuration register.

5.6 Modulator in Basic Mode

The modulator consists of data encoders for the following types of modulation in Basic mode:

Table 5-6. Types of Modulation in Basic Mode

Mode	Direct Data Output		
FSK1a[1]	FSK/8 - FSK/5	0 = RF/8	1 = RF/5
FSK2a[1]	FSK/8 - FSK/10	0 = RF/8	1 = RF/10
FSK1[1]	FSK/5 - FSK/8	0 = RF/5	1 = RF/8
FSK2[1]	FSK/10 - FSK/ 8	0 = RF/10	1 = RF/8
PSK1[2]	Phase change when input changes		
PSK2[2]	Phase change on bit clock if input high		
PSK3[2]	Phase change on rising edge of input		
Manchester	0 = falling edge, 1 = rising edge		
Bi-phase	1 creates an additional mid-bit change		
NRZ	1 = damping on, 0 = damping off		

Notes: 1. A common multiple of bit rate and FSK frequencies is recommended.
2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub carrier frequency.

5.7 Maxblock

After entering regular-read mode the ATA5577 transmits the data content starting with block 1. The MAXBLK setting defines how many data blocks will be transmitted.

5.8 Password

When password mode is active (PWD = 1), the first 32 bits after the opcode are regarded as the password. They are compared bit by bit with the contents of block 7, starting at bit 1. If the comparison fails, the ATA5577 will not program the memory, instead it will restart in regular-read mode once the command transmission is finished.

Note: In password mode, MAXBLK should be set to a value lower than 7 to prevent the password from being transmitted by the ATA5577.

Each transmission of the direct access command (two opcode bits, 32-bit password, '0' bit plus 3 address bits = 38 bits) needs about 18 ms. Testing all possible combinations (about 4.3 billion) would take about two years.

5.9 Answer-On-Request (AOR) Mode

When the AOR bit in the configuration register is set the ATA5577 does not start modulation in the regular-read mode after loading configuration block 0. The tag waits for a valid AOR data stream (*wake-up command*) from the reader before modulation is enabled. The wake-up command consists of the opcode (“10” or “11”) followed by a valid password. The selected tag will remain active until the RF field is turned off or a new command with a different password is transmitted, which may address another tag in the RF field.

Table 5-7. ATA5577 - Modes of Operation

PWD	AOR	Behavior of Tag after Reset Command or POR	De-activate Function
1	1	Answer-On-Request (AOR) mode: - Modulation starts after wake-up with a matching password - Programming needs valid password	Command with non-matching password deactivates the selected tag
1	0	Password mode: - Modulation in regular-read mode starts after reset - Programming and direct access needs valid password	
0	-	Normal mode: - Modulation in regular-read mode starts after reset - Programming and direct access without password	

Figure 5-1. Answer-On-Request (AOR) Mode, For Example, Fixed Bit-length Protocol

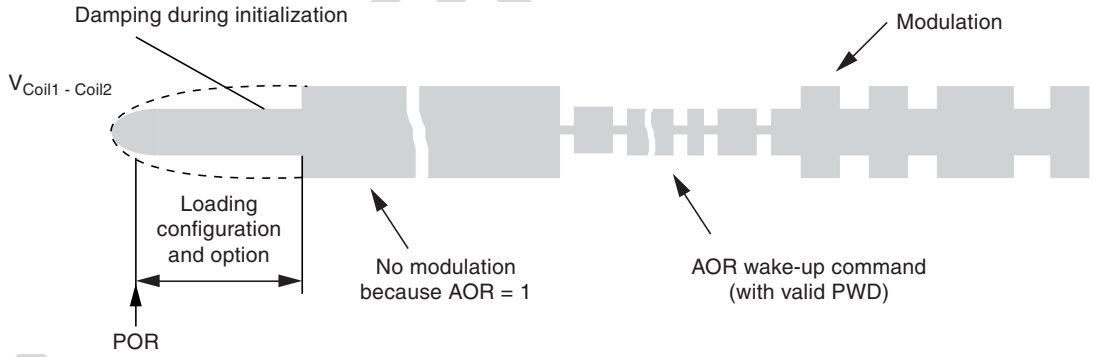
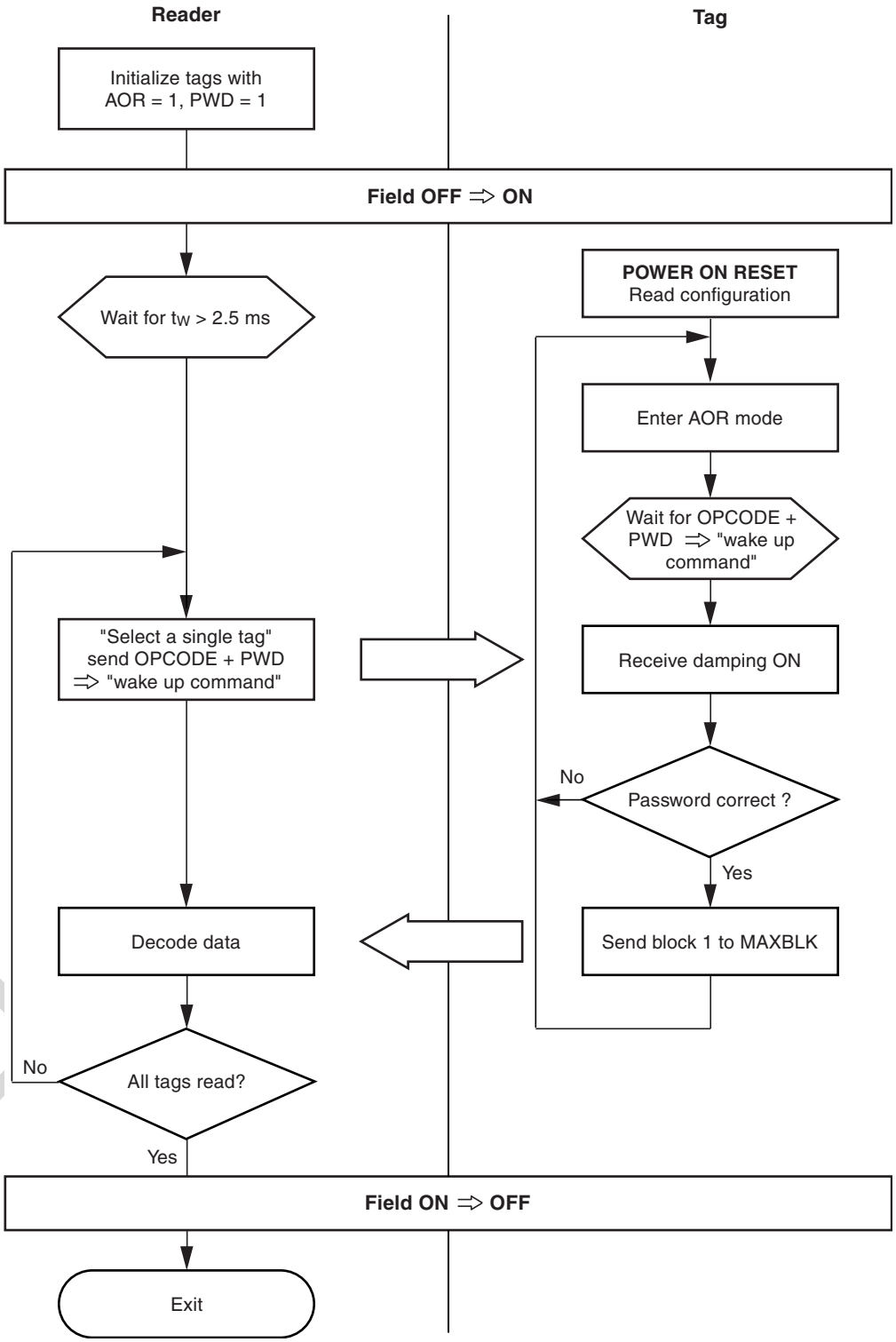


Figure 5-2. Anticollision Procedure Using AOR Mode



5.10 ATA5577 in Extended Mode (X-mode)

In general, setting of the master key (bits 1 to 4) of block 0 to the value 6 or 9 together with the X-mode bit will enable the extended mode functions such as the *binary bit-rate generator*, *OTP functionality*, *fast downlink*, *inverse data output* and *sequence start marker*.

- Master key = 9: Test mode access and extended mode are both enabled.
- Master key = 6: Any test mode access will be denied but the extended mode is still enabled.

Any other master key setting will prevent the activation of the ATA5577 extended mode options, even when the X-mode bit is set.

5.10.1 Modulator in Extended-Mode

Table 5-8. ATA5577 Types of Modulation in Extended Mode

Mode	Direct Data Output Encoding	Inverse Data Output Encoding
FSK1(1)	FSK/5 - FSK/8 0 = RF/5; 1 = RF/8	FSK/8 - FSK/5 0 = RF/8; 1 = RF/5 (= FSK1a)
FSK2(1)	FSK/10 - FSK/8 0 = RF/10; 1 = RF/8	FSK/8 - FSK/10 0 = RF/8; 1 = RF/10 (= FSK2a)
PSK1(2)	Phase change when input changes	Phase change when input changes
PSK2(2)	Phase change on bit clock if input high	Phase change on bit clock if input low
PSK3(2)	Phase change on rising edge of input	Phase change on falling edge of input
Manchester	0 = falling edge, 1 = rising edge mid bit	1 = falling edge, 0 = rising edge mid bit
Bi-phase	1 creates an additional mid-bit change	0 creates an additional mid-bit change
Differential bi-phase	0 creates an additional mid-bit change	1 creates an additional mid-bit change
NRZ	1 = damping on, 0 = damping off	0 = damping on, 1 = damping off

Notes: 1. A common multiple of bit rate and FSK frequencies is recommended.
2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

5.10.2 Binary Bit-rate Generator

In extended mode the data rate is binary programmable to operate at any even-numbered data rate between RF/2 and RF/128 as given in the formula below.

Data rate = RF / (2n + 2)

5.10.3 OTP Functionality

If the OTP bit is set to 1, all memory blocks are write protected and behave as if all lock bits are set to 1. If, in addition, the master key is set to 6, the ATA5577 mode of operation is locked forever (one-time-programming functionality).

If the master key is set to 9, the test-mode access allows the re-configuration of the tag.

5.10.4 Fast Downlink

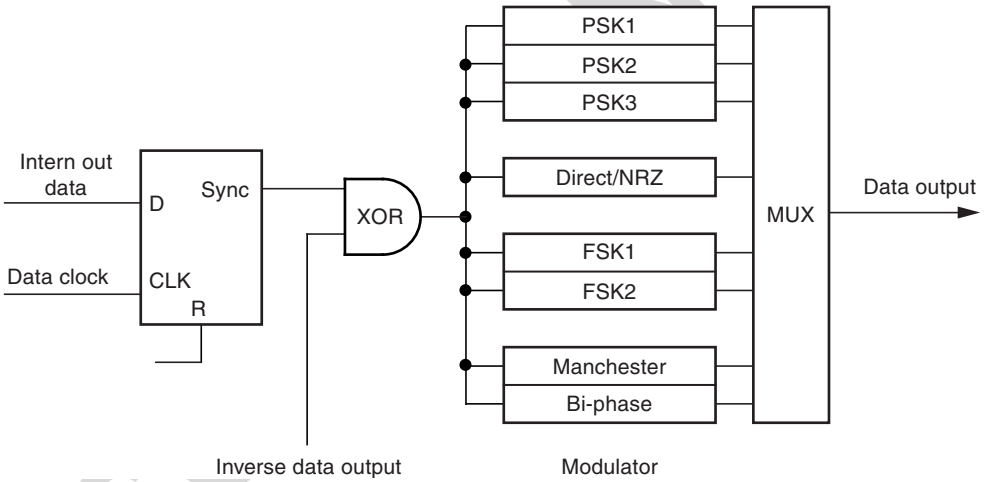
In the optional fast downlink mode, the time between two gaps is reduced. In the fixed bit length protocol mode, there are nominally 12 field clocks for a 0 and 28 field clocks for a 1. When there is no gap for more than 32 field clocks after a previous gap, the ATA5577 in the *Fixed Bit Length Protocol* mode will exit the downlink mode (refer to Table 5-10 on page 21).

For the timings in fast downlink mode of the long-leading-reference protocol refer to Table 5-11 on page 22, for the leading-zero-reference protocol to Table 5-12 on page 23 and for the 1-of-4-coding protocol to Table 5-12 on page 23.

5.10.5 Inverse Data Output

In extended mode (X-mode), the ATA5577 supports an inverse data output option. If inverse data is enabled, the modulator as shown in Figure 5-3 works on inverted data (see Figure 5-8 on page 14). This function is supported for all basic types of encoding.

Figure 5-3. Data Encoder for Inverse Data Output



5.11 Tag to Reader Communication

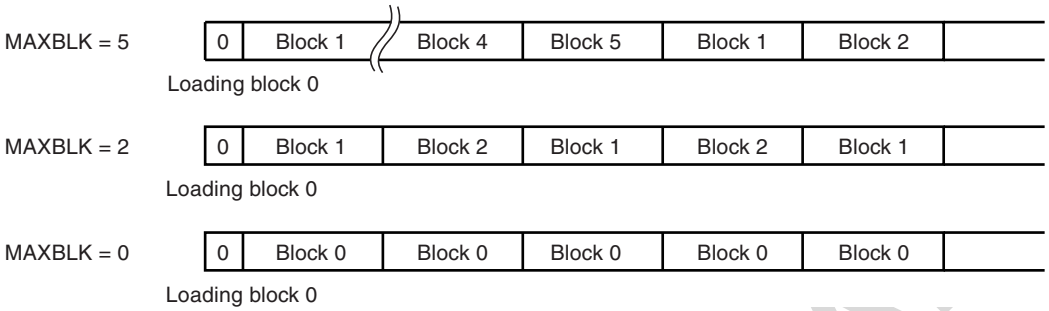
During read operation (Uplink mode), the data stored within the EEPROM is cycled and the Coil 1 and Coil 2 terminals are load modulated. This resistive load modulation can be detected at the reader device.

5.11.1 Regular-read Mode

In regular-read mode, data from the memory is transmitted serially, starting with block 1, bit 1, up to the last block (for example, 7), bit 32. The last block which will be read is defined by the mode parameter field MAXBLK in EEPROM block 0. When the data block addressed by MAXBLK has been read, data transmission restarts with block 1, bit 1.

The user may limit the cyclic data stream in regular-read mode by setting the MAXBLK between 0 and 7 (representing each of the 8 data blocks). If set to 7, blocks 1 through 7 can be read. If set to 1, only block 1 is transmitted continuously. If set to 0, the contents of the configuration block (normally not transmitted) can be read. In the case of MAXBLK = 0 or 1, regular-read mode can not be distinguished from block-read mode.

Figure 5-4. Examples for Different MAXBLK Settings



Every time the ATA5577 enters regular- or block-read mode, the first bit transmitted is a logical 0. The data stream starts with block 1, bit 1 and continues through MAXBLK, bit 32 and, if in regular-read mode, cycles continuously.

Note: This behavior is different from the original e555x and helps to decode PSK-modulated data.

5.11.2 Block-read Mode

With the direct-access command, only the addressed block is read repetitively. This mode is called block-read mode. Direct access is entered by transmitting the page access opcode (“10” or “11”), a single 0 and the requested 3-bit block address when the tag is in normal mode.

In password mode (PWD bit set), the direct access to a single block needs the valid 32-bit password to be transmitted after the page access opcode followed by a 0 and the 3-bit block address. If the transmitted password does not match the contents of block 7, the ATA5577 tag returns to regular-read mode.

Note: A direct access to block 0 of page 1 will read the configuration data of block 0, page 0.
A direct access to block 4 to 7 of page 1 reads all data bits as zero.

5.11.3 Sequence Terminator (Basic Mode)

The sequence terminator (ST) is a special damping pattern which is inserted in front of the first block and may be used to synchronize the reader. This sequence terminator is recommended only for FSK and Manchester coding. This Basic mode sequence terminator consists of four bit periods. During the first and third bit period, the data value is 1. During the second and the fourth bit period, modulation is switched off (using Manchester encoding, switched on).

Bi-phase modulated data blocks need fixed leading and trailing bits in combination with the sequence terminator to be reliably identified.

The sequence terminator may be individually enabled by setting the mode bit 29 (ST = 1) in Basic mode (X-mode = 0).

In the regular-read mode, the sequence terminator is inserted at the start of each MAXBLK- limited read data stream.

In block-read mode - after any block-write or direct access command - or if MAXBLK was set to 1, the sequence terminator is inserted before the transmission of the selected block.

Especially this behavior is different to former ICs (e5551/T5551, T5554). For further details refer to relevant application notes.

Figure 5-5. Read Data Stream with Sequence Terminator

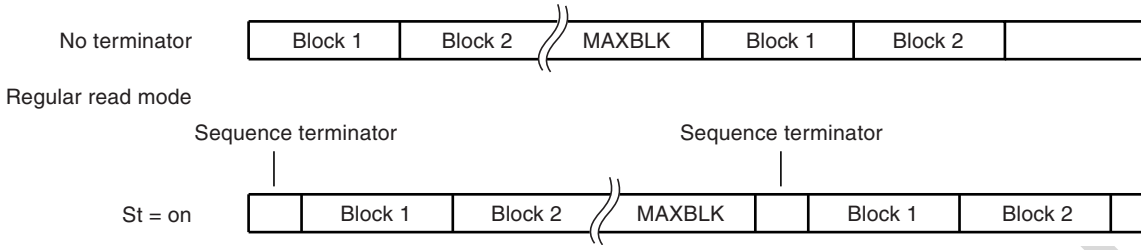
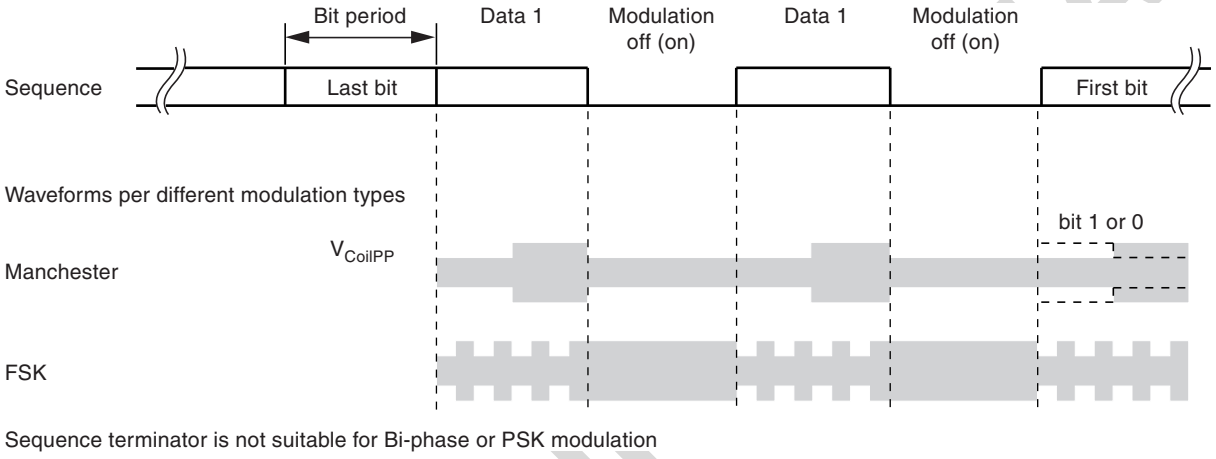


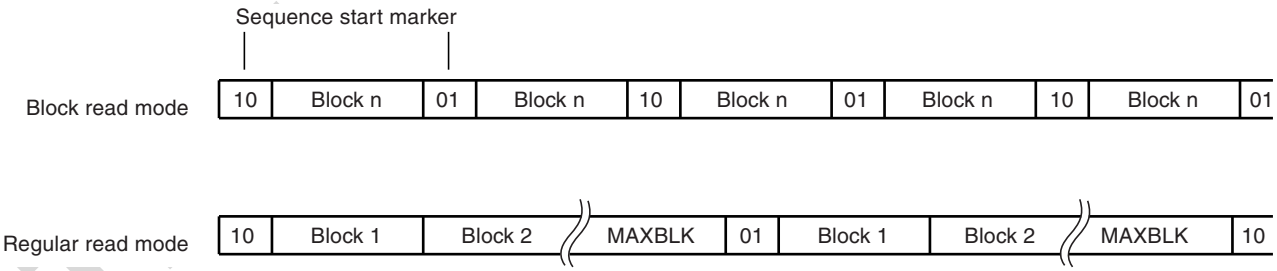
Figure 5-6. Basic Mode Sequence Terminator Waveforms



5.11.4 Sequence Start Marker (X-mode)

The ATA5577 sequence start marker is a special damping pattern in Extended mode, which may be used to synchronize the reader. The sequence start marker consists of two bits (“01” or “10”) which are inserted as header before the first block to be transmitted if in extended mode bit 29 is set. At the start of a new block sequence, the value of the two bits is inverted.

Figure 5-7. ATA5577 Sequence Start Marker in Extended Mode



5.12 Reader to Tag Communication

Data is transmitted to the tag by interrupting the RF field with short field gaps (on-off keying) in accordance with the T5557/ATA5567 write method (Downlink mode). The duration of these field gaps is, for example, 100 µs. The time between two gaps encodes the 0/1 information to be transmitted (pulse interval encoding). There are four different downlink protocols available, which are selectable via bit 21 and bit 22 in the option register block 3 page 1 (see Table 5-1 on page 7). Choosing the default downlink protocol (fixed-bit-length protocol), the time between two gaps is nominally 24 field clocks for a 0 and 56 field clocks for a 1. When there is no gap for more than 64 field clocks after a previous gap, the ATA5577 exits the downlink mode. The tag starts with the command execution if the correct number of bits were received. If a failure is detected, the ATA5577 does not continue and enters regular-read mode.

Improved downlink performance could be achieved by choosing self-calibrating downlink protocols. The ATA5577 offers three different possibilities to get a better performance using self-calibrating downlink protocols:

- Long leading reference:
  Fully forward and backward compatible with former tags and readers.
- Leading zero:
  A reader has to send a leading zero in front of the downlink bit stream. This leading zero serves as a reference for the following zero and one bits.
- 1 of 4 coding:
  Compact downlink protocol with optimized energy balance

5.12.1 Start Gap

The initial gap is referred to as the start gap. This triggers the reader-to-tag communication. In the option register (block 3 page 1) several settings can be chosen to ease gap detection during this mode of operation, for example, the receive damping can be activated (see Table 5-1 on page 7). The start gap may need to be longer than subsequent gaps — so-called *write gaps* — in order to be detected reliably.

A start gap will be accepted at any time after the mode register has been loaded (≥ 3 ms). A single gap will not change the previously selected page (by a previous opcode “10” or “11”).

Figure 5-8. Start of Reader-to-tag Communication

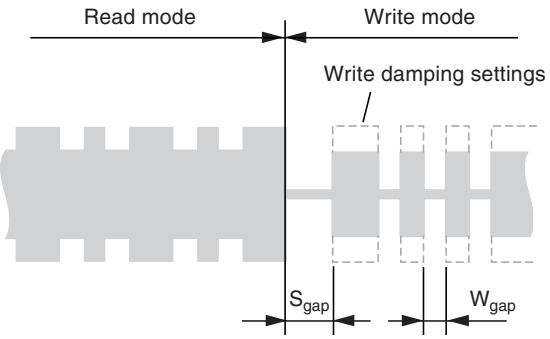


Table 5-9. Gap Scheme

Parameters	Remark	Symbol	Min.	Max.	Unit
Start gap		S_{gap}	8	50	T_C
Write gap	Normal downlink mode	W_{gap}	8	20	T_C

Note: All absolute times assume $T_C = 1 / f_C = 8$ µs ($f_C = 125$ kHz)

5.12.2 Downlink Data Protocols

The ATA5577 expects to receive a dual-bit opcode as a part of a reader command sequence. There are three valid opcodes:

- The opcode “10” precedes all downlink operations for page 0.
- The opcode “11” precedes all downlink operations for page 1. Performing a direct access command on block 0 always provides block 0 page 0 independently of the page selector (see Figure 4-2 on page 5).
- The RESET opcode “00” initiates an initialization cycle

The fourth opcode “01” precedes all test mode write operations. Any test mode access is ignored after master key (bits 1 to 4) in block 0 has been set to “6”. Any further modifications of the master key are prohibited by setting the lock bit of block 0 or the OTP bit.

Downlink has to follow these rules:

- Standard write needs the opcode, the lock bit, 32 data bits and the 3-bit address (38 bits total)
- Protected write (PWD bit set) requires a valid 32-bit password between the opcode and the data and address bits
  Protected write (PWD bit set) in conjunction with the leading-zero-reference protocol or with the 1-of-4-coding protocol requires two padding zero bits between the opcode and the password (see also Figure 5-17 on page 26). This ensures the uniqueness of the *direct access with password* and the *standard write* command (see also Table 6-1 on page 27).
- For the AOR wake-up command an opcode and a valid password are necessary to select and activate a specific tag

Note: The data bits are read in the same order as written.

If the transmitted command sequence is invalid, the ATA5577 enters regular-read mode with the previously selected page (by previous opcode “10” or “11”).

Figure 5-9. Complete Writing Sequence with Fixed-bit-length Protocol

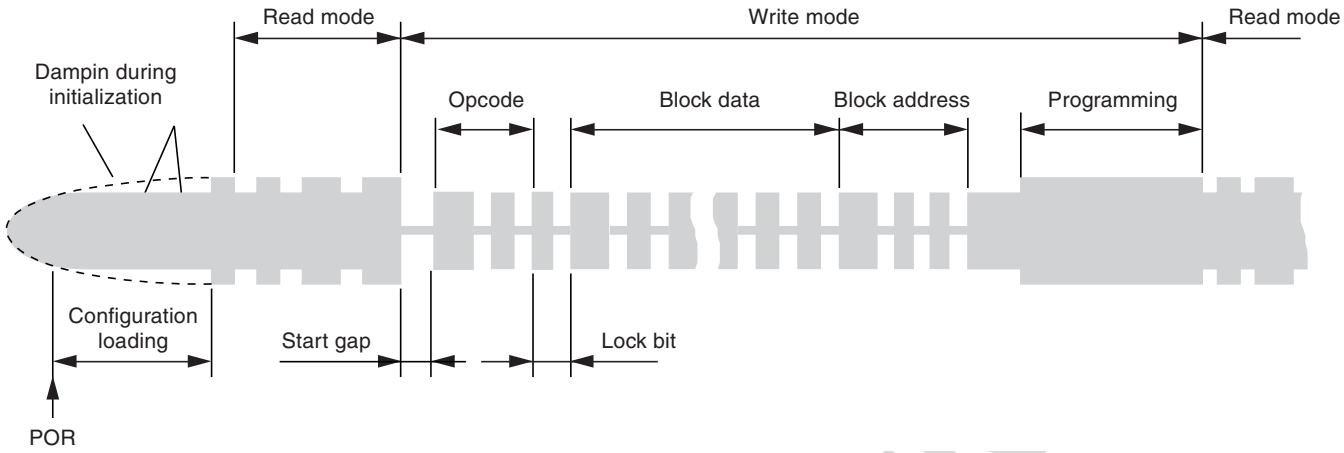


Figure 5-10. ATA5577 Command Formats Fixed-bit-length Protocol and Long-leading-reference Protocol

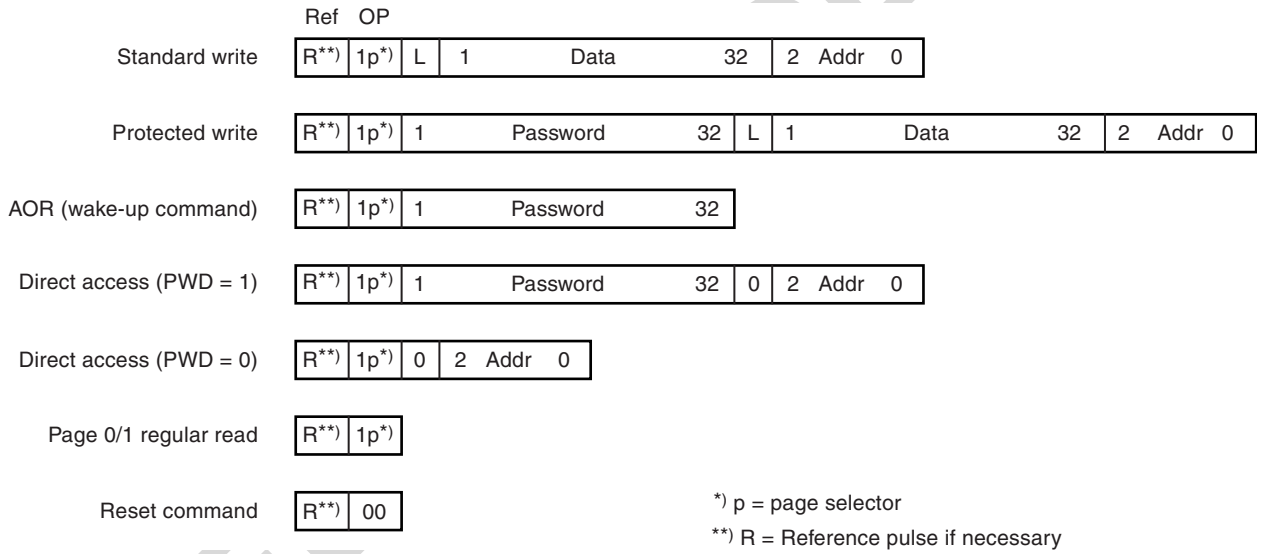
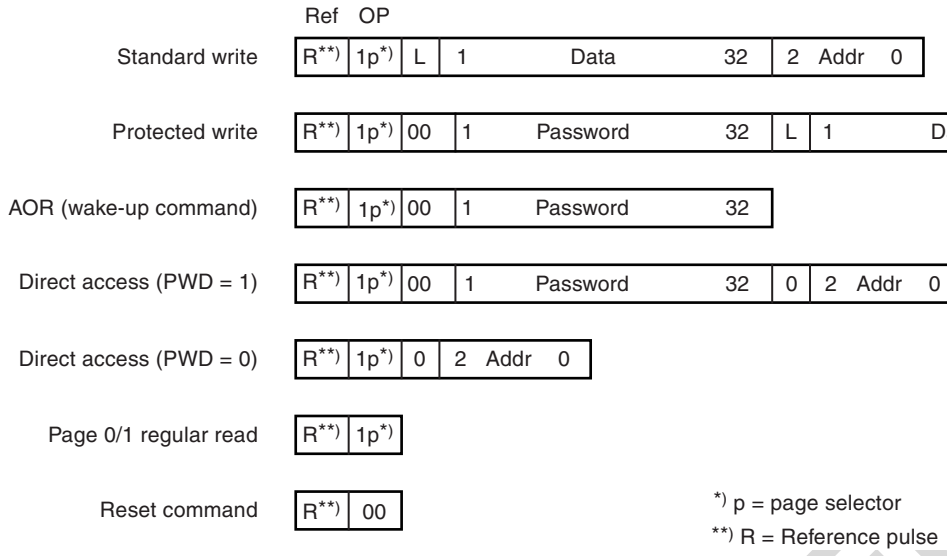


Figure 5-11. ATA5577 Command Formats Leading-zero-reference Protocol and 1-of-4-coding Protocol



5.12.3 Fixed-bit-length Protocol

In the fixed-bit-length protocol, the time between two gaps is nominally 24 field clocks for a 0 and 56 field clocks for a 1. When there is no gap for more than 64 field clocks after a previous gap, the ATA5577 exits the downlink mode. This protocol is compatible to the T5557/ATA5567 transponder.

Table 5-10. Downlink Data Coding Scheme with Fixed-bit-length Protocol

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap		S_{gap}	8	15	50	8	15	50	T_c
Write gap		W_{gap}	8	10	20	8	10	20	T_c
Write data coding (gap separation)	0 data	d_0	16	24	32	8	12	16	T_c
	1 data	d_1	48	56	64	24	28	32	T_c

Note: All absolute times assume $T_C = 1 / f_C = 8$ µs ($f_C = 125$ kHz)

Figure 5-12. Fixed Bit Length Protocol

5.12.4 Long-leading-reference Protocol

To achieve better downlink performance, an enhanced ATA5577 reader places a reference pulse in front of the opcode. This reference pulse is used as a timing reference for all following data, thus providing an auto-adjustment for varying environmental conditions. The long-leading-reference protocol allows full compatibility and coexistence of both T5557/ATA5567 and ATA5577 devices with both T5557/ATA5567 compatible readers and advanced ATA5577 readers. However, only the ATA5577 devices can profit from the self-calibration and the resultant increase in write distance (see Table 5-1 on page 7 for option register settings).

In this mode, the reference pulse in front of the command is monitored. Depending on its length, the remainder of the command is either evaluated using the fixed-bit-length protocol or this pulse is used as a measurement reference to evaluate the following command bits. Otherwise the following bits are considered as an invalid command.

a) For a reference-based command, the reference pulse (d_{Ref}) will have a length of 16 to 32 + 136 = 152 to 168 field clocks (zero bit + timing bias = reference pulse). Hence the expected length will lie between 152 and 168 field clocks. The equivalent expected zero bit length is then extracted and used as a reference for all following bits. The long-leading-reference pulse in this case is used as a timing reference only and does not contribute to the command data itself (see Figure 5-13, part a on page 23).

b) should the first bit lie within the *fixed bit length* frame (for example in normal mode: 0: 16 to 32 clocks; 1: 48 to 64 clocks) the device will then automatically switch to the fixed-bit-length protocol (see Section 5.12.3 “Fixed-bit-length Protocol” on page 21) and this first pulse will be evaluated as the first command bit. This allows compatibility with long-leading-reference programmed ATA5577 devices interacting with T5557/ATA5567 readers, which do not send any reference pulses (see Figure 5-13, part b on page 23).

c) If a T5557/ATA5567 device interacts with an enhanced ATA5577 reader, the reference pulse (152 to 168 field clocks) is ignored by the T5557/ATA5567 and the following data bits will evaluated correctly. Therefore a T5557/ATA5567 device is compatible with an enhanced ATA5577 reader (see Figure 5-13, part b on page 23).

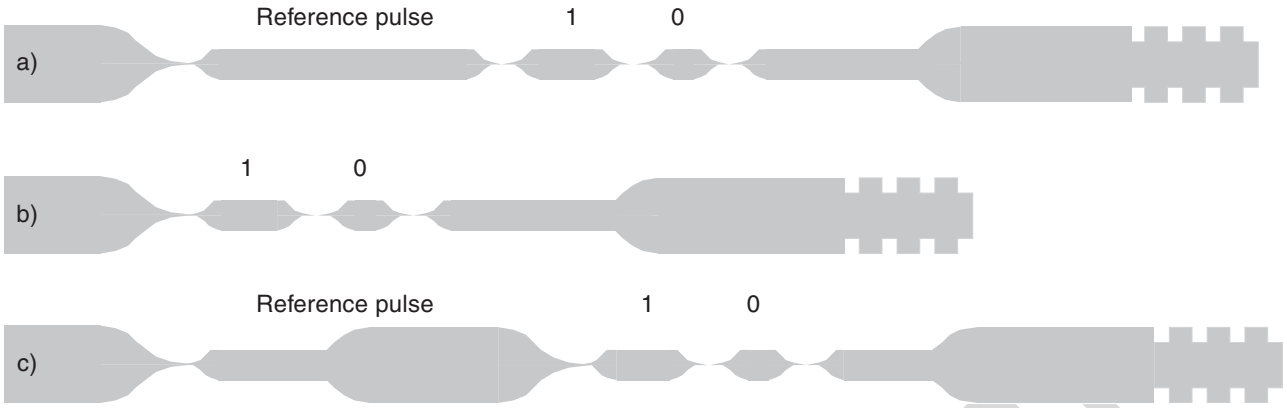
d) Should the first bit correspond to neither (a) nor (b) then it will be rejected as an invalid command.

Table 5-11. Downlink Data Coding Scheme with Long Leading Reference

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap		S_{gap}	8	15	50	8	15	50	T_c
Write gap		W_{gap}	8	10	20	8	10	20	T_c
Write data coding (gap separation)	Reference Pulse	d_{ref}	152	160	168	140	144	148	T_c
			136 clocks + 0 data bit			132 clocks + 0 data bit			
	0 data	d_0	d_{ref} – 143	d_{ref} – 136	d_{ref} – 128	d_{ref} – 135	d_{ref} – 132	d_{ref} – 124	T_c
	1 data	d_1	d_{ref} – 111	d_{ref} – 104	d_{ref} – 96	d_{ref} – 119	d_{ref} – 116	d_{ref} – 112	T_c

Note: All absolute times assume $T_C = 1 / f_C = 8$ µs ($f_C = 125$ kHz)

Figure 5-13. Long-leading-reference Protocol



5.12.5 Leading-zero-reference Protocol

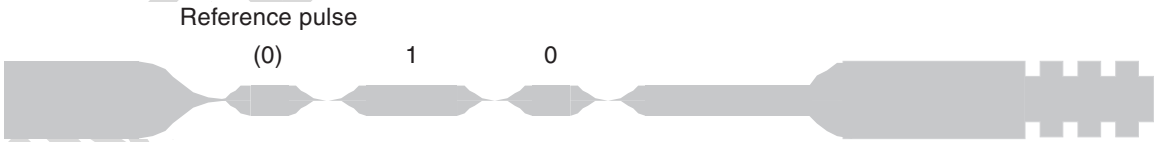
If the device is programmed in this mode it will always expect a reference pulse before the command data itself. This pulse length should correspond exactly to the length of the zero bits in the following command. All further lengths of the zero bits and one bits of the command are derived from the reference pulse. Therefore, downlink performance is optimal in different environmental conditions.

Table 5-12. Downlink Data Coding Scheme with Leading-zero Reference

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap		S_{gap}	8	15	50	8	15	50	T_c
Write gap		W_{gap}	8	10	20	8	10	20	T_c
Write data coding (gap separation)	Reference Pulse	d_{ref}	12	–	72	8	–	68	T_c
	0 data	d_0	$d_{ref} - 7$	d_{ref}	$d_{ref} + 8$	$d_{ref} - 3$	d_{ref}	$d_{ref} + 4$	T_c
	1 data	d_1	$d_{ref} + 9$	$d_{ref} + 16$	$d_{ref} + 24$	$d_{ref} + 5$	$d_{ref} + 8$	$d_{ref} + 12$	T_c

Note: All absolute times assume $T_C = 1 / f_C = 8$ µs ($f_C = 125$ kHz)

Figure 5-14. Leading Zero Reference Protocol



5.12.6 1-of-4-coding Protocol

This protocol codes the data in bit pairs so that the length of each packet can have one of four discrete lengths. This protocol is extremely compact and exhibits the least number of field gaps which in turn improves the device's ability to extract power from the field. Additionally a leading reference pulse "00" is placed in front of the downlink command. This serves as a reference pulse for all following data bits, thus providing an auto-adjustment for varying environmental conditions.

Table 5-13. Downlink Data Coding Scheme with 1-of-4 Coding

Parameter	Remark	Symbol	Normal Downlink			Fast Downlink			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Start gap		S_{gap}	8	15	50	8	15	50	T_c
Write gap		W_{gap}	8	10	20	8	10	20	T_c
Write data coding (gap separation)	Reference pulse "00"	d_{ref}	12	–	72	8	–	68	T_c
	"00" data	d_{00}	$d_{ref} - 7$	d_{ref}	$d_{ref} + 8$	$d_{ref} - 3$	d_{ref}	$d_{ref} + 4$	T_c
	"01" data	d_{01}	$d_{ref} + 9$	$d_{ref} + 16$	$d_{ref} + 24$	$d_{ref} + 5$	$d_{ref} + 8$	$d_{ref} + 12$	T_c
	"10" data	d_{10}	$d_{ref} + 25$	$d_{ref} + 32$	$d_{ref} + 40$	$d_{ref} + 13$	$d_{ref} + 16$	$d_{ref} + 20$	T_c
	"11" data	d_{11}	$d_{ref} + 41$	$d_{ref} + 48$	$d_{ref} + 56$	$d_{ref} + 21$	$d_{ref} + 24$	$d_{ref} + 28$	T_c

Note: All absolute times assume $T_C = 1 / f_C = 8$ µs ($f_C = 125$ kHz)

Figure 5-15. 1 of 4 Coding Protocol

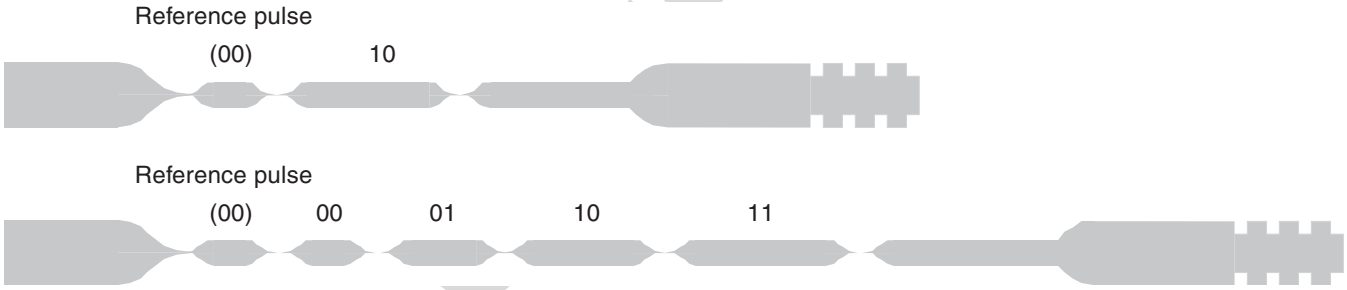
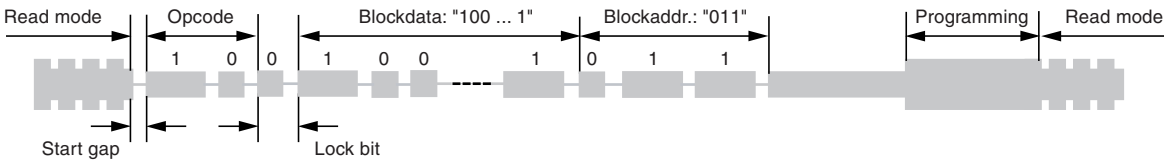
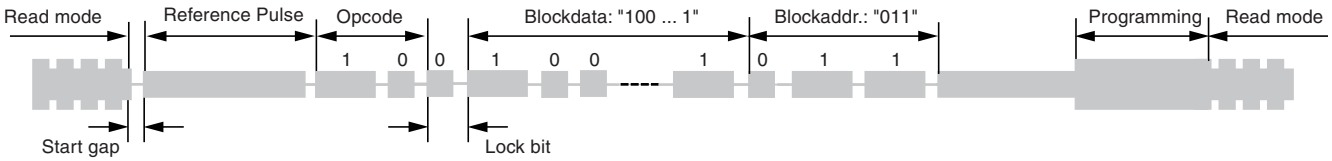


Figure 5-16. *Standard Write* Sequence Example

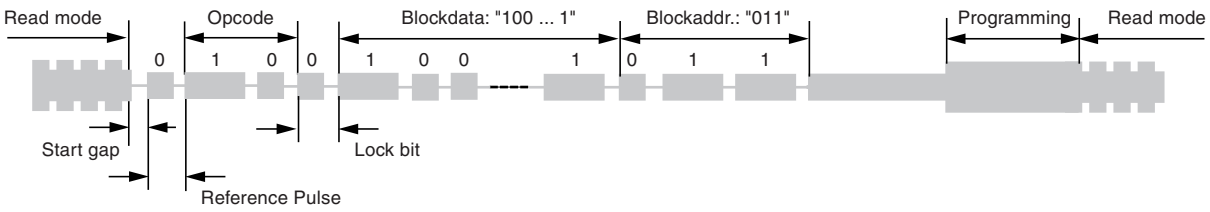
a) Fixed Bit Length Protocol



b) Long Leading Reference Protocol



c) Leading Zero Reference Protocol



d) 1 of 4 Coding Protocol

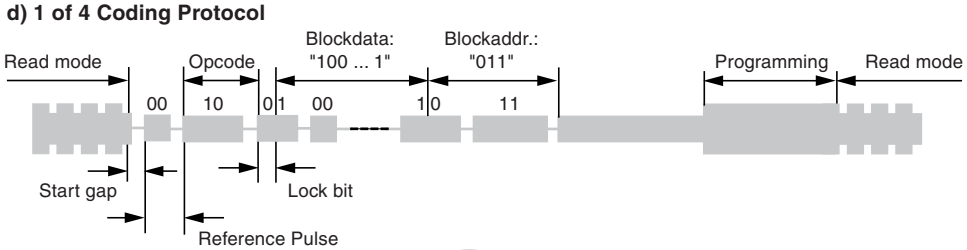
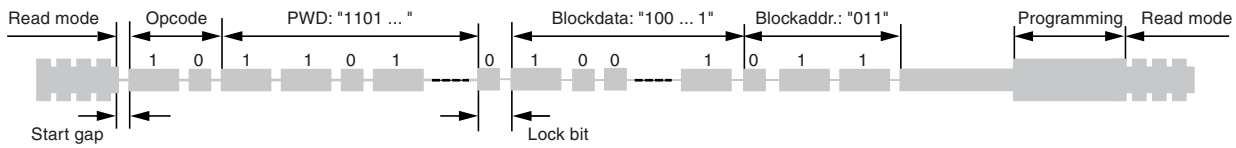
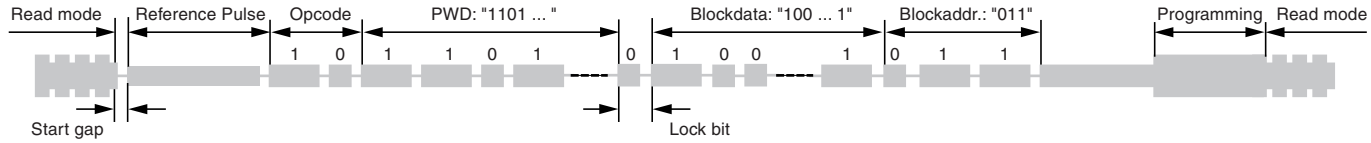


Figure 5-17. *Protected Write* Sequence Example

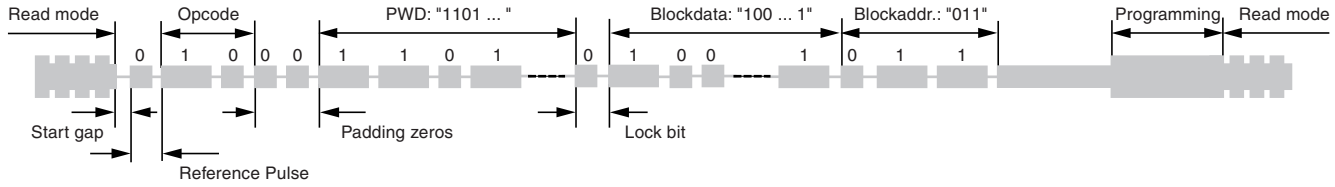
a) Fixed Bit Length Protocol



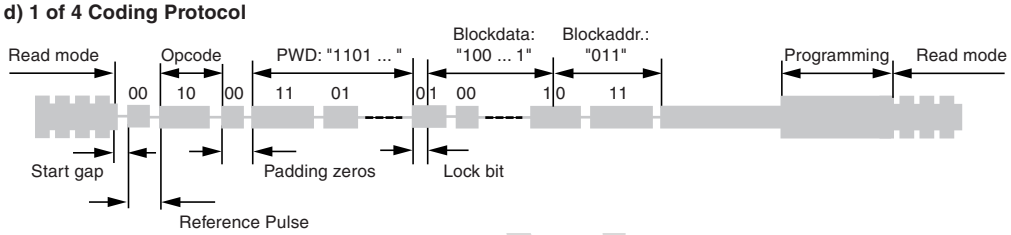
b) Long Leading Reference Protocol



c) Leading Zero Reference Protocol



d) 1 of 4 Coding Protocol



5.13 Programming

When all necessary information has been received by the ATA5577, programming may proceed. There is a clock delay between the end of the writing sequence and the start of programming.

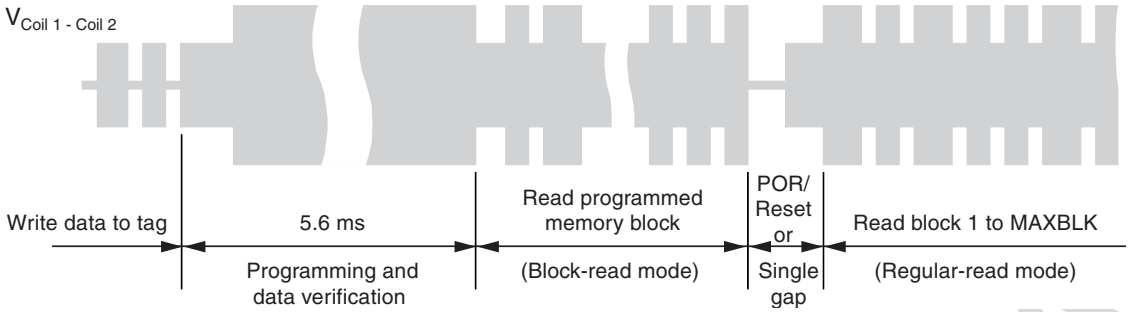
Typical programming time is 5.6 ms. This cycle includes a data verification read to grant secure and correct programming. After programming is successfully executed, the ATA5577 enters block-read mode, transmitting the block just programmed (see Figure 5-18 on page 27).

Note: This timing and behavior is different from the e555x-family predecessors. For further details refer to relevant Atmel application notes.

If the command sequence is validated and the addressed block is not write protected, the new data will be programmed into the EEPROM memory. The new state of the block write protection bit (lock bit) will be programmed at the same time accordingly.

Each programming cycle consists of four consecutive steps: erase block, erase verification (data = 0), programming, and write verification (corresponding data bits = 1).

Figure 5-18. Coil Voltage after Programming a Memory Block



Notes: 1. Programming of page 1 with following single gap will lead to a page 1 read. To enter regular-read mode, a POR or Reset command has to be performed.

6. Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

6.1 Errors During Command Sequence

The following detectable errors could occur sending a command sequence to the ATA5577:

- Wrong number of field clocks between two gaps (that is, not a valid 1 or 0 pulse stream)
- Password mode is activated and the password does not match the contents of block 7
- The number of bits received in the command sequence is incorrect

Valid bit counts accepted by the ATA5577 are:

Table 6-1. Bit Counts of Command Sequences

Command	Protect	Fixed-bit-length Protocol	Long-leading-reference Protocol	Leading-zero-reference Protocol	1-of-4-coding Protocol
Standard write	(PWD = 0)	38 bits	38 bits	38 bits	38 bits
Direct access	(PWD = 0)	6 bits	6 bits	6 bits	6 bits
Password write	(PWD = 1)	70 bits	70 bits	72 bits	72 bits
Direct access with PWD	(PWD = 1)	38 bits	38 bits	40 bits	40 bits
AOR wake-up	(PWD = 1)	34 bits	34 bits	36 bits	36 bits
Reset command		2 bits	2 bits	2 bits	2 bits
Page 0/1 regular read		2 bits	2 bits	2 bits	2 bits

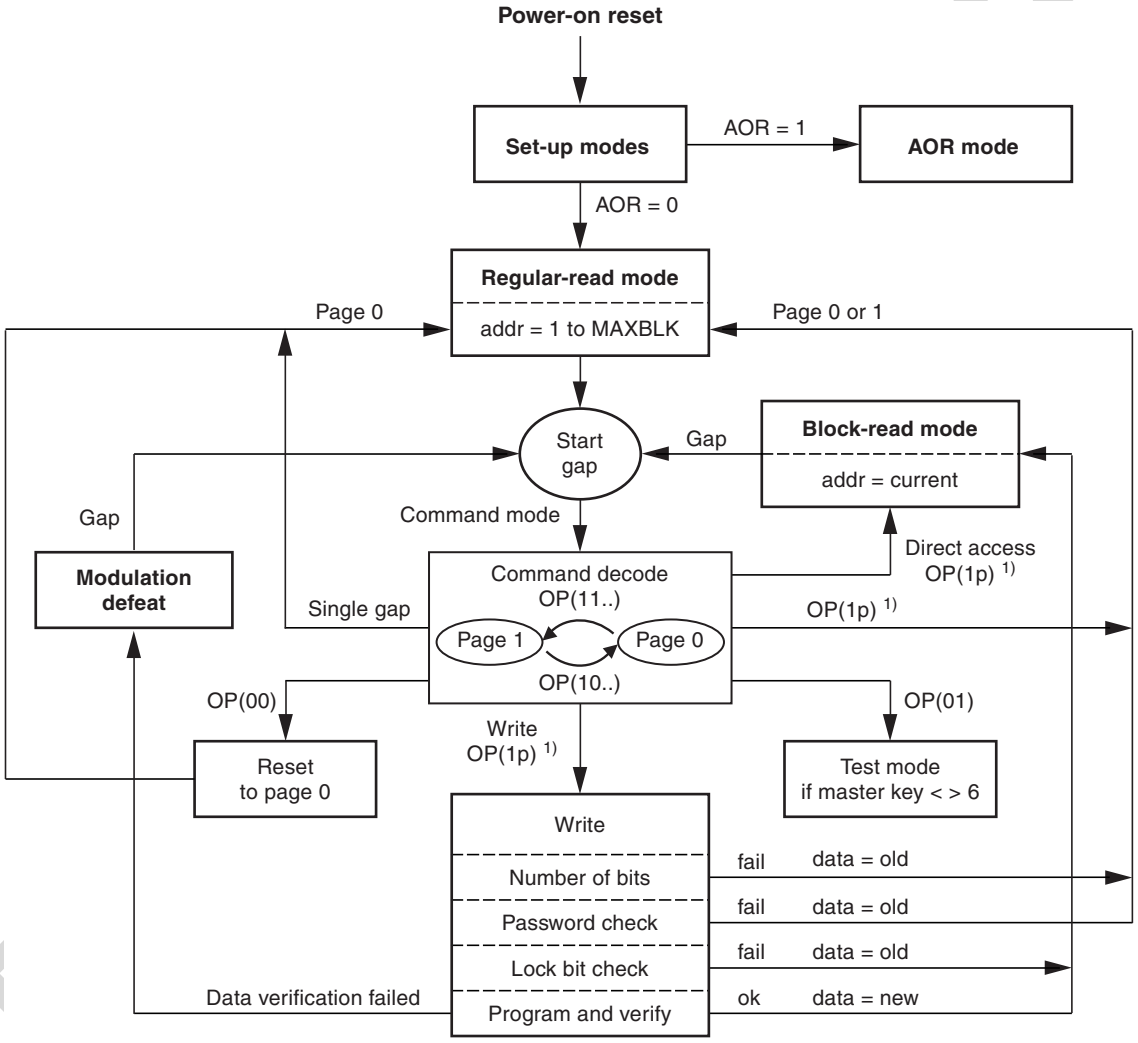
If any of these erroneous conditions (except AOR mode) are detected, the ATA5577 enters regular-read mode, starting with block 1 of the page defined in the command sequence. An erroneous AOR wake-up command will stop modulation (modulation defeat).

6.2 Errors Before/During Programming the EEPROM

If the command sequence was received successfully, the following error could still prevent programming:

- The lock bit of the addressed block is set already
- In case of a locked block, programming mode will not be entered. The ATA5577 reverts to block-read mode continuously transmitting the currently addressed block.
- If a data verification error is detected after an executed data block programming, the tag will stop modulation (modulation defeat) until a new command is transmitted.

Figure 6-1. ATA5577 Functional Diagram



1) p = page selector

Figure 6-2. Example with Manchester Coding with Data Rate RF/16

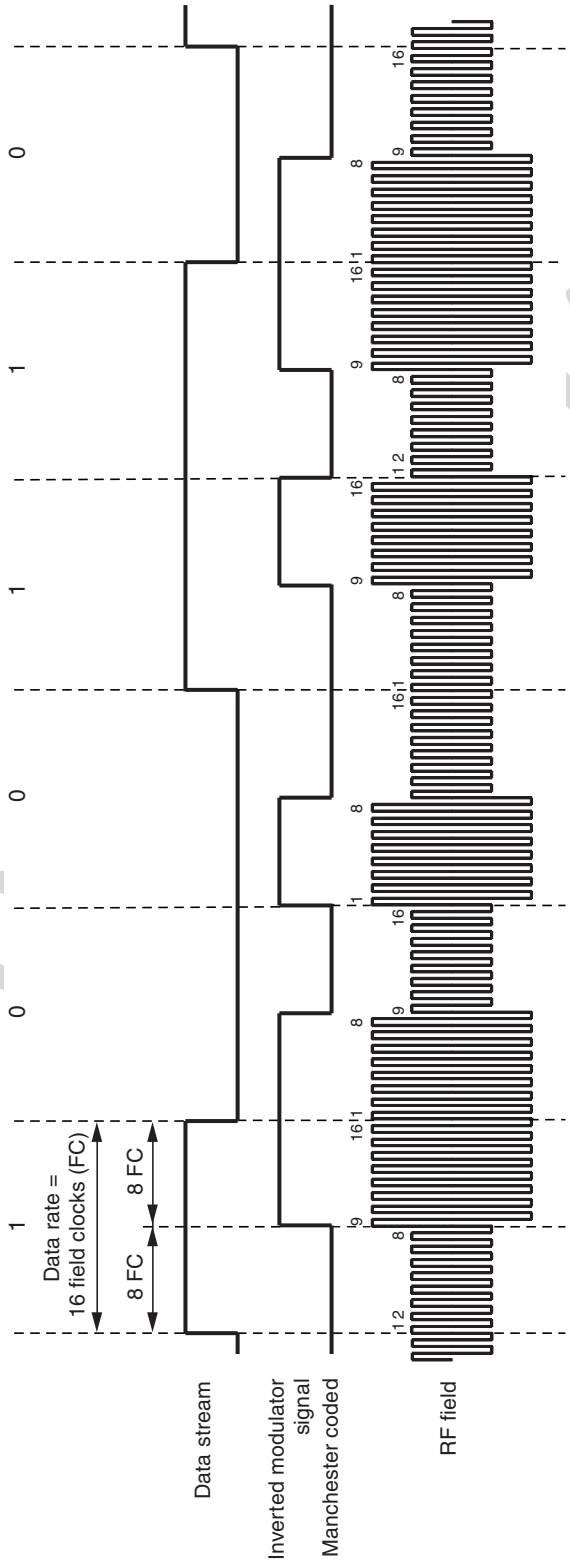


Figure 6-3. Example of Bi-phase Coding with Data Rate RF/16

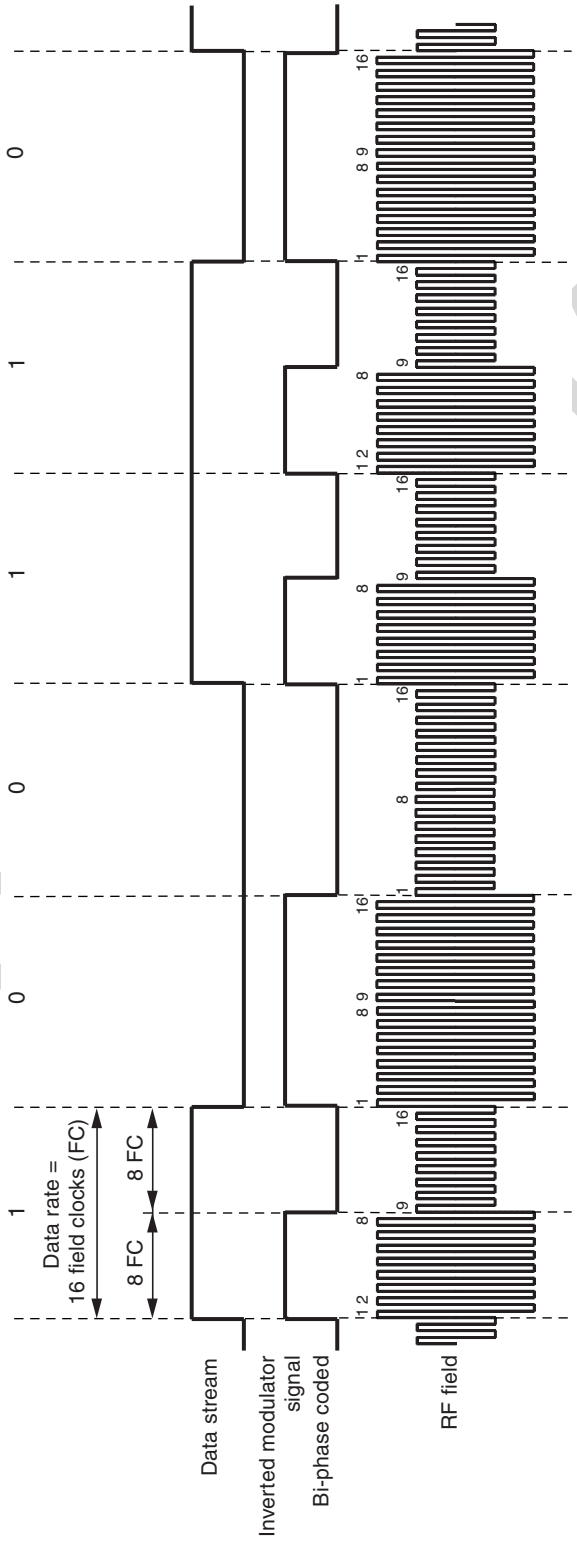


Figure 6-4. Example: FSK1a Coding with Data Rate RF/40, Sub-carrier f_0 = RF/8, f_1 = RF/5

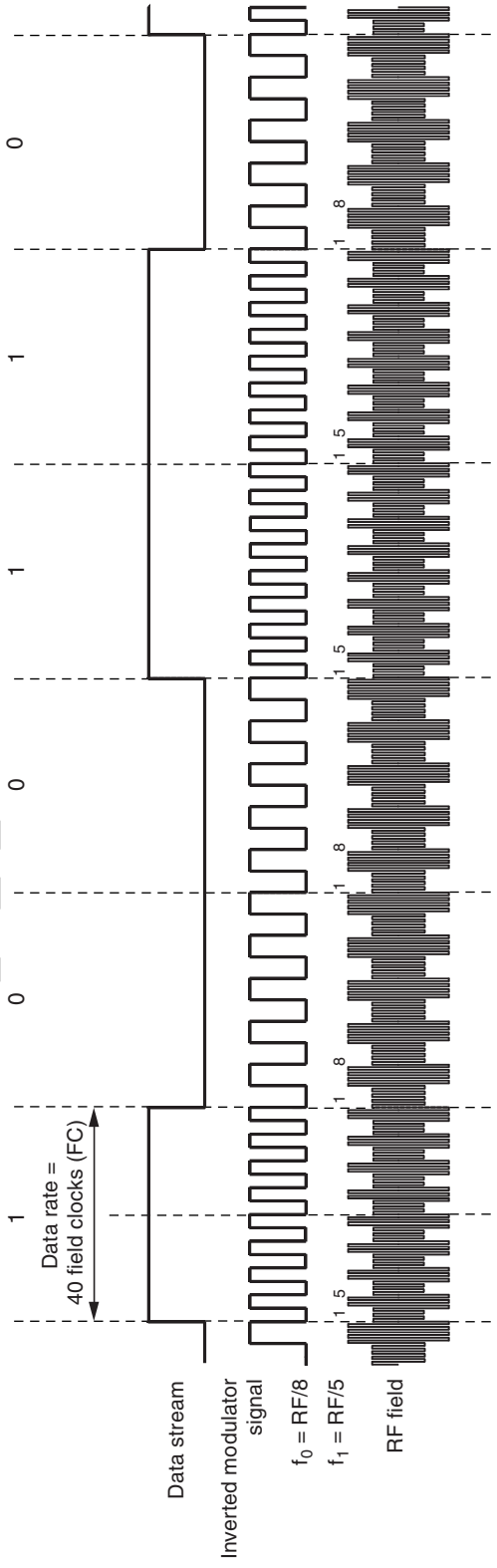


Figure 6-5. Example of PSK1 Coding with Data Rate RF/16

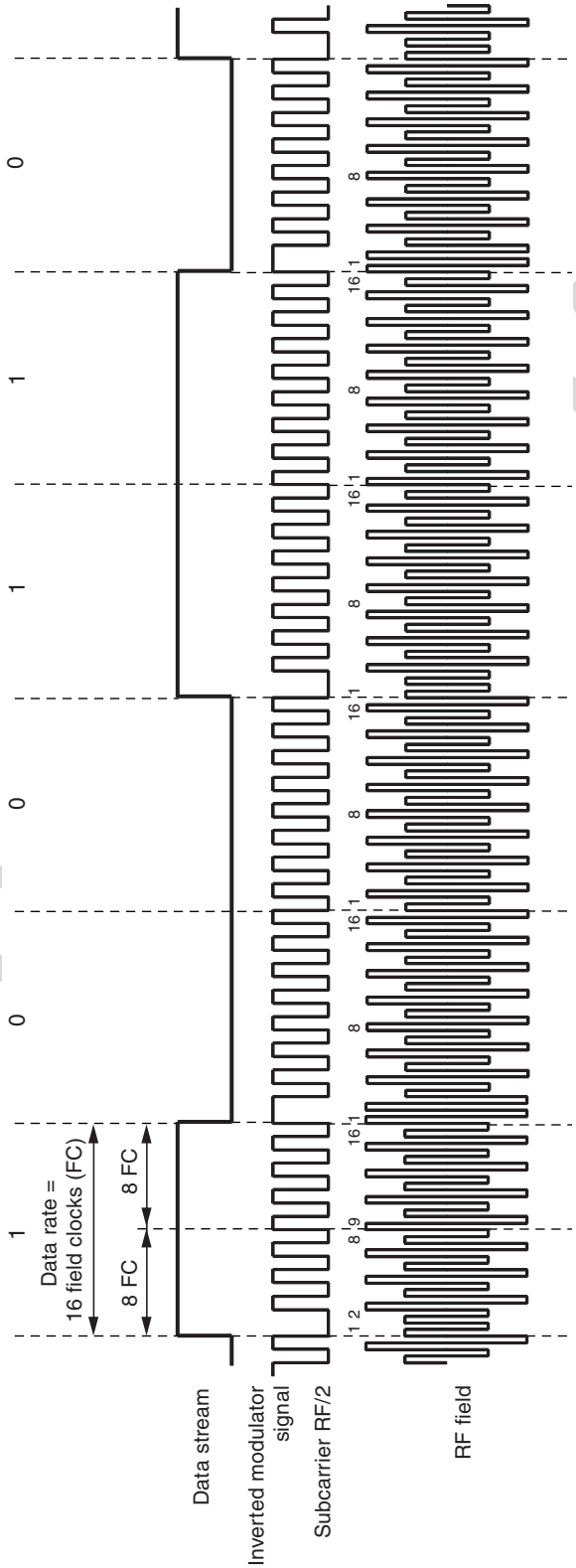


Figure 6-6. Example of PSK2 Coding with Data Rate RF/16

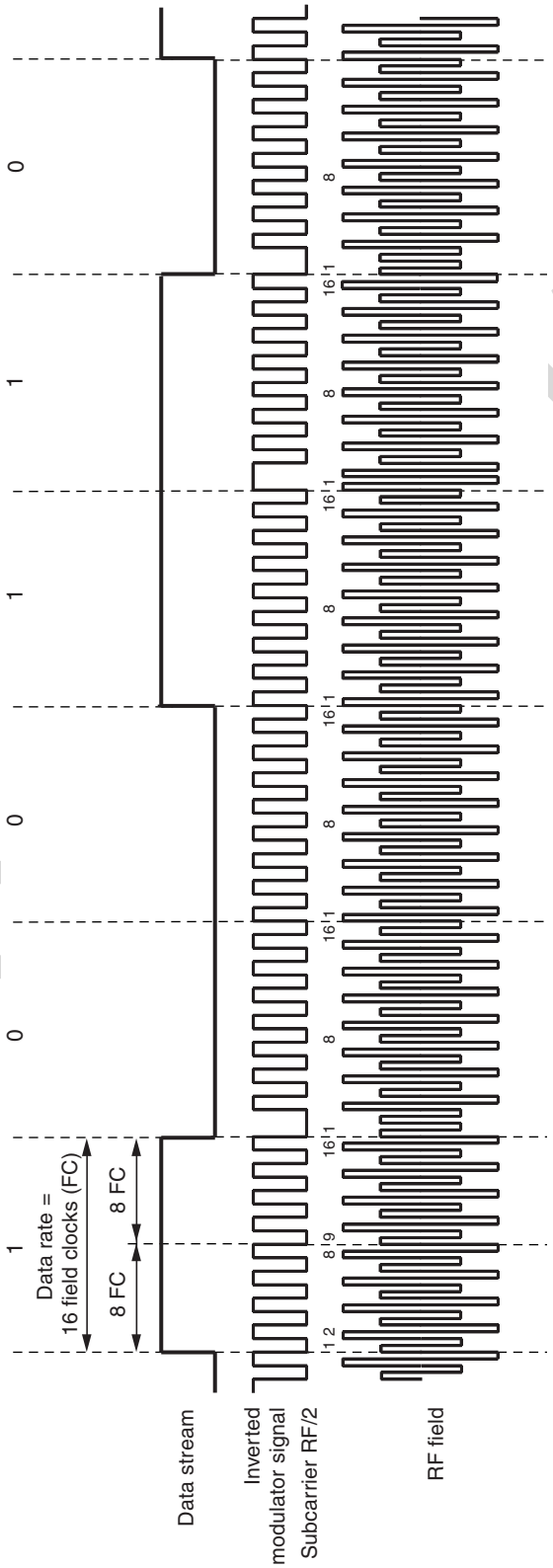
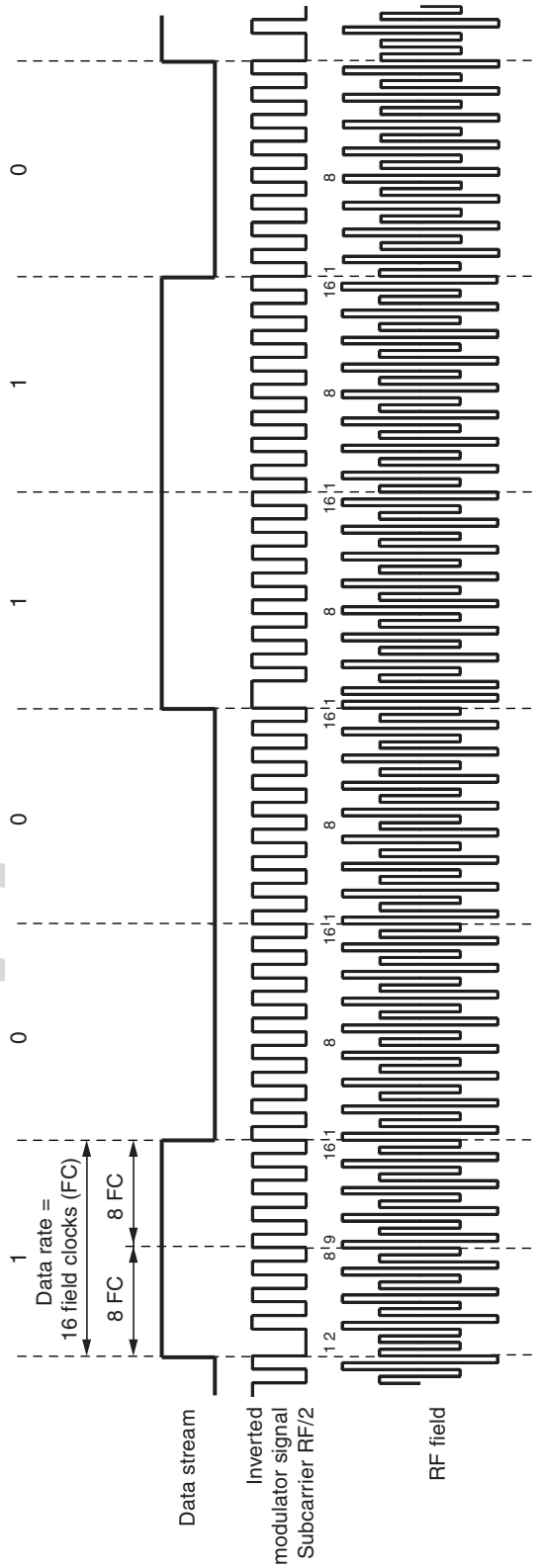


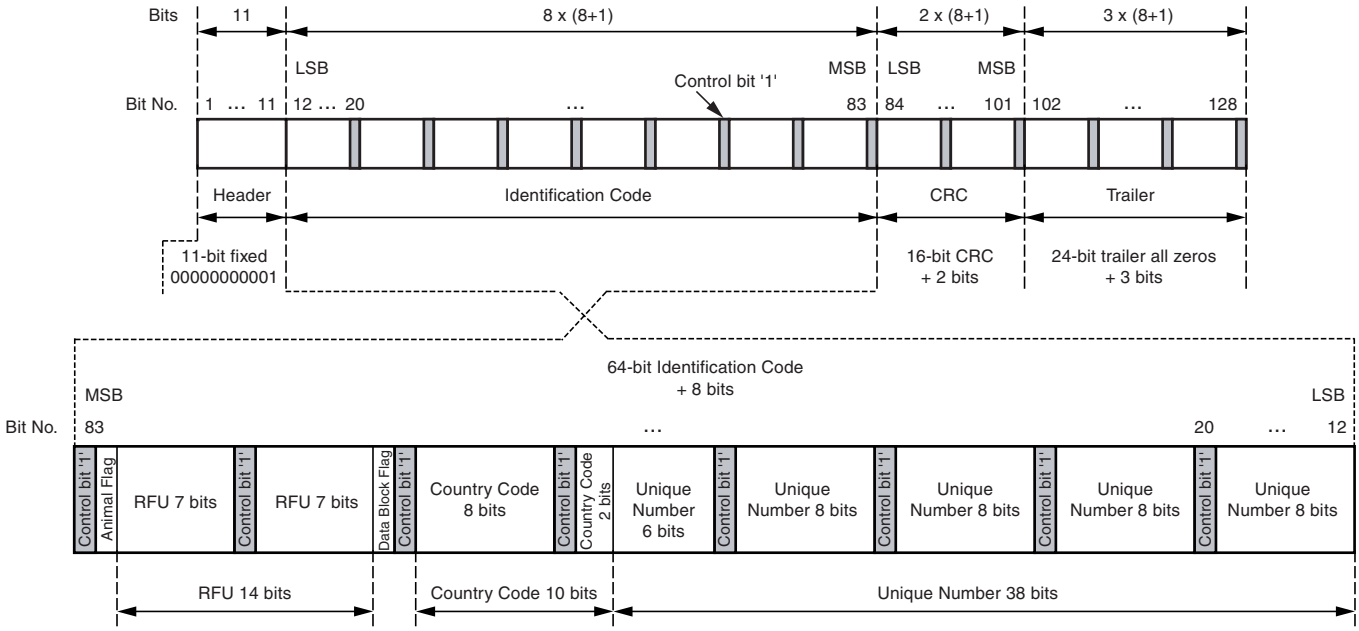
Figure 6-7. Example of PSK3 Coding with Data Rate RF/16



7. Animal ID

In ISO11784/11785, the code structure of a 128-bit FDX-B telegram is defined. Following is an example of how to program the ATA5577 for ISO 11785 FDX-B.

Figure 7-1. Structure of the ISO 11785 FDX-B Telegram



Notes:
1. Except for the header, every 8 bits are followed by one control bit (1), to prevent the header from recurring.
2. All data is transmitted LSB first.
3. Country codes are defined in ISO 3166
4. The bits reserved for future use (RFU) are all set to 0.
5. If the data block flag is not set, the trailer bits are all set to 0.
6. CRC is performed on the 64-bit identification code without the control bits. The generator polynomial is $P(x) = x^{16} + x^{12} + x^5 + 1$. Reverse CRC-CCITT (0x 8 408) is used. Data stream is LSB first.

Table 7-1. Example Data for Animal ID

Code	Dec. Value	Hex. Value	Comment
Animal flag	1	1	Use for animal ID
RFU	0	0	Reserved for future use
Data block flag	0	0	No data in trailer
Country code	999	3E7	Country code for demo tags
Unique number	78187493530	123456789A	Any demo number
CRC	36255	8D9F	CRC for the identification code

Programming of the ATA5577 for animal ID:

- Encoding of the data is differential bi-phase RF/32
- 128 bits have to be transmitted in regular-read mode (Maxblock = 4)

Table 7-2. Programming the ATA5577 with Example Data

Block	Address	Value	Comment
Option register	Block 3, page 1	0x 6DD0 0000[1]	Soft modulation, two pulses recommended
Configuration register	Block 0, page 0	0x 603F 8080	RF/32, differential bi-phase, Maxblock = 4
User data block 1	Block 1, page 0	0x 002B 31EB	Header, unique number
User data block 2	Block 2, page 0	0x 54B2 979F	Unique number (cont.), country code
User data block 3	Block 3, page 0	0x 8040 7F3B	Data block flag, RFU, animal flag, CRC
User data block 4	Block 4, page 0	0x 1804 0201	CRC (cont.), trailer bits

Note: 1. Depending on application, settings may vary

8. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil1/Coil2	I_{coil}	20	mA
Maximum AC current into Coil1/Coil2, f = 125 kHz	$I_{coil\ p}$	20	mA
Power dissipation (die) (free-air condition, time of application: 1s)	P_{tot}	100	mW
Electrostatic discharge maximum to ANSI/ESD-STM5.1-2001 standard (HBM)	V_{max}	3000	V
Operating ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	–40 to +150	°C

9. Electrical Characteristics

T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	T_{amb} = 25°C(1)	I_{DD}		1.5	3	µA	T
2.2		Read - full temperature range			2	5	µA	Q
2.3		Programming - full temperature range			25		µA	Q
3.1	Coil voltage (AC supply)	POR threshold (50-mV hysteresis)	$V_{coil\ pp}$		3.6		V	Q
3.2		Read mode and write command(2)		6		V_{clamp}	V	Q
3.3		Program EEPROM(2)		8		V_{clamp}	V	Q
4	Start-up time	$V_{coil\ pp}$ = 6V	$t_{startup}$		2.5		ms	Q
5.1	Clamp voltage (depends on settings in option register)	3-mA current into Coil1/Coil2	$V_{pp\ clamp\ lo}$		11		V	Q
5.2			$V_{pp\ clamp\ med}$		13		V	Q
5.3			$V_{pp\ clamp\ hi}$	14	17	21	V	T
5.4		20-mA current into Coil1/Coil2	$V_{pp\ clamp\ med}$	13	15	18	V	T
6.1	Modulation parameters (depends on settings in option register)	3-mA current into Coil1/Coil2 and modulation ON	$V_{pp\ mod\ lo}$	2	3	4	V	T
6.2			$V_{pp\ mod\ med}$		5		V	Q
6.3			$V_{pp\ mod\ hi}$		7		V	Q
6.4		20 mA current into Coil1/Coil2 and modulation ON	$V_{pp\ mod\ med}$	6	7.5	9	V	T
6.5	Thermal stability		$V_{mod\ lo}/T_{amb}$		–1		mV/°C	Q
7.1	Clock detection level (depends on settings in option register)	$V_{coil\ pp}$ = 8V	$V_{clkdet\ lo}$		250		mV	Q
7.2			$V_{clkdet\ med}$	400	550	730	mV	T
7.3			$V_{clkdet\ hi}$		800		mV	Q
7.4	Gap detection level (depends on settings in option register)	$V_{coil\ pp}$ = 8 V	$V_{gapdet\ lo}$		250		mV	Q
7.5			$V_{gapdet\ med}$	400	550	730	mV	T
7.6			$V_{gapdet\ hi}$		850		mV	Q
8	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
9	Endurance	Erase all/Write all(3)	n_{cycle}	100000			Cycles	Q

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement set-up: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10 mA.
3. Since EEPROM performance is influenced by assembly processes, Atmel can not confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. See Section 10. “Ordering Information” on page 39.

9. Electrical Characteristics (Continued)

T_{amb} = +25°C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
10.1	Data retention	Top = 55°C(3)	$t_{retention}$	10	20	50	Years	Q
10.2		Top = 150°C(3)	$t_{retention}$	96			hrs	T
10.3		Top = 250°C(3)	$t_{retention}$	24			hrs	Q
11.1	Resonance capacitor	Mask option(4) $V_{coil\ pp}$ = 1V	C_r	320	330	340	pF	T
11.2				242	250	258		
11.3					130			
11.4					75			
11.5					10			Q
12.1	Micromodule capacitor parameters	Capacitance tolerance T_{amb}	C_r	320	330	340	pF	T

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement set-up: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10 mA.
3. Since EEPROM performance is influenced by assembly processes, Atmel can not confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. See Section 10. “Ordering Information” on page 39.

10. Ordering Information

ATA5577M	t	ccc	-xxx	Package		Drawing
				DDB	6” sawn wafer on foil with ring, thickness 150 µm (approx. 6 mil)	Figure 11-3 on page 43
				DBB	6” sawn wafer on foil with ring and NiAu bumps 25 µm, thickness 150 µm (approx. 6 mil)	Figure 11-4 on page 44
				DDW	6” wafer, thickness 250 µm (approx. 10 mil) on request	
				DDT	Die in waffle pack, thickness 150 µm (approx. 6 mil)	Figure 11-8 on page 48
				PAE	NOA3 micromodule (lead-free, planned)	Figure 11-6 on page 46/ Figure 11-7 on page 47
				On-chip Capacity Value in pF		
				000	(planned)	
				075	(planned)	
				250		
				330		
				Type		
				1	Standard pads	

ATA5577M	t	ccc	-xxx	Package		Drawing
				DBB	6” sawn wafer on foil with ring and gold bumps 25 µm, thickness 150 µm (approx. 6 mil)	Figure 11-5 on page 45
				DDT	Die in waffle pack, thickness 150 µm (approx. 6 mil, on request)	Figure 11-9 on page 49
				DBN	Die on sticky tape with goldbumps 25 µm, thickness 280 µm (approx. 11 mil)	Sticky Tape: 3M 7419
				On-chip Capacity Value in pF		
				000	(on request)	
				075	(planned)	
				250		
				330		
				Type		
				2	Mega pads	

Note: A special version with *damping during initialization* could be generated on request (see also Section 5.5 “Initialization and Init-Delay” on page 10)

10.1 Available Order Codes

ATA5577M1250-DDT
ATA5577M1250-DDB
ATA5577M1330-DDT
ATA5577M1330-DDB
ATA5577M1330-DBB
ATA5577M1330-PAE
ATA5577M2250-DBB
ATA5577M2330-DBB
ATA5577M2330-DBN

New order codes will be created by customer request if order quantities are over 250k pieces.

10.2 Configuration on Delivery

Table 10-1. Configuration on Delivery

Block	Address	Value	Comment
AFE option set-up	Block 3, page 1	0x 0000 0000	All option take on the default state
Configregister	Block 0, page 0	0x 0008 8040	RF/32, Manchester, Maxblock =2
User data block 1	Block 1, page 0	0x 0000 0000	All “0”
User data block 2	Block 2, page 0	0x 0000 0000	All “0”

11. Package Information

Figure 11-1. Pad Layout, (Type 1, Standard Pads)

Dimensions in µm

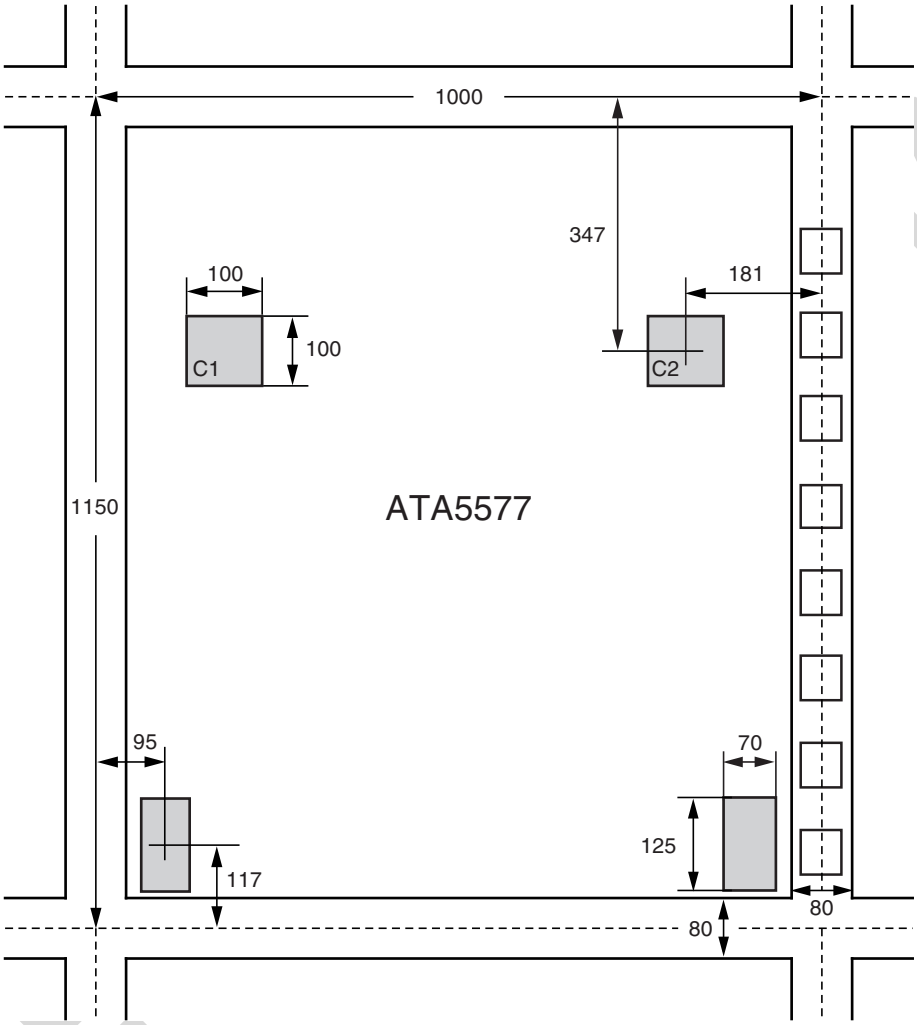


Figure 11-2. Pad Layout (Type 2, Mega Pads)

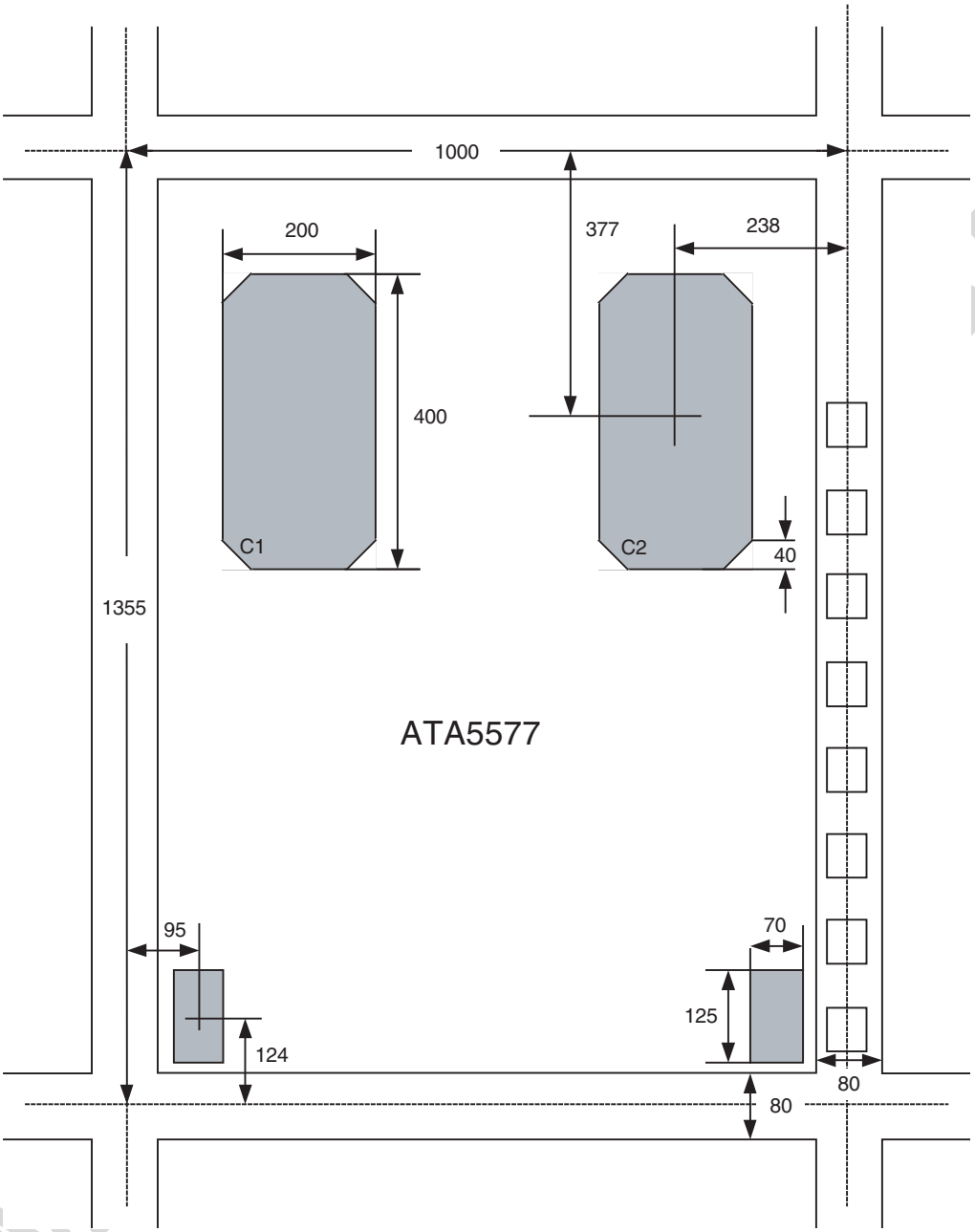


Figure 11-3. Sawn Wafer on Foil with Ring (Type 1, Standard Pads)

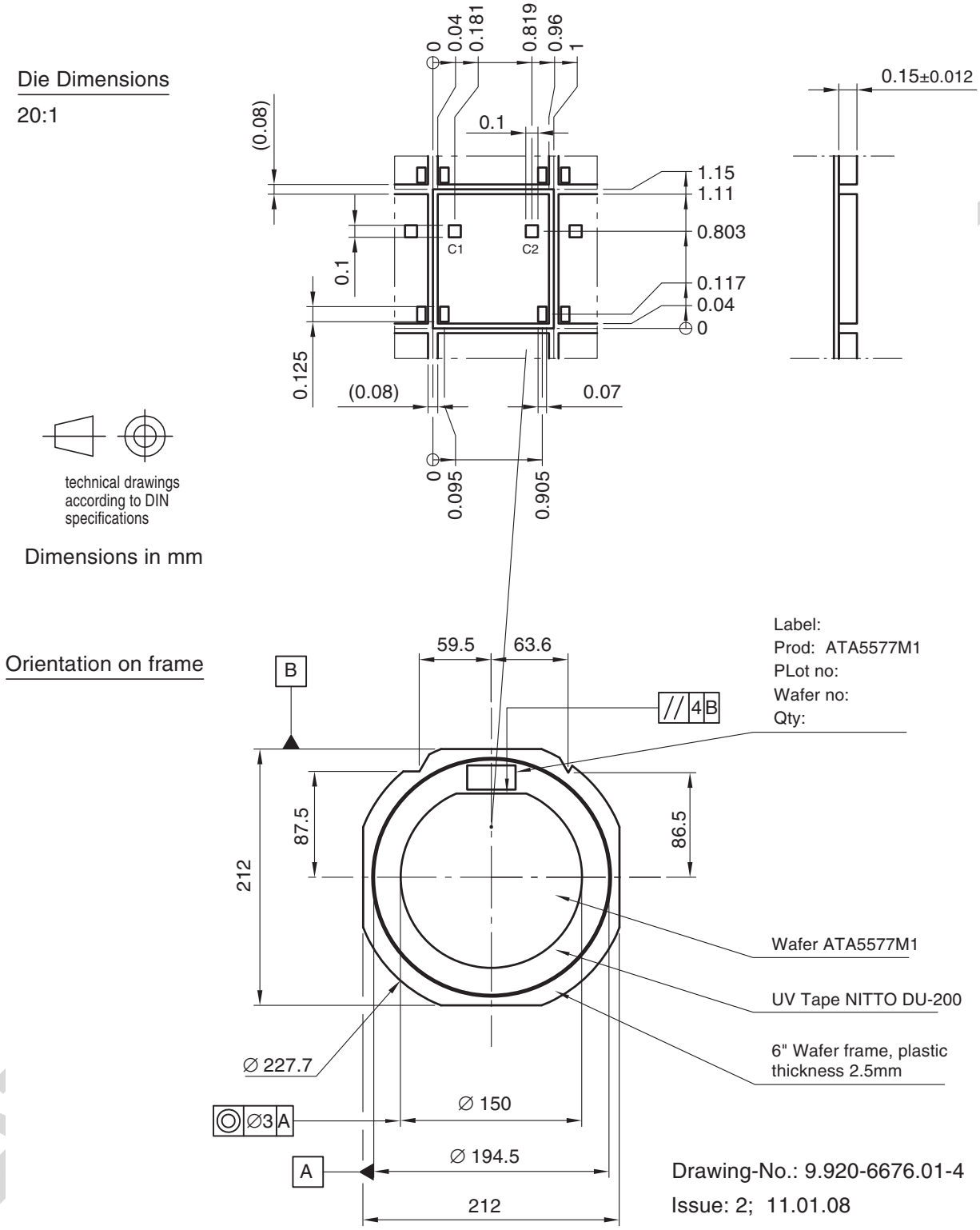


Figure 11-4. Sawn Wafer on Foil with Ring (Type 1, Standard Pads and NiAu Bumps)

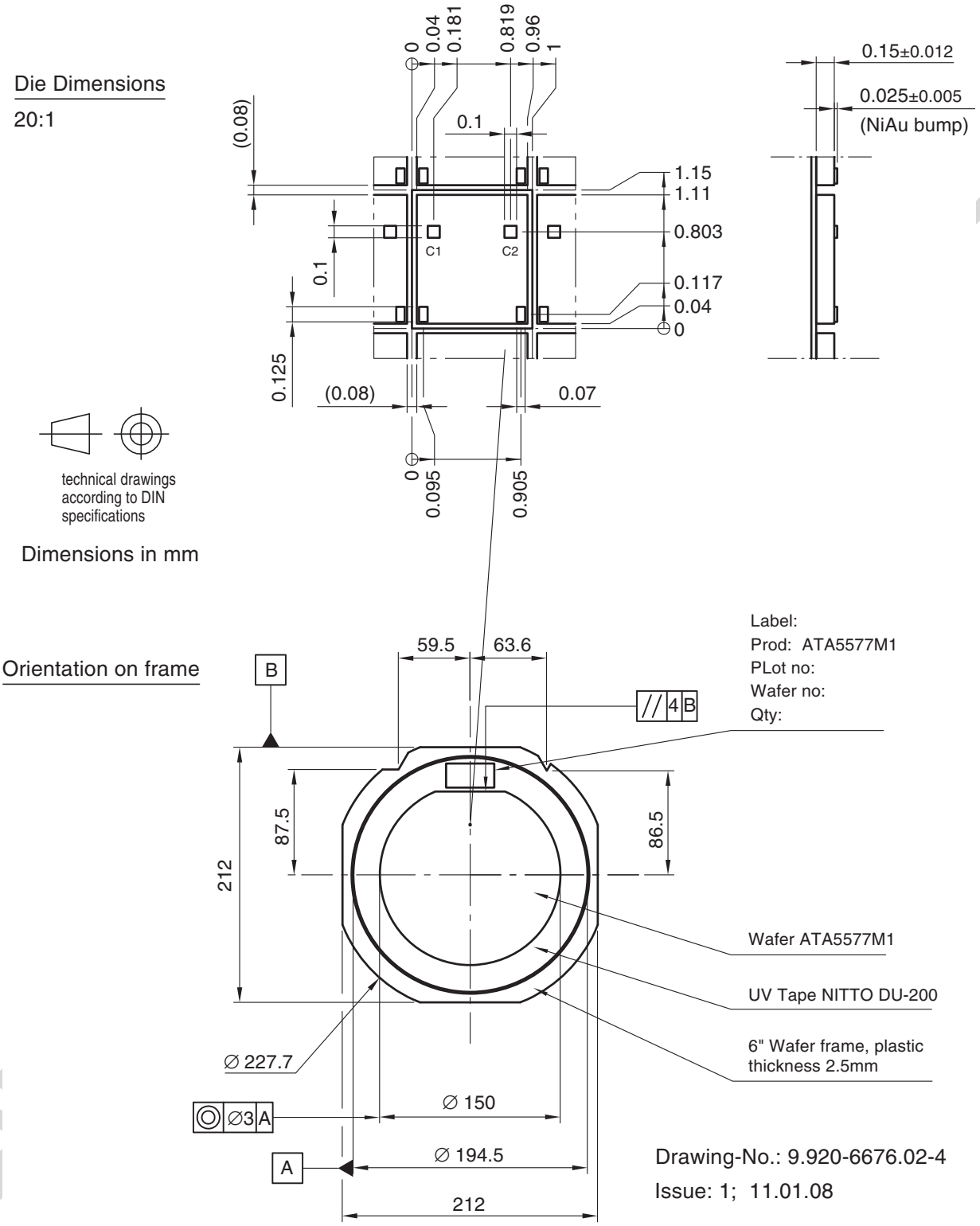


Figure 11-5. Sawn Wafer on Foil with Ring (Type 2, Mega Pads and Au Bumps)

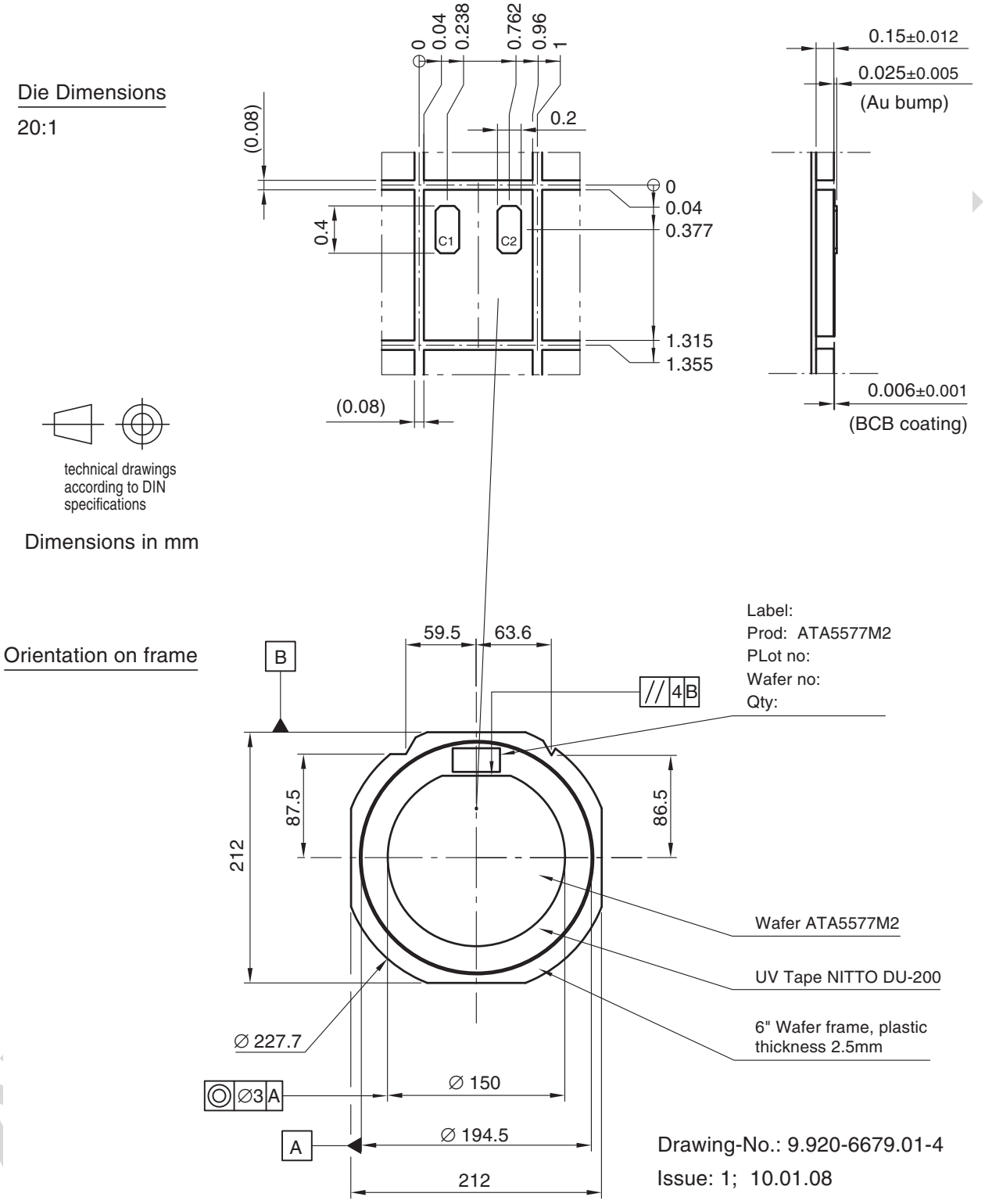
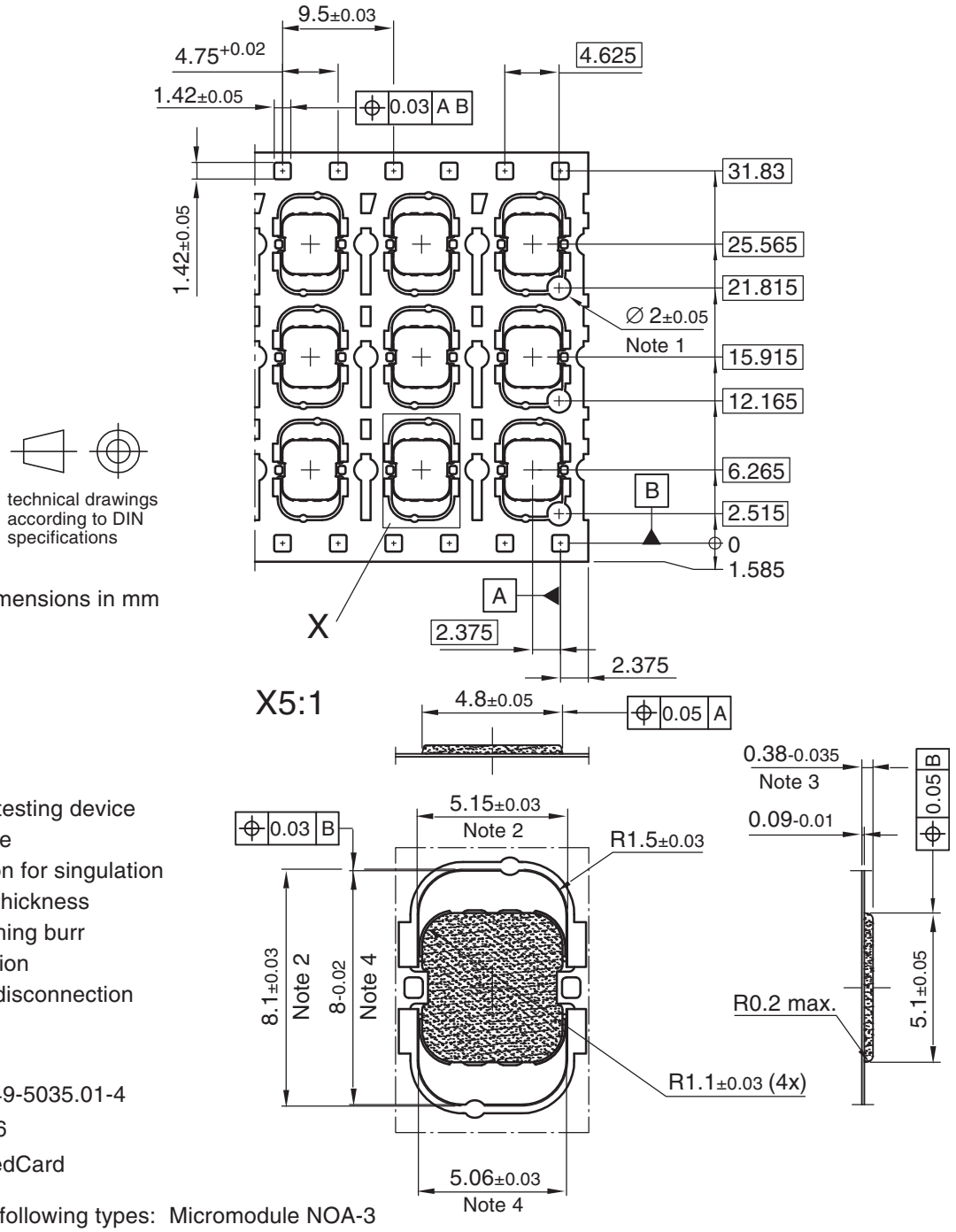


Figure 11-6. NOA3 Micromodule



Note:
1. Reject hole by testing device
2. Punching cutline
   recommendation for singulation
3. Total package thickness
   exclusive punching burr
4. Module dimension
   after electrical disconnection

Drawing-No.: 6.549-5035.01-4
Issue: 1; 28.04.06
Subcontractor: NedCard

Drawing refers to following types: Micromodule NOA-3

Figure 11-7. Shipping Reel for NOA3 Micromodule

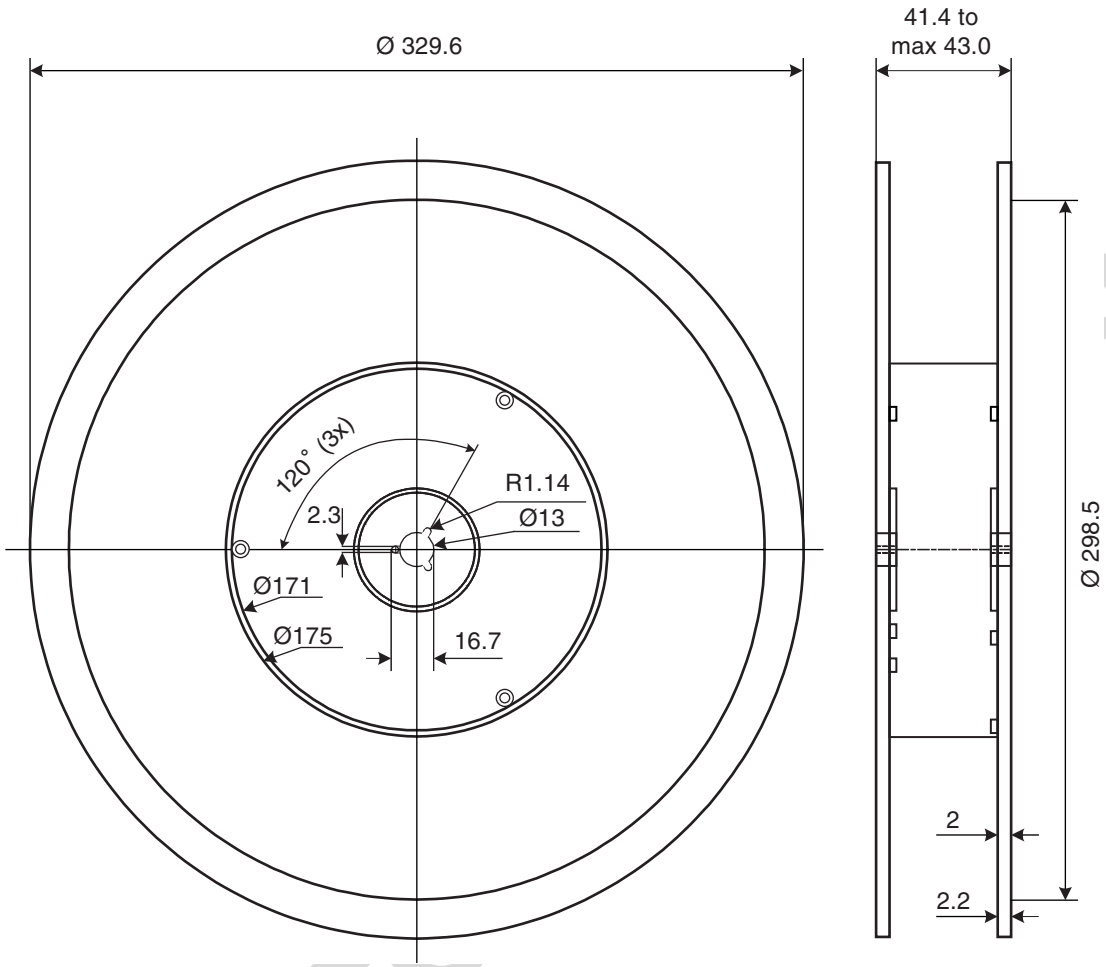
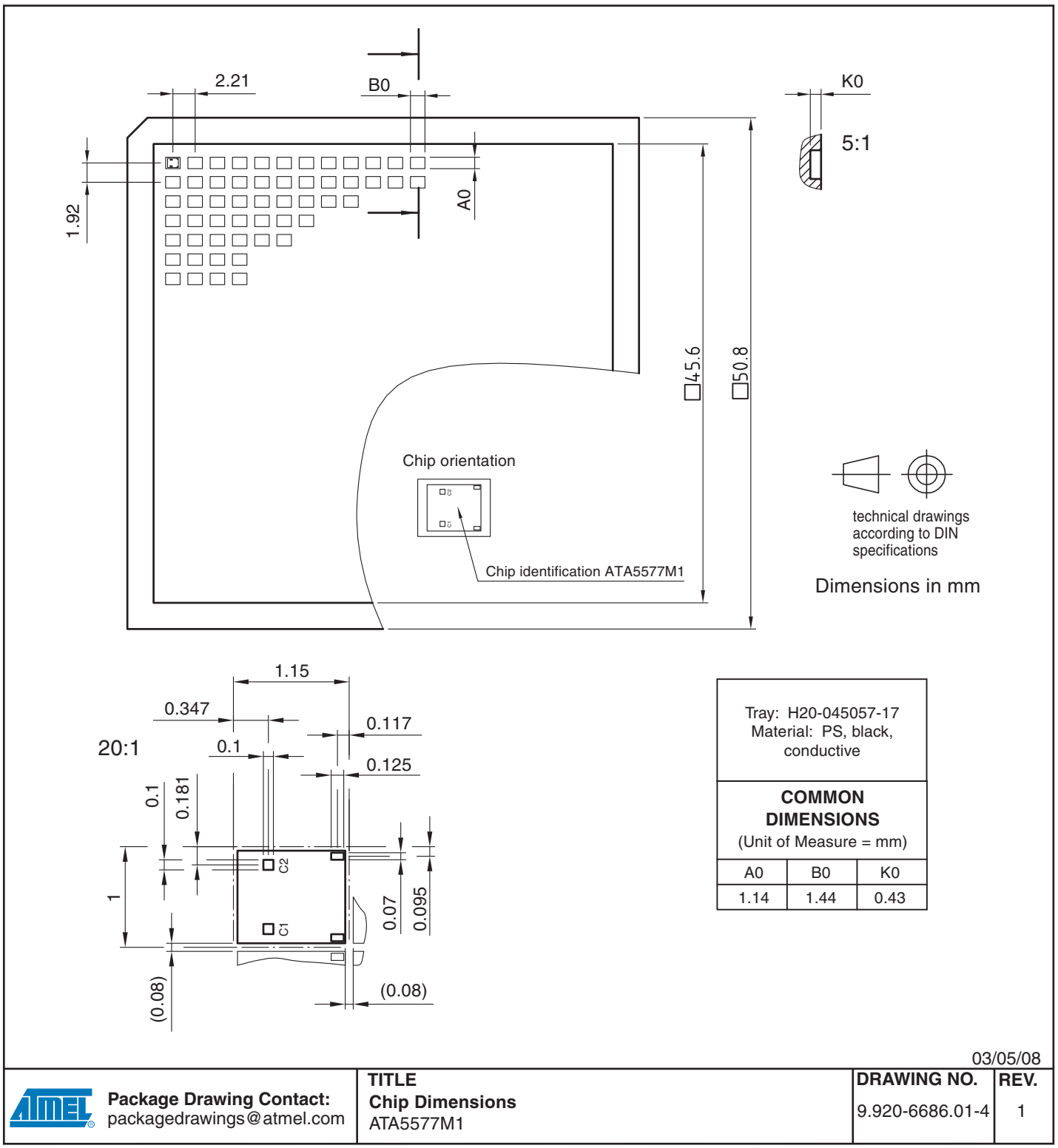


Figure 11-8. Die in Waffle Pack (Type 1)



Tray: H20-045057-17
Material: PS, black, conductive

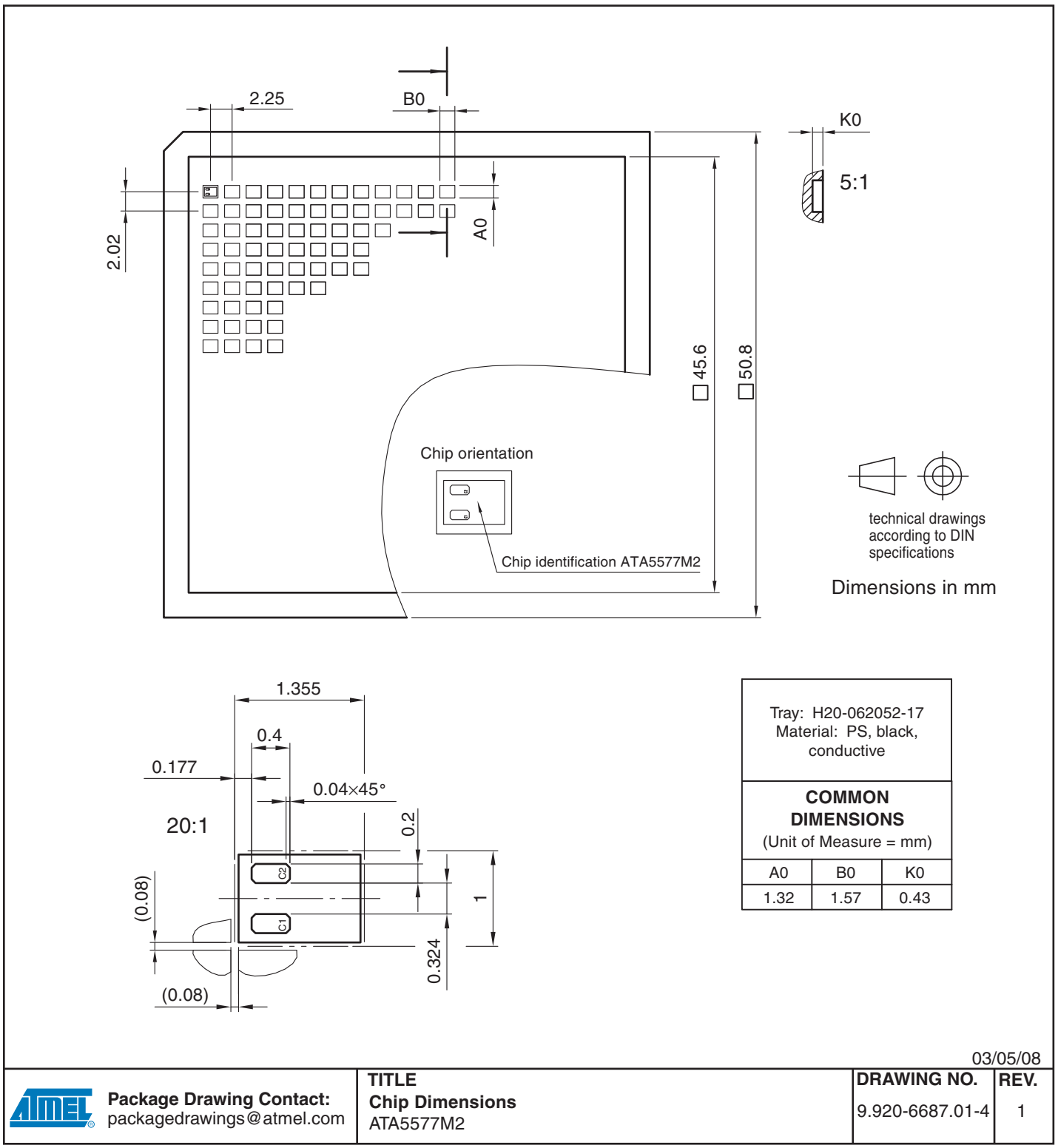
COMMON DIMENSIONS
(Unit of Measure = mm)

A0	B0	K0
1.14	1.44	0.43

03/05/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE Chip Dimensions ATA5577M1	DRAWING NO. 9.920-6686.01-4	REV. 1

Figure 11-9. Die in Waffle Pack (Type 2)



Tray: H20-062052-17
Material: PS, black, conductive

COMMON DIMENSIONS
(Unit of Measure = mm)

A0	B0	K0
1.32	1.57	0.43

03/05/08

Package Drawing Contact: packagedrawings@atmel.com	TITLE Chip Dimensions ATA5577M2	DRAWING NO. 9.920-6687.01-4	REV. 1

12. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4867CX-RFID-12/08	• Section 9 “Electrical Characteristics” on pages 37 to 38 changed • Section 10 “Ordering Information” on page 39 changed • Section 10.1 “Available Order Codes” on page 40 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
rfid@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature