Theory of Operation

80286 Microprocessor

The 80286 (U31) is an advanced, high-performance, 16-bit microprocessor with special capabilities for multi-tasking and multi-user systems. Two modes of operation are available in the 80286, the Real Address mode, and the Protected Virtual Address mode. In the Real Address mode, the 80286 is compatible with existing 8086 and 8088 software and allows addressing of one megabyte of memory space. The Tandy 1000 TL does **NOT** support the Protected Virtual Address mode.

80287 Numerical Math Coprocessor

The 80287 (U60) performs high-speed arithmetic and logarithmic functions and trigonometric operations that increase the performance of an 80286 system. Performance increases are obtained by the 80287's ability to perform math calculations faster than the 80286, and also by executing math instructions in parallel with the 80286.

Clock Generation (Night Blue)

All clocks required by the system are generated by the custom CPU Controller (U17). There are two independent clock circuits supplied by a Dual Oscillator Clock (Y2) from which all other clocks are derived.

The 16 MHz Clock is routed into the CPU Controller, which generates the output signals PRCLK, DMACLK, and SCLK. The Clock Switch circuitry required to toggle the 80286 Microprocessor between 8 MHz and 4 MHz mode, as well as the logic to prevent any short cycling during a clock switch cycle, are implemented in the CPU Controller IC. If the signal XD3 is asserted high during an I/O write to port 062 (hex), then the output signal PRCLK is 16 MHz, which operates the 80286 in 8 MHz mode. If the signal XD3 is asserted low during an I/O write to port 062 (hex), the output signal PRCLK is at 8 MHz, operating the 80286 in the 4 MHz mode. When Reset is generated, the signal RES- is asserted low and defaults the Tandy 1000 TL to the 8 MHz mode.

The CPU Controller Chip also controls wait states to insert the proper number of wait states required for a two clock mode of operation. When the PRCLK signal is 16 MHz (8 MHz Mode), then four wait states are inserted in all 8-bit Memory and I/O cycles. When the signal PRCLK is 8 MHz (4 MHz mode) then two wait states are inserted during all 8-bit Memory and I/O cycles. During all 16-bit memory cycles, only one wait state is inserted in both the 8 MHz and 4 MHz modes.

PRCLK0 is then routed through a damping resistor to produce the signal PRCLK for the 80286, PRCLKA for the 80287 math co-processor, and PRCLKB for the DRAM/DMA control logic.

DMACLK and SCLK are output signals for system use. The DMACLK output frequency is ¼ of the PRCLK signal, and the SCLK output frequency is ½ of the PRCLK signal. Both are synchronized by Reset to the PRCLK output signal. After a Reset, DMACLK and SCLK are held low until the 80286 asserts status S1 = 0. SCLK and DMACLK make the first transition on the falling edge of PRCLK, following with a Ts state that synchronizes them to PRCLK.

SCLK is buffered and filtered, then routed to the Expansion Bus for option board use. DMACLK is filtered and then routed to the DMA Controller.

Table 2 shows all the clocks generated from 16 MHz in both modes:

	8 MHz Mode	4 MHz Mode
PRCLK	16 MHz	8 MHz
SCLK	8 MHz	4 MHz
DMACLK	4 MHz	2 MHz

Table 2. Clocks Generated From 16MHz.

Command and Control Signal Generation

The command and control signals required for the Tandy 1000 TL operation are generated by the CPU Controller (U17). The command signals are decoded from the CPU status signals S0- through S1- and M/(IO-) during the Ts cycle. The decoded signals indicate the type of cycle that is to be executed (MEMR, MEMW, IOR-, IOW-, INTA-). The control signals (ALE, DT/R, DSDEN0-, DSDEN1-, MEMCYC) control the latching of addresses, determine the direction and enabling of the data bus buffers, and start a memory cycle. Table 3 indicates the decoding of the CPU status signals.

M/(IO-)	S1-	S0-	Type of Bus Cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	None: Idle
1	0	0	Halt or Shutdown
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	None: Idle

Table 3. CPU Status Signal Decoding.

A0 and BHE- are decoded to determine the data transfer width to and from the CPU. Table 4 shows the data transfer width depending on the state of A0 and BHE-.

BHE-	A0	Width of Data Transfer
0	0	Word Transfer
0	1	Byte Transfer D8 - D15
1	0	Byte Transfer D0 - D7
1	1	Not Used

Table 4. Data Transfer Width Decode.

Command Buffer

Some of the command signals generated by the CPU Controller require buffering to the system. This is accomplished by ½ of an ALS244 (U25) and ½ of another ALS 244 (U9). These ICs buffer the command signals to the system bus for the expansion bus slots, the peripheral devices, and also the Video Controller.

DRAM Control

The CPU address decode for the Dynamic Random Access Memory (DRAM) array is generated by the Custom DRAM/DMA Control IC (U22). These signals are latched by ALE internally to the DRAM/DMA Control IC and held for the complete cycle. The address decode signals are RAS0-, RAS1-, CASL-, and CASH-. Memory configurations supported by the Tandy 1000 TL are 640K bytes or 768K bytes (which includes 128K of video memory). Table 5 shows the different options available on the DRAM/DMA Control IC.

Memory Option	MC1	MC0	System Memory	Total System Memory*	Control	Bank	Address Range
1	0	1	512K	640K	RAS0	512K	000000-07FFFF
2	1	1	640K	768K	RAS0	512K	000000-07FFFF
					RAS1	128K	080000-09FFFF

* Note: Total system memory includes 128K of video memory.

Table 5. Memory Configurations.

Port FFEA hex, Bits 6 & 7, control the Memory Configuration Options. See the I/O Map later in this manual for details. MEMCYC triggers the control signals for the DRAM array. The MEMCYC signal (generated by the CPU Controller) indicates that a DRAM bus cycle is in progress. MEMCYC enables RAS0-, RAS1-, CASH-, and CASL-, depending on the address of the bus cycle. The selected RAS(x)- lines become active at the next falling edge of PRCLK.

After ½ PRCLK cycle at the rising edge of the clock, MUX is generated and switches the DRAM address (MA0-MA8) from Row Address to Column Address. After another PRCLK cycle at the next rising edge of the clock, CASL- and/or CASH- are asserted. Two CAS signals are generated internally to the DRAM/DMA Control IC to provide the ability to access word or byte cycles in the DRAM array. Table 6 shows the state of each control signal during each type of bus cycle.

Address Range	Bus Width	RAS0-	RAS1-	CASL-	CASH-
000000-07FFFFH	Even Byte	0	1	0	1
000000-07FFFFH	Odd Byte	0	1	1	0
000000-07FFFFH	Even Word	0	1	0	0
080000-09FFFFH	Even Byte	1	0	0	1
080000-09FFFFH	Odd Byte	1	0	1	0
080000-09FFFFH	Even Word	1	0	0	0

Table 6. Signal State Control Signals.

The signals WE0- and WE1- provide read and write control. Both are asserted at the same time and are controlled by MEMW- (memory write). If WE0- and WE1- are asserted high, it is a read cycle; if they are asserted low, it is a write cycle.

Refresh Control

The REFREQ pin of the KFIT custom IC (U13) generates an active high pulse every 15 usec. The rising edge of the REFREQ signal clocks the 8237 DMA controller. This input to the DMA controller is actually Data Transfer Request 0, (DREQ0), which requests the DMA to perform a DMA cycle. The DMA controller channel 0 has been programmed to perform a single transfer from memory to an I/O device, such as a floppy drive. This causes a memory read at a certain address to be performed. Each time the REFREQ signal is generated, the DMA controller increments the address and performs another memory read. This causes all memory rows to be read every 4ms to keep data in the DRAMs stable. Refer to the section on the DMA controller for more information on DMA cycles.

BIOS ROM Control

The DRAM/DMA IC (U22) provides the CPU address decode used for the ROM select. The signal generated is called ROMCS- (ROM Chip Select) and is used as part of the decode used by PLS173 IFL U44. The PLS173 IFL then generates the ROM Page Selects (RPCS-) and Chip Enable for the BIOS ROMs U54, U55, U56, and U57. This output is asserted whenever any of three addressed ranges is detected, CPHLDA is inactive, and ALE is asserted. The three address ranges are 0E0000-0FFFFFH, EE0000-EFFFFFH, and FE0000-FFFFFFH. The address lines SA1-SA15 are provided to the BIOS ROMs for lower address control. The data is buffered onto the MD0-MD15 data bus, controlled by the 82C205 IC.