DRAM/DMA CONTROL CHIP

TABLE OF CONTENTS

Tandy 1000TL DRAM/DMA Control IC consists of the following functional blocks:

- ROM/DRAM Decode Latch and Control signals
- Page Registers
- Memory Address Multiplexer

ROM/DRAM Decode Latch and Control signal

The ROM/DRAM Decode Latch block contains the circuitry to decode the CPU's Address bus A17 - A23 and to provide the necessary latched signals for controlling ROMS and DRAMS. CPU's Address A17 - A23 together with MC0 - MC2 determine which segment (bank) of memory is being selected based on one of six possible memory configurations. (see memory map figure 1.).The memory configurations ranging from 256 kilo bytes to 1.5 mega bytes.

Additional support for memory refresh is also provided in this block. During a Refresh Cycle, the assertion of REFRESH* will cause the circuitry to ignore the current address inputs and activate RAS0*, RAS1*, RAS2*, RAS3* and LMEGCS* outputs. Also MEMCYC and PRCLK signals are used for controlling the start of a memory access and timing for all RASx*s, MA0 - MA8 and CASx*s signals. (see Timing Diagram figure 2.).

ROMCS* is decoded from A17 - A23 and latched by ALE when HLDA is active. The ROM address ranges from 0E0000h to 0FFFFFh for the low address, EE0000h to EFFFFFh and FE0000h to FFFFFFh for high address. This output signal is asserted when any one of the three address ranges is detected and REFRESH* is inactive.

The two outputs LMEGCS* and MDBEN* are intended to be used as memory buffer enable signal. LMEGCS* is active whenever any memory access is made to an address below 010000h or when REFRESH* is active. MDBEN* is memory data bus buffer and becomes active whenever CASx*s or ROMCS* is active.

The ROM/DRAM Decode's internal latch is controlled by two input signals - HLDA and ALE. During a CPU Memory Cycle, ALE will enable the RAM Decode latch and allow the input from decoder to be transferred to the output pins. When ALE goes inactive, the decoder outputs is latched for the remainder of the cycle. Asserting HLDA will enable the decoder outputs to the output pins and force ROMCS* inactive. This block has one output signal that is unlatched. This output, AF16*, is intended to be used by external circuitry as an indication that a 16-bit memory transfer is taking place.

Page Register

At the time the 82C37A-5 - DMA Controller takes control of the address bus, the first operation comes in two bytes. The first byte is a lower address bus (SA0 through SA7) that is put directly on the S address bus by DMA controller. The second byte is a upper address (SA8 through SA15) that is on its data outputs, to be latched in the 74ALS373 internally by Address Strobe (AS) signal from DMA Controller.

Two 4 by 4 registers are used to perform Page Register function. During DMA Bus Cycle, the read function is controlled by the DMA Request Acknowledge signals - DACK2# and DACK3# in conjunction with HLDA# enables the Page Register to be output as the upper address (SA16 and A17 through A23). The write function is controlled by SA0 to SA3 in conjunction with PGREGWR# to latch data bits - XD0 to XD7 into Page Register.

Address Multiplexer

The Memory Address Multiplexer is used to provide the Row Address or Column Address and refresh counter that is required by Dynamic Rams. Additionally, it provides the drive and buffering capability for memory address bus MA0 to MA8. MA7 is generated from SA0 or SA8 which is multiplexed by REFRESH# signal. The addresses for the memory are multiplexed as shown below.

Equation For Multiplexed Memory Addresses

	Row Address (First)	Column Address (Second)
MA0 -----	SA1	SA9
MA1 -----	SA2	SA10
MA2 -----	SA3	SA11
MA3 -----	SA4	SA12
MA4 -----	SA5	SA13
MA5 -----	SA6	SA14
MA6 -----	SA7	SA15
MA7 -----	SA8/SA0	SA16
MA8 -----	SA17	SA18

2. MEMORY CONFIGURATION

OPTION	MC2	MC1	MC0	BANK0	BANK1	BANK2	CONTROL	ADDRESS RANGE
1	0	0	0		128K		Ras1	(000000-01FFFF)
						128K	Ras2	(020000-03FFFF)
2	0	0	1	512K			Ras0	(000000-07FFFF)
3	0	1	1	512K			Ras0	(000000-07FFFF)
					128K		Ras1	(080000-09FFFF)
4	0	1	0	512K			Ras0	(000000-07FFFF)
					128K		Ras1	(08FFFF-09FFFF)
						128K	Ras2	(100000-17FFFF)
5	1	1	1	512K			Ras0	(000000-07FFFF)
					128K		Ras1	(080000-09FFFF)
						512K	Ras2	(100000-17FFFF)
6	1	1	0	512K			Ras0	(000000-07FFFF)
					128K		Ras1	(080000-09FFFF)
						512K	Ras2	(100000-17FFFF)
						512K	Ras3	(180000-1FFFFF)
7	1	0	1	NOT DEFINED				
8	1	0	0	NOT DEFINED				

FIGURE 1. MEMORY CONFIGURATION.

3. DMA Control Logic Equations

```
/Bras0 = /la23 & /la22 & /la21 & /la20 & /la19 & /mc2 & mc0
         +/la23 & /la22 & /la21 & /la20 & /la19 & mc1
         +refresh;

/Bras1 = /la23 & /la22 & /la21 & /la20 & /la19 & /la18 & /la17 & /mc0
          & /mc1 & /mc2
         +/la23 & /la22 & /la21 & /la20 & la19 & /la18 & /la17 & mc1
         +refresh;

/Bras2 = /la23 & /la22 & /la21 & /la20 & /la19 & /la18 & la17 & /mc0
          &  /mc1 & /mc2
         +/la23 & /la22 & /la21 & la20 & /la19 & /la18 & /la17 & /mc0 & mc1
          & /mc2
         +/la23 & /la22 & /la21 & la20 & /la19 & mc1 & mc2
         +refresh;

/Bras3 = /la23 & /la22 & /la21 & la20 & la19 & /mc0 & mc1 & mc2
         +refresh;

/Bcas  = /la23 & /la22 & /la21 & /la20 & /la19 & /la18 & /mc2 & /mc1
          & /mc0 & /refresh
         +/la23 & /la22 & /la21 & /la20 & /la19 & /mc2 & mc0 & /refresh
         +/la23 & /la22 & /la21 & /la20 & /la19 & mc1 & /refresh
         +/la23 & /la22 & /la21 & /la20 & la19 & /la18 & /la17 & mc1
          & /refresh
         +/la23 & /la22 & /la21 & la20 & /la19 & /la18 & /la17 & /mc2 & mc1
          & /mc0 & /refresh
         +/la23 & /la22 & /la21 & la20 & /la19 & mc2  & mc1  & /refresh
         +/la23 & /la22 & /la21 & la20 & mc2 & mc1 & /mc0 & /refresh;

/Blmeg  = /la23 & /la22 & /la21 & /la20+refresh;

/Bromcs =/la23 & /la22 & /la21 & /la20 & la19 & la18 & la17 & /refresh
         +la23 & la22 & la21 & la20 & la19 & la18 & la17 & /refresh
         +la23 & la22 & la21 & /la20 & la19 & la18 & la17 & /refresh;
```

4. Block Diagram

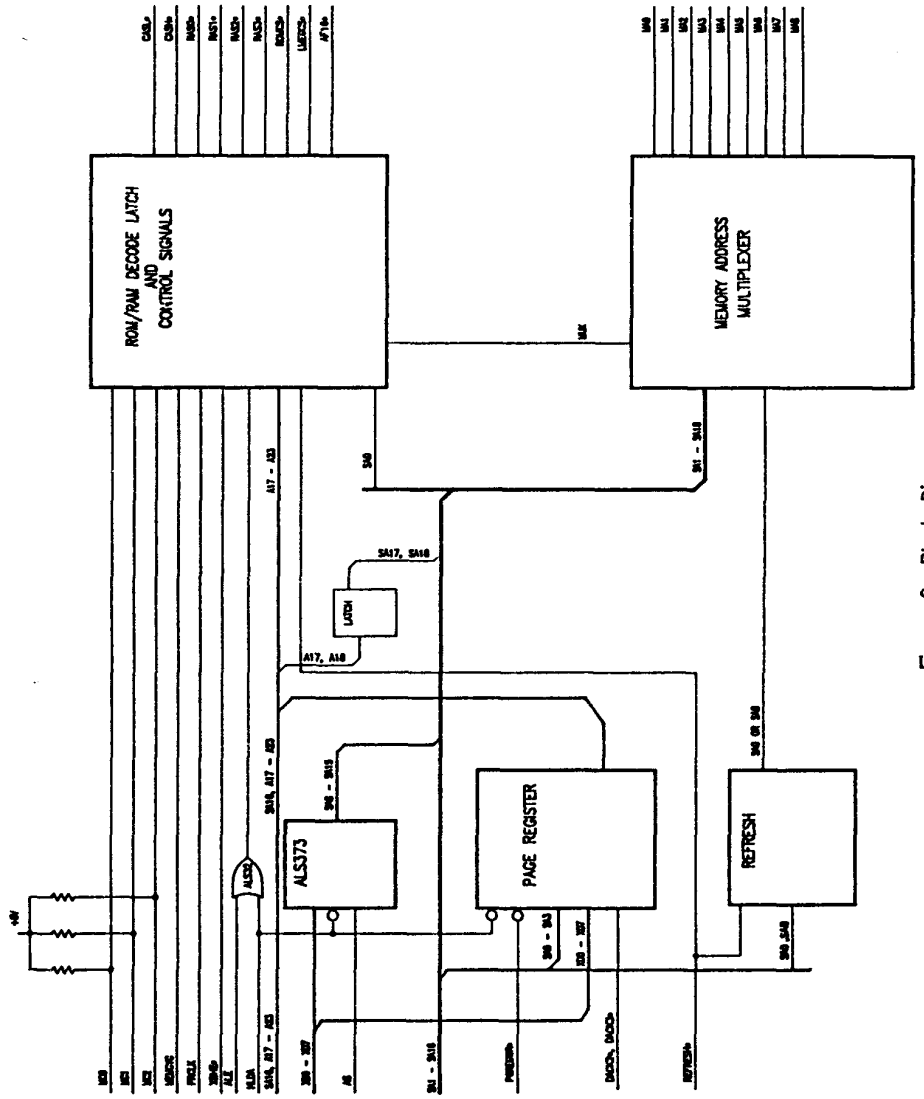


Figure 2. Block Diagram

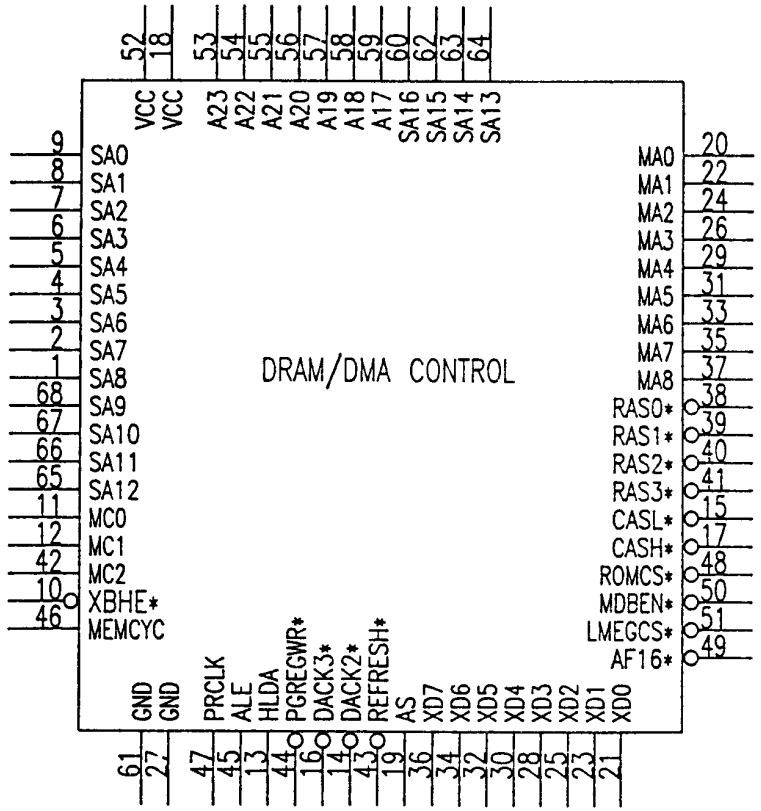


FIGURE 3. PIN CONFIGURATION

6. INPUT/OUTPUT PINS FUNCTION AND DESCRIPTION

PIN#	PIN NAME	TYPE	DESCRIPTION
9	SA0	INPUT	CPU ADDRESS LINE
8	SA1	INPUT	CPU ADDRESS LINE
7	SA2	INPUT	CPU ADDRESS LINE
6	SA3	INPUT	CPU ADDRESS LINE
5	SA4	INPUT	CPU ADDRESS LINE
4	SA5	INPUT	CPU ADDRESS LINE
3	SA6	INPUT	CPU ADDRESS LINE
2	SA7	INPUT	CPU ADDRESS LINE
1	SA8	INPUT/OUTPUT	CPU ADDRESS LINE
68	SA9	INPUT/OUTPUT	CPU ADDRESS LINE
67	SA10	INPUT/OUTPUT	CPU ADDRESS LINE
66	SA11	INPUT/OUTPUT	CPU ADDRESS LINE
65	SA12	INPUT/OUTPUT	CPU ADDRESS LINE
64	SA13	INPUT/OUTPUT	CPU ADDRESS LINE
63	SA14	INPUT/OUTPUT	CPU ADDRESS LINE
62	SA15	INPUT/OUTPUT	CPU ADDRESS LINE
60	SA16	INPUT/OUTPUT	CPU ADDRESS LINE
59	A17	INPUT/OUTPUT	CPU ADDRESS LINE
58	A18	INPUT/OUTPUT	CPU ADDRESS LINE
57	A19	INPUT/OUTPUT	CPU ADDRESS LINE
56	A20	INPUT/OUTPUT	CPU ADDRESS LINE
55	A21	INPUT/OUTPUT	CPU ADDRESS LINE
54	A22	INPUT/OUTPUT	CPU ADDRESS LINE
53	A23	INPUT/OUTPUT	CPU ADDRESS LINE
45	ALE	INPUT	ADDRESS LATCH ENABLE Active HIGH - to latch generated RAS/CAS/LMEG.
43	REFRESH*	INPUT	REFRESH - Active LOW to initiate a refresh cycle for dynamic RAMs.
14	DACK2*	INPUT	8237 Channel 2 DMA ACKNOWLEDGE
16	DACK3*	INPUT	8237 Channel 3 DMA ACKNOWLEDGE
13	HLDA	INPUT	HOLD ACKNOWLEDGE Active HIGH - it indicates that the DMA has the system bus.
44	PGREGWR*	INPUT	PAGE REGISTER WRITE- active LOW to perform I/O WRITE cycle to the DMA Page Register.
46	MEMCYC	INPUT	MEMORY CYCLE - Active HIGH to initiate RAS/CAS/MA0-MA8 outputs.
19	AS	INPUT	ADDRESS STROBE - Active HIGH it latches the addres lines SA8-SA15 D0-D7 into external latch for DMA cycle

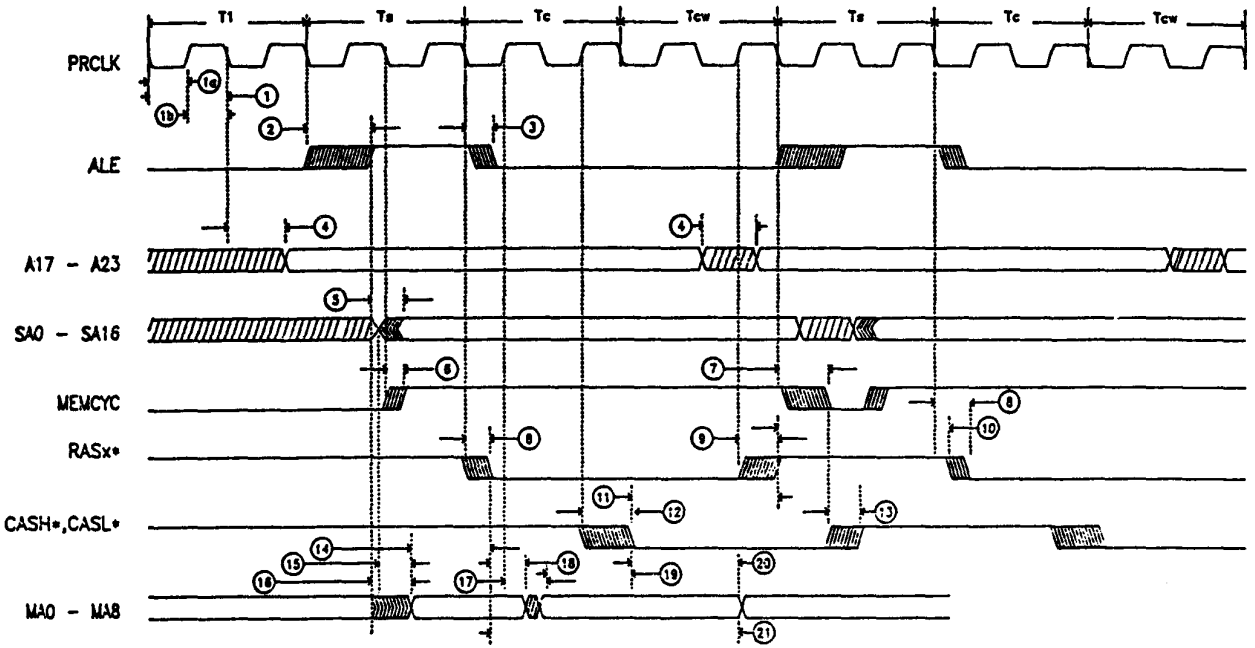
PIN#	PIN NAME	TYPE	DESCRIPTION
10	XBHE*	INPUT	BYTE HIGH ENABLE To enable the high memory data bytes D8-D15
47	PRCLK	INPUT	16MHZ CLOCK.
11	MC0	INPUT	MEMORY CONFIGURATION SELECT LSB.
12	MC1	INPUT	MEMORY CONFIGURATION SELECT.
42	MC2	INPUT	MEMORY CONFIG. SELECT MSB.
20	MA0	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
22	MA1	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
24	MA2	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
26	MA3	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
29	MA4	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
31	MA5	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
33	MA6	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
35	MA7	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
37	MA8	OUTPUT	MULTIPLEXED MEMORY ADDRESS - addressing required for DRAM memory.
17	CASH*	OUTPUT	COLUMN ADDRESS STROBE HIGH - Active LOW, it's used to select the high data byte MD8-MD15 for a DRAM access cycle.

PIN#	PIN NAME	TYPE	DESCRIPTION
15	CASL*	OUTPUT	COLUMN ADDRESS STROBE LOW - Active LOW, it's used to select low data byte MD0-MD7 for a DRAM access cycle.
38	RAS0*	OUTPUT	ROW ADDRESS STROBE 0 - Active LOW, it's used for selecting DRAM Bank0.
39	RAS1*	OUTPUT	ROW ADDRESS STROBE 1 - Active LOW, it's used for selecting DRAM Bank1.
40	RAS2*	OUTPUT	ROW ADDRESS STROBE 2 - Active LOW, it's used for selecting DRAM Bank2.
41	RAS3*	OUTPUT	ROW ADDRESS STROBE 3 - Active LOW, it's used for selecting DRAM Bank2.
51	LMEGCS*	OUTPUT	LOWER MEGABYTE CHIP SELECT - Active LOW,it indicates that bellow 1 megabyte
50	MDBEN*	OUTPUT	MEMORY DATA BUS ENABLE Active LOW it is used to enable the data bus buffer.
49	AF16*	OUTPUT	AF16 Active LOW - it signals the control logic (CPU CNTL) that the memory cycle is a 16 bit 1 wait state cycle.
48	ROMCS*	OUTPUT	ROM CHIP SELECT Active LOW
21	XD0	INPUT	DATA BUS 0 for the peripheral bus.
23	XD1	INPUT	DATA BUS 1 for the peripheral bus.
25	XD2	INPUT	DATA BUS 2 for the peripheral bus.
28	XD3	INPUT	DATA BUS 3 for the peripheral bus.
30	XD4	INPUT	DATA BUS 4 for the peripheral bus.
32	XD5	INPUT	DATA BUS 5 for the peripheral bus.
34	XD6	INPUT	DATA BUS 6 for the peripheral bus.
36	XD7	INPUT	DATA BUS 7 for the peripheral bus.
18,52	VCC		+5V POWER SUPPLY
27,61	GND		GROUND

7. TIMING SPECIFICATIONS

SYM	PARAMETER	MIN	MAX	UNITS	REMARKS
T1	PRCLK Period	62.5	250	nsec	
T1a	PRCLK Low Time	25	125	nsec	
T1b	PRCLK High time	25	125	nsec	
T2	ALE Active Delay	6	53	nsec	
T3	ALE Inactive Delay	5	25	nsec	
T4	Address Delay	1	60	nsec	
T5	Latched Address From ALE Active	-	23	nsec	
T6	MEMCYC Active Delay From ↓PRCLK	5	25	nsec	
T7	MEMCYC Inactive Delay From ↓PRCLK	5	35	nsec	
T8	RASx* Active Delay From ↓PRCLK	5	45	nsec	at 100pf
T9	RASx* Inactive Delay From ↑PRCLK	5	30	nsec	
T10	RASx* Precharge Time	110		nsec	
T11	RASx* Hold Time	30		nsec	
T12	CASx* Active Delay Time From ↑PRCLK	5	40	nsec	at 165pf
T13	CASx* Inactive Delay Time From ↓ MEMCYC	5	30	nsec	
T14	Row Address Setup Time	5		nsec	
T15	Memory Address Delay Time From SA1 to SA16	0	50	nsec	at 200pf
T16	Memory Address Delay From ALE	8	50	nsec	
T17	Memory Address Stable Delay From ↑ PRCLK		50	nsec	at 200pf
T18	Row Address Hold Time	20		nsec	
T19	Column Address Setup Time	5		nsec	
T20	Column Address Hold Time	30		nsec	
T21	Column Address Hold Time Referenced To RASx*	120		nsec	
T22	ALE ↑ to MDBEN ↑↓ A/I		50	nsec	
T23	ALE ↑ to LMEGCS* ↓↑ A/I		50	nsec	
T24	ALE ↑ to ROMCS* ↓↑ A/I		50	nsec	CPUHLDA HIGH

SYM	PARAMETER	MIN	MAX	UNITS	REMARKS
T25	A17-A23 ↑↓ to AF16* ↓↑ A/I		50	nsec	
T26	CPUHLDA↑↓ to MDBEN ↑I		50	nsec	
T27	CPUHLDA↑↓ to ROMCS* ↓↑ A/I		50	nsec	
T28	CPUHLDA↑↓ to SA8-SA15 ↓↑		50	nsec	
T29	CPUHLDA↑↓ to SA16,A17-A23 ↑↓		50	nsec	
T30	DACK2*, DACK3* ↑↓ to SA16, ↑↓ A17-A23		50	nsec	
T31, T32	DACKx* to AF16*, MDBEN*				
T33	LMEGCS*		80	nsec	
T34	REFRESH* ↑↓ to MA7↑↓A/I		50	nsec	at 200pf
T35	XD0-XD7 Setup to AS ↓	100		nsec	
T36	XD0-XD7 Setup to PGREGWR*	100		nsec	
T37	SA0-SA3 Setup to PGREGWR*	100		nsec	
T38	REFRESH* ↓↑ to AF16*		50	nsec	
T39	REFRESH* ↓↑ to MDBEN*		50	nsec	


T1
Ts
Tc
Tcw
Ts
Tc
Tcw
PRCLK
ALE
A17 - A23
SA0 - SA16
MEMCYC
RASx*
CASH*,CASL*
MA0 - MA8
1a
1b
1
2
3
4
4
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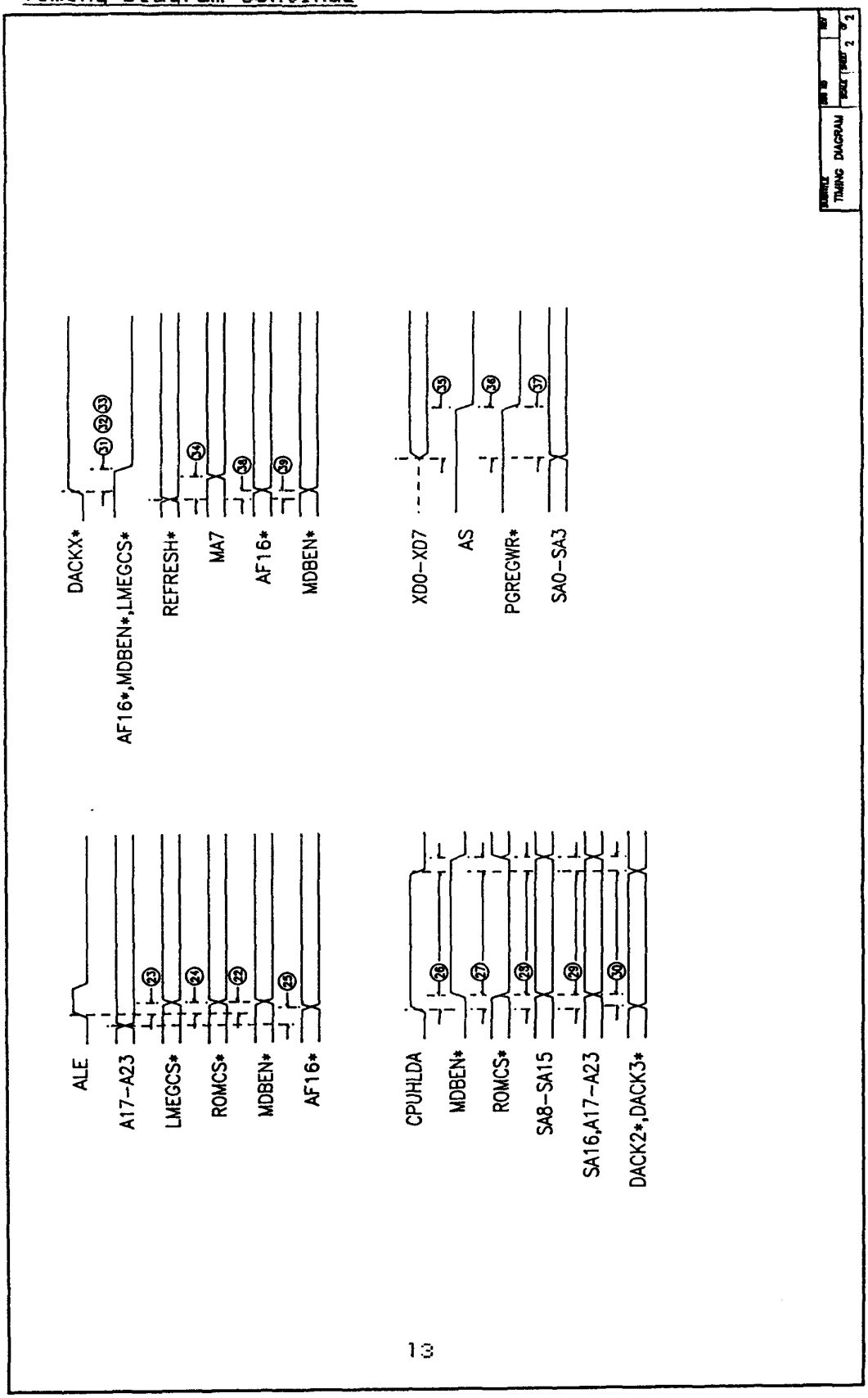
Timing Diagram Continue



9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAX RATINGS (NON-OPERATING, VSS=0.0V)

	MIN	MAX	UNITS
STORAGE TEMPERATURE	-65	+150	Degrees C.
VOLTAGE ON ANY PIN W.R.T GROUND	-0.5	7.0	Volts

OPERATING ELECTRICAL SPECIFICATIONS:

OPERATING AMBIENT	MIN	TYP	MAX	UNITS
AIR TEMP. RANGE	0	25	70	Degrees C
POWER SUPPLIES				
VCC	4.5	5.0	5.5	Volts
VSS	0	0	0	Volts

	MIN	TYP	MAX	UNITS
LEAKAGE CURRENT				
Vin = 0.0 v		20		Microamps
Vin = 5.0 v	-20			Microamps
INPUT VOLTAGES				
LOGIC "0" (Vil)		0.8		volts
LOGIC "1" (Vih)	2.0			volts

OUTPUT VOLTAGES CURRENT LOADING

LOGIC "0" (vol)			0.4	volts

MA[0]-MA[8] @ 8ma(min)
SXA8-SXA16,A17-A23 @ 4ma(min)
RASx* @ 4ma(min)
CASX* @ 8 ma(min)
Others must be able
to SINK minimum @ 2ma

LOGIC "1" (Voh)	2.4			volts

MA[0]-MA[8],
SXA8-SXA16,A17-A23 @ 8ma
CASx*,RASx* @ 4ma
CASX* @ 8 ma
Others must be able
to DRIVE minimum @ 2ma

INPUT CAPACITANCE

All inputs 0.0 < Vin < 5.0	10	picofarads

OUTPUT CAPACITANCE

MA[0]-MA[8]	200	picofarads
CAS	165	picofarads
RAS	100	picofarads
SA8-SA16	150	picofarads
All other outputs	50	picofarads