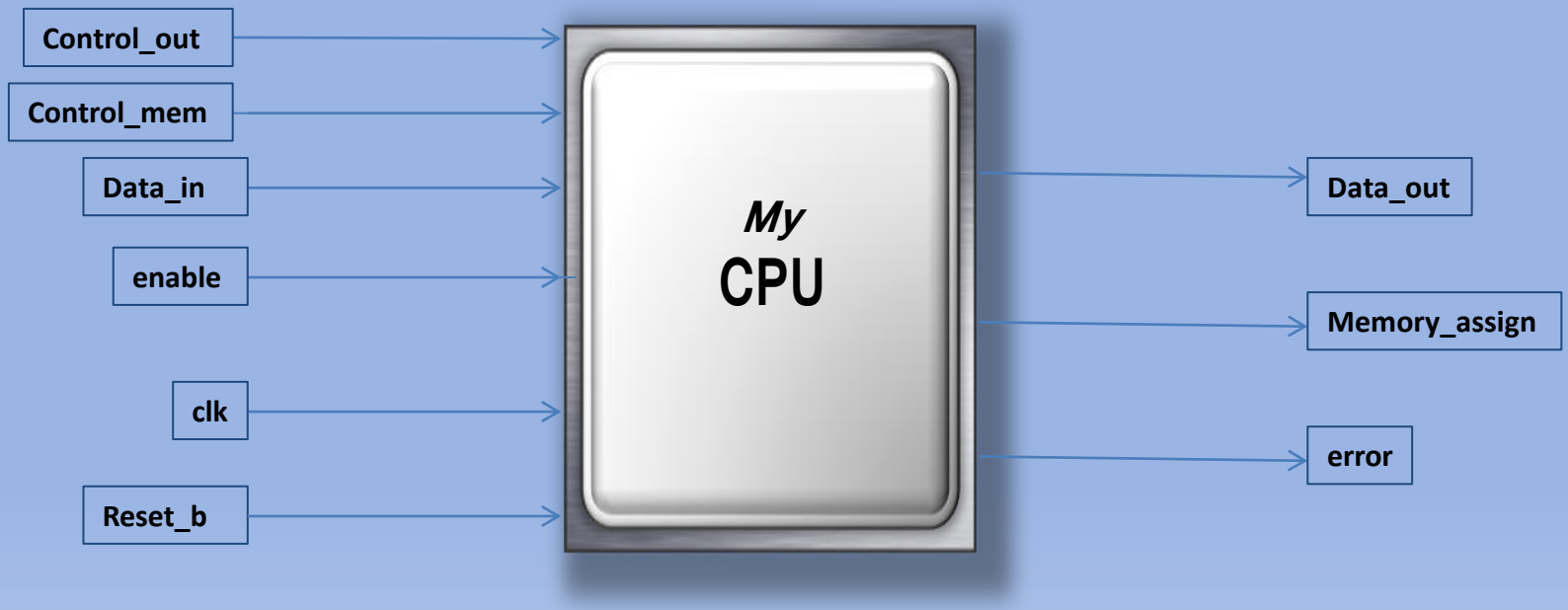
PROCESSOR DESIGN

Ankit Arora

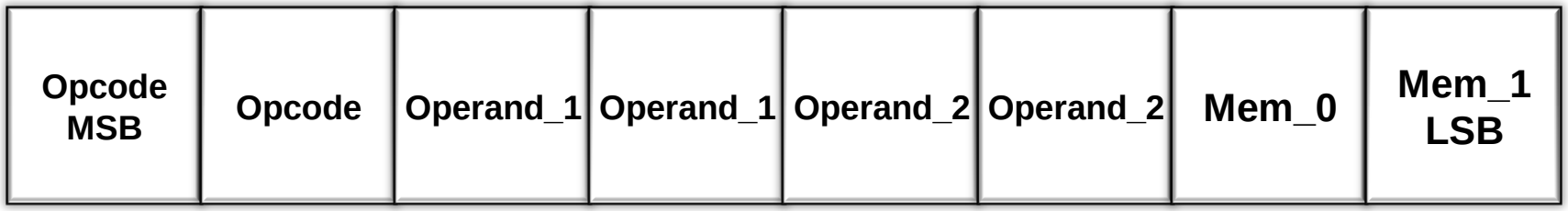
Input and output pins



Some information about my processor

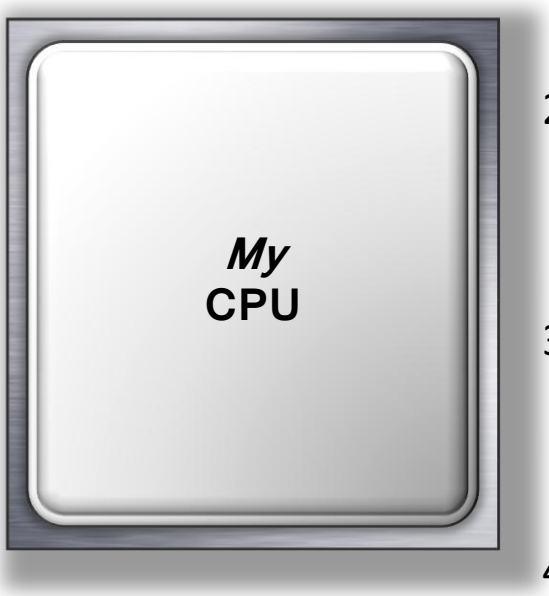
- Data memory: 2 bytes
- Instruction memory: 8 bytes
- Word size: 8 bits
- Architecture: Harvard Architecture

Instruction Register



Instruction Set

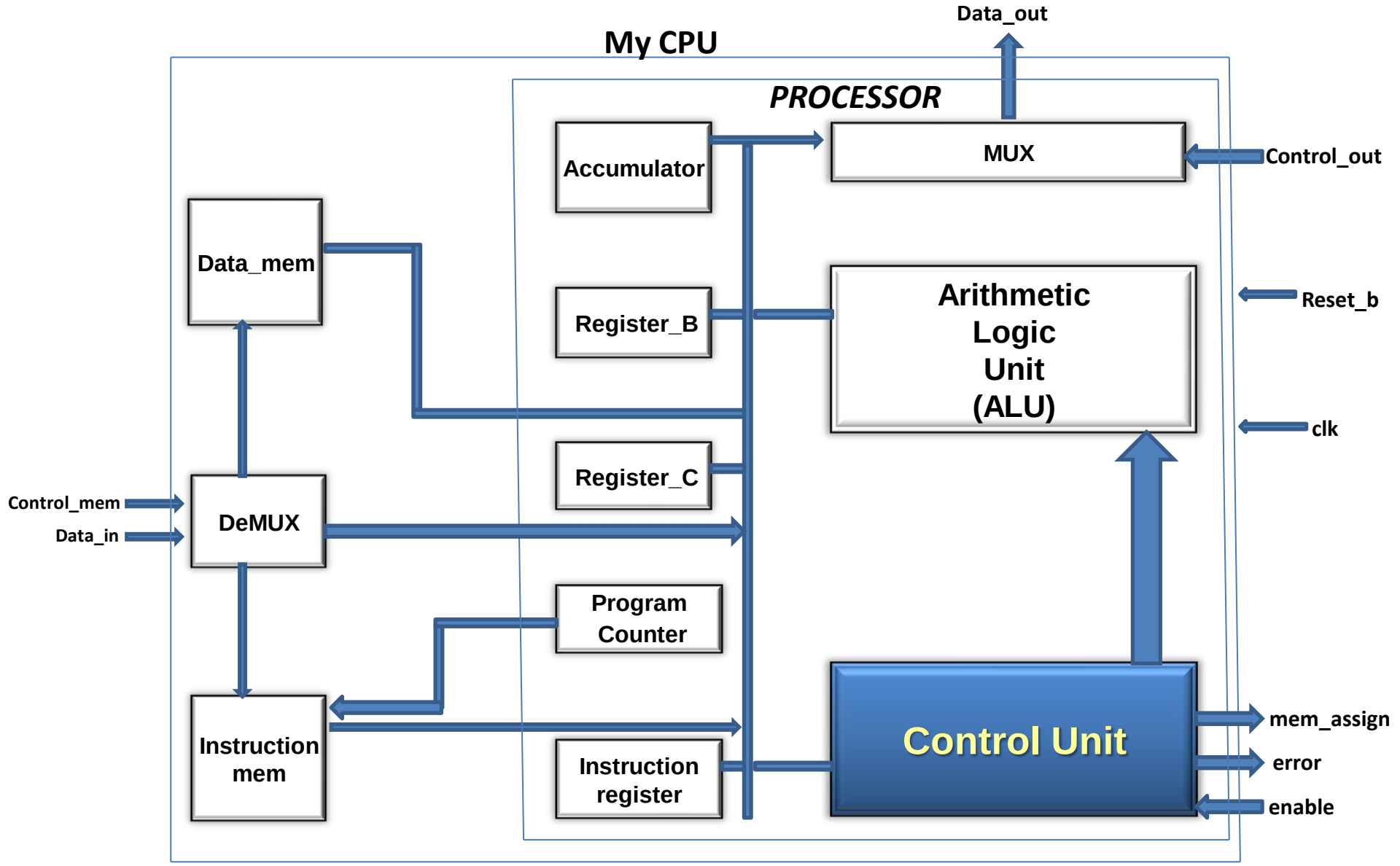
1. add reg/mem,reg/mem - used for adding the data in a register/memory to the data in another register/memory.



2. mov reg,reg - used for moving the data from one register to another register.

3. mov reg,mem - used for moving the data from the memory to a register.

4. mov mem,reg - used for moving the data from the register to a memory.


My CPU
PROCESSOR
Data_out
Accumulator
MUX
Control_out
Data_mem
Register_B
Arithmetic
Logic
Unit
(ALU)
Reset_b
clk
Register_C
Control_mem
Data_in
DeMUX
Program
Counter
Instruction
mem
Instruction
register
Control Unit
mem_assign
error
enable

Testbench

- 04 - 00000100 - add a,b
- 08 - 00001000 - add a,c
- 0c - 00001100 - add a,mem[0]
- 0d - 00001101 - add a,mem[1]

Instruction mem

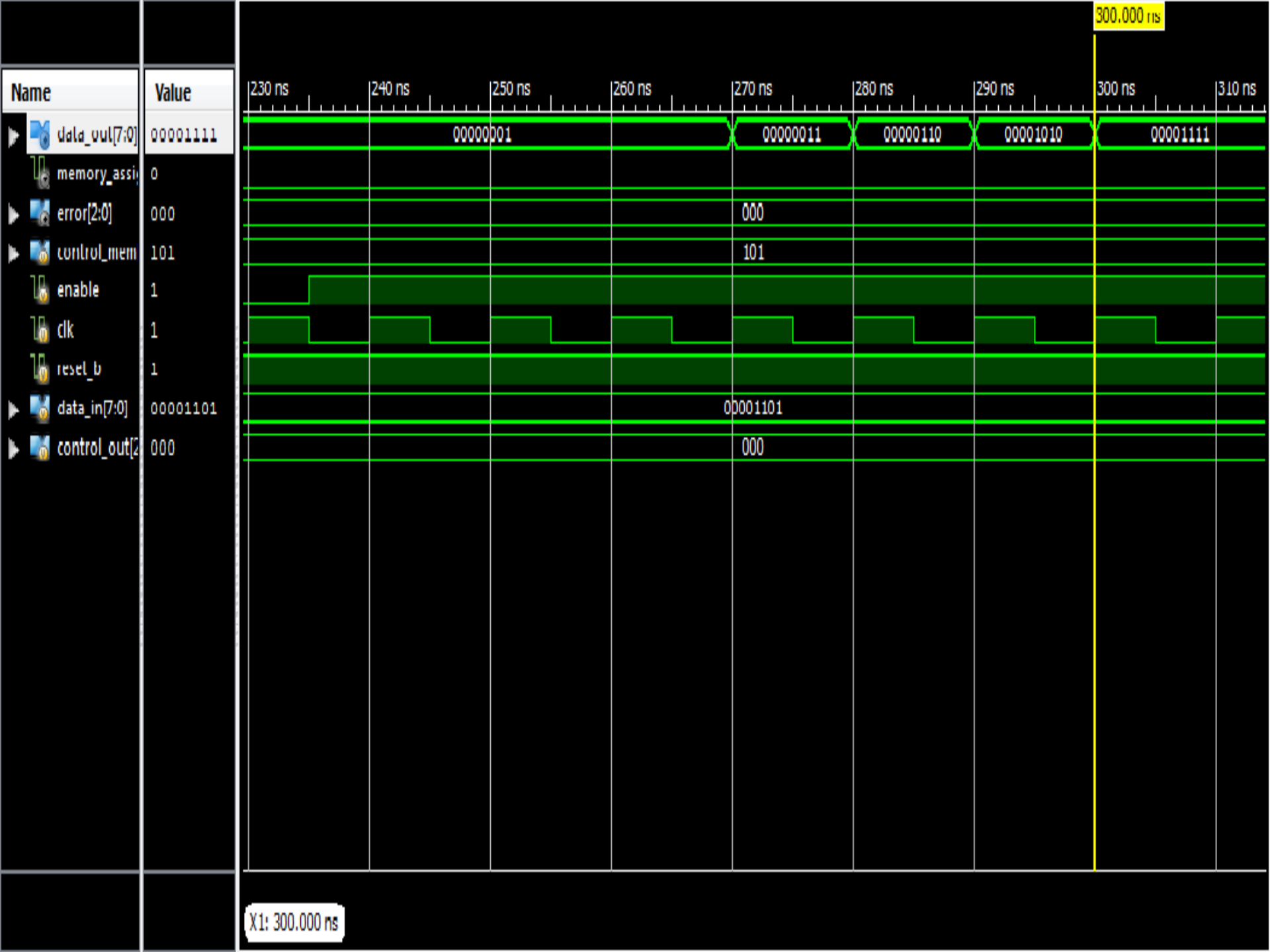
000	Add a,b
001	Add a,c
010	Add a,mem[0]
011	Add a,mem[1]
100	
101	
110	
111	

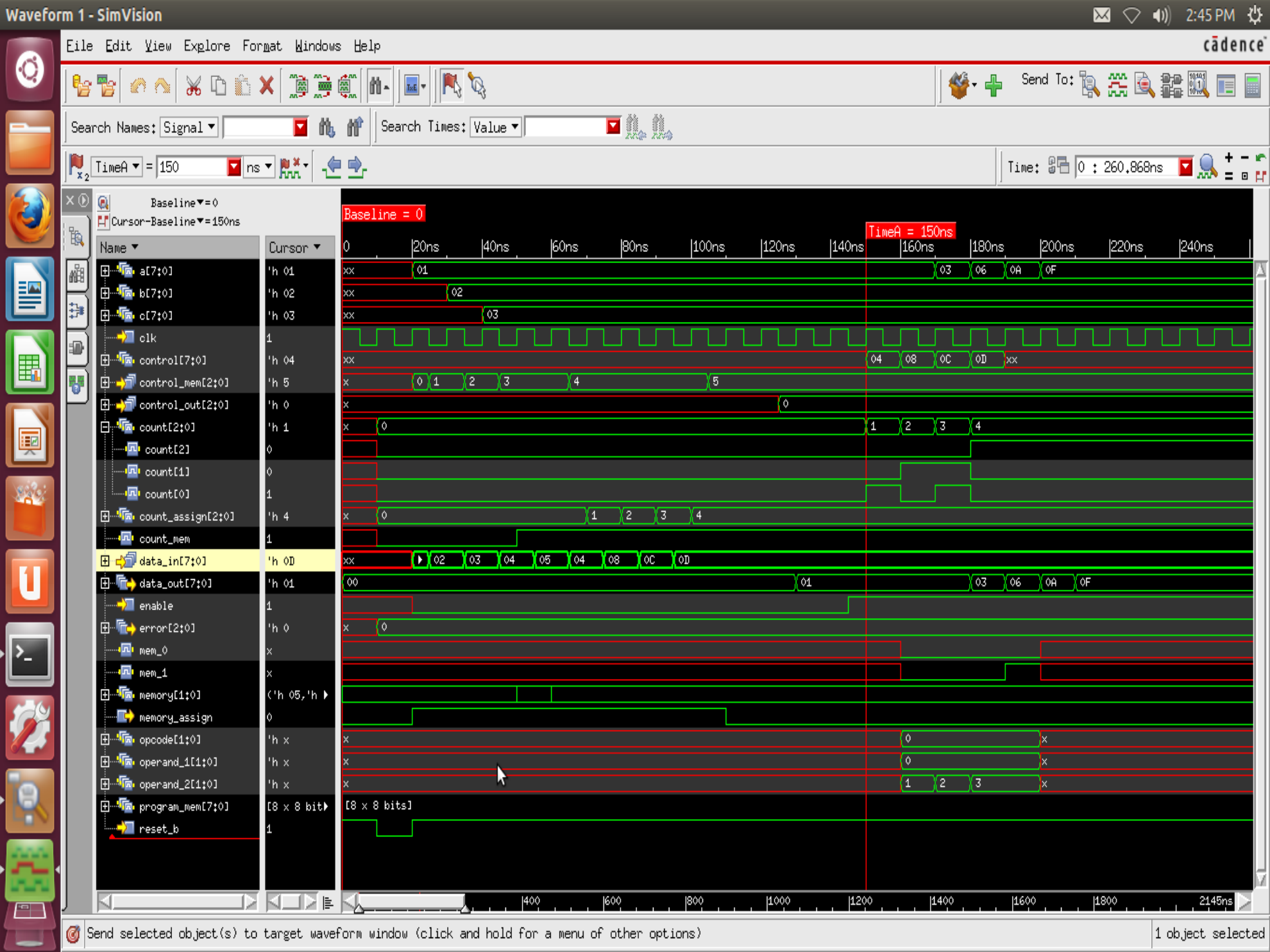
Initialization of memories:

Accumulator: 01H Register B: 02H Register C: 03H

RAM: 04H and 05H

Result stored in accumulator after the above four operations: 0FH


Name
Value
data_out[7:0]
00001111
memory_assi
0
error[2:0]
000
control_mem
101
enable
1
clk
1
resel_b
1
data_in[7:0]
00001101
control_out[2
000
300.000 ns
230 ns
240 ns
250 ns
260 ns
270 ns
280 ns
290 ns
300 ns
310 ns
00000001
00000011
00000110
00001010
00001111
000
101
00001101
000
X1: 300.000 ns


Waveform 1 - SimVision
2:45 PM
File Edit View Explore Format Windows Help
cadence
Send To:
Search Names: Signal
Search Times: Value
TimeA = 150 ns
Time: 0 : 260.868ns
Baseline = 0
Cursor-Baseline = 150ns
Name
Cursor
Baseline = 0
TimeA = 150ns
0 20ns 40ns 60ns 80ns 100ns 120ns 140ns 160ns 180ns 200ns 220ns 240ns
a[7:0] 'h 01
b[7:0] 'h 02
c[7:0] 'h 03
clk 1
control[7:0] 'h 04
control_mem[2:0] 'h 5
control_out[2:0] 'h 0
count[2:0] 'h 1
count[2] 0
count[1] 0
count[0] 1
count_assign[2:0] 'h 4
count_mem 1
data_in[7:0] 'h 0D
data_out[7:0] 'h 01
enable 1
error[2:0] 'h 0
mem_0 x
mem_1 x
memory[1:0] ('h 05,'h
memory_assign 0
opcode[1:0] 'h x
operand_1[1:0] 'h x
operand_2[1:0] 'h x
program_mem[7:0] [8 x 8 bit
reset_b 1
[8 x 8 bits]
400 600 800 1000 1200 1400 1600 1800 2145ns
Send selected object(s) to target waveform window (click and hold for a menu of other options)
1 object selected