Homework 4

CSE 232

May 2021

Design a 6 bit register for *load*, *swap*, *clear* using the control inputs (ld, sw, cl) to swap the 6 bits data inputs I5 I4 I3 I2 I1 I0 and result the data outputs Q5Q4Q3Q2Q1. The load input will load the data to register, the clear input will load 0 to the register and the swap function *swap* the consecutive bits. For example, after running the swap function, the abcdef will become badefe. The bits at location 5 and 6 are swapped, the bits at 4 and 3 are swapped, the bits at 2 and 1 locations are swapped.

(The priority rank is clear, load, swap)

Make your design following the steps below

1- Define MUX size
2- Create MUX table
3- Connect MUX input
4- Map control lines