MEF UNIVERSITY
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EE 305 Digital Electronics

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Homework 1 –Inverter

Due: 21.10.2019

Q1. An "enhancement" load inverter is shown in Figure 1. Explain how this circuit functions as an inverter. Follow these steps:

a. What is the operation mode of M_L in the figure? What is the role of M_2 ?
b. What is V_{OH} of the second inverter? Calculate it by hand. (Hint: Drain currents are 0)
c. Run SPICE simulations and plot VTCs of the inverter.
d. Compare this structure with a resistive load inverter. Comment on the advantages and disadvantages of an enhancement load inverter over a resistive load inverter.

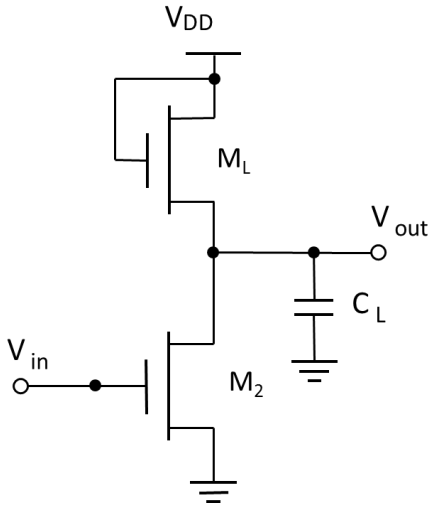

Figure 1: Enhancement load inverter

You can choose your own parameters for simulation, or use these ones:

M2 : VT = 0.7V, kn = 100µA/V^2

ML : VT = 0.7V, kn = 10µA/V^2

Q2. (Exercise 5.7, modified)

Design a CMOS inverter circuit with the following parameters:
$V_{T0,n}$ = 0.44V $\mu_n C_{ox}$ = 102µA/V^2 (W/L)=12
$V_{T0,p}$ = -0.42V $\mu_p C_{ox}$ = 51.6µA/V^2 (W/L)=19
The power supply is 1.2V. The channel length for both transistors Ln = Lp = 60nm.

a. Determine the (Wn/Wp) ratio so that the switching threshold voltage V_{th} = 0.5V.

b. The CMOS fabrication process used to manufacture this inverter allows a variation of the $V_{T0,n}$ value by ±15% around its nominal value and a variation of the $V_{T0,p}$ value by ±20% around its nominal value. Assuming that all other parameters (such as μ_n , μ_p, C_{ox}, Wn, Wp) always retain their nominal values, find the upper and lower limits of the switching threshold voltage V_{th} of this inverter. Use MATLAB to answer this question. Graphically show the change in V_{th} as a function of $V_{T0,p}$ and $V_{T0,n}$. Make a 3D plot.

Q3. (Exercise 6.10, modified)

Consider a CMOs inverter with the following parameters:
$V_{T0,n}$ = 0.5V $\mu_n C_{ox}$ = 98μA/V^2 (W/L)=10
$V_{T0,p}$ = -0.48V $\mu_p C_{ox}$ = 46μA/V^2 (W/L)=15
The power supply is 1.2V, and the output capacitance is 10fF.

a. Plot VTC and calculate the critical voltage points (V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_{th})

b. Estimate the rise time and the fall time of the output.

c. Determine the maximum frequency of a periodic square-wave input signal so that the output voltage can still exhibit a full logic swing from 0 to 1.2V in each cycle.

d. Calculate the dynamic power dissipation at this frequency.

e. Assume that the output load capacitance is mainly dominated by fixed fan-out components (which are independent of W_n and W_p). We want to re-design the inverter so that the propagation delay times are reduced by 25%. Determine the required channel dimensions of the nMOS and the pMOs transistors. How does this re-design influence the switching (inversion) threshold, V_{th} ?