DIGITAL SYSTEM DESIGN

PROJECT DOCUMENTATION

VGA CONTROLLER

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# Specification

The requirement of the project is to implement a VGA controller using an FPGA board. There must be four different images (square, circle, triangle, vertical lines) displayed on the screen which must show the ability of the controller to choose at least four different colors for the images. A button must control the switching of the images. The user should be able to move the objects on the screen along the X-axis and Y-axis using other buttons.

# General Considerations

The acronym VGA stands for Video Graphic Array and it represents a video display standard first introduced in 1987 by the IBM PS/2 line of computers. The general implementation of a VGA controller consists of 2 timing signals (Horizontal and Vertical Sync) and 3 busses that represent the bit-encodings for colors red, green and blue.

This project was implemented using a Nexys 4 DDR FPGA board and therefore each color buss has 4 bits creating a 12-bit unique pattern which can display 4096 different colors. Furthermore, the resolution considered is 640x480 pixels.

A close up of a map

Description automatically generatedThe rest of this section will present the basic functioning principles of the VGA port and the VGA timing constraints according to the FPGA board reference manual.

The first displays to use the VGA standard were CRT-based (cathode-ray tube). The main components of a CRT-display are the signals, the electron guns, the deflection coils, a high voltage source connected to the screen and the cathode-rays themselves (as seen in the image on the right). The cathode ray ‘hits’ the screen with electrons controlled by the electron guns. As a result of this collision, the inner phosphor coat of the display glows at the exact point where the impact happened. The color emanated depends on the RGB signals which are driven to the electron guns. The horizontal and vertical sync (HS and VS) signals control the movement of the electron beam through the deflection coils, making the cathode-ray traverse the screen on a pixel-by-pixel basis.

HS and VS have the role of synchronizing the electron beam with the display. A pixel clock of 25MHz represents the time available for the controller to print one pixel; it also coordinates HS and VS. An entire time period of the horizontal sync signal can be split into 4 distinct frames: display time (640 pixel clocks) – effective writing of pixels, front-porch (16 pixel clocks) – changing direction from forward moving to backward, sync pulse (96 pixel clocks) – traversing the screen from right to left without displaying anything on the screen, it also coincides with the only time when HS is not active – and back-porch (48 pixel clocks) – changing direction from backward moving to forward. A similar logic is used for VS: display time (480 rows), front-porch (1 row), sync pulse (3 rows), back porch (16 rows).

The LCD displays no longer have cathode rays. The acronym stands for liquid-cristal display; the colors displayed on the screen are controlled through voltage imposed across the liquid cristal to change the light permittivity of a very small area. The crystal properties are change on pixel-by-pixel basis. LCD’s have adapted their functioning to work with the same timing signals as the CRT displays, so the same implementation logic can be used.

# Block Diagram

A picture containing wall, indoor

Description automatically generated

Input and output description:

* fpga\_clock: input, internal clock of the FPGA board, used to obtain the pixel clock for the VGA controller and to control the debouncers linked to the buttons
* imgBtn: input, button, controls the switching of the images
* btnLeft: input, button, used for moving the image along the X-axis one pixel left on each press
* btnRight: input, button, used for moving the image along the X-axis one pixel right

on each press

* btnUp: input, button, used for moving the image along the Y-axis one pixel up on each press
* btnDown: input, button, used for moving the image along the Y-axis one pixel down on each press
* RIn [3:0]: bus input, switches, receives the red component of the pixel color
* GIn [3:0]: bus input, switches, receives the green component of the pixel color
* BIn [3:0]: bus input, switches, receives the blue component of the pixel color
* H\_Sync: output, horizontal sync signal
* V\_Sync: output, vertical sync signal
* R [3:0]: bus output, red component of the color
* G [3:0]: bus output, green component of the color
* B [3:0]: bus output, blue component of the color

Note: All outputs of the controller are sent directly to the VGA port, which will then display an image on the screen.

# Project Implementation

The project contains a total of 14 source files which can be divided into 7 basic MSI components, 6 major modules built from the MSI components and a top module file in which the major modules are instantiated and connected.

## Basic MSI components

### AND\_GATE

A close up of a logo

Description automatically generated

Generic Parameters:

* N: size of the input bus

Inputs and Outputs:

* Input [N-1:0]: std\_logic\_vector input of variable length; generic parameter N gives the number of wires in the bus
* Gate\_output: std\_logic output

This component implements a basic and-gate with a variable number of inputs which are received through a bus. This is done using a generic parameter *N* which gives the number wires of the input bus. The output represents a single standard logic signal: the result of the and logic operator ‘and’ applied to all of *input*’s terms.

### D Flip Flop

A close up of a logo

Description automatically generated

Generic Parameters: none

Inputs and Outputs:

* D: std\_logic input
* CLK: std\_logic input, clock signal of the component
* Q: std\_logic output

This component implements a basic D Flip Flop that changes its state on the rising edge of the clock pulse. The output *Q* will take the value of input *D* when the clock signal changes from ‘0’ to ‘1’.

### D Flip Flop for Integers

Generic Parameters:

* Nr\_range: range of integer signals

Inputs and Outputs:

* D: integer input
* Ce: std\_logic input
* Clk: std\_logic input
* Q integer output

It has a similar behavior to the previous component, the only differences are the type if *D* and *Q* signals, which are integers, and the feature of having a clock enable (*ce*) signal. If *ce* has value ‘1’ then the output takes the value of input *D* on the rising edge of the clock signal *clk*, otherwise the counter is inactive, and it maintains its previous state.

### Offset Counter

A picture containing object

Description automatically generated

Generic Parameters:

* numberRange: maximum value of output

Input and Output:

* enable: std\_logic input
* plus: std\_logic input, clock signal of the component
* offset: integer output, its range is given by the generic parameter

This component implements a counter which has the clock enable feature implemented and whose output variable is of type integer. If the input *enable* is active (has value ‘1’) then the counter increases the output value by one unit on every rising edge of the clock, *pulse*. If *enable* is not active, the counter does not work. The range of the output is given by the generic parameter *numberRange*: it can take values between 0 and *numberRange* – 1. When *offset* reaches its upper limit the counter resets automatically on the next clock cycle.

If we assume *ce* is ‘1’ and that the generic parameter has value 10 then the following table show the behavior of the counter:

|  |  |
| --- | --- |
| CURRENT STATE | NEXT STATE |
| 0 | 1 |
| 1 | 2 |
| 2 | 3 |
| 3 | 4 |
| 4 | 5 |
| 5 | 6 |
| 6 | 7 |
| 7 | 8 |
| 8 | 9 |
| 9 | 0 |

### A picture containing object Description automatically generatedCounter

Generic Parameters:

* Nr\_bits: gives the size of the output bus

Inputs and Outputs:

* Reset: std\_logic input
* Clock: std\_logic input, clock signal of component
* Q [nr\_bits – 1: 0]: std\_logic\_vector output

This is a basic counter on a variable number of bits with an asynchronous reset. On the rising edge of the clock signal, the output *Q* will increase with one unit.

If *reset* is active (has value ‘1’) then regardless of the previous state *Q* will be set to 0. If *reset* is ‘0’ and assuming the generic parameter has value 3 the following table shows the behavior of the counter:

|  |  |
| --- | --- |
| CURRENT STATE | NEXT STATE |
| 000 | 001 |
| 001 | 010 |
| 010 | 011 |
| 011 | 100 |
| 100 | 101 |
| 101 | 110 |
| 110 | 111 |
| 111 | 000 |

### Integer Counter

Generic parameters:

* Max\_value: gives the range of the output

Inputs and Outputs:

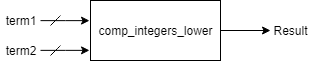
* Clk: std\_logic input, clock signal of the component
* Count: integer output

This component implements a counter whose output is and integer. The output’s maximum value is given by the generic parameter. The counter goes to the next state on the rising edge of the clock cycle. If the value of the output has reached the maximum value, the counter will reset automatically on the next clock cycle.

If we assume that *max\_value* is given value 5 the counter has the following behavior.

|  |  |
| --- | --- |
| CURRENT STATE | NEXT STATE |
| 0 | 1 |
| 1 | 2 |
| 2 | 3 |
| 3 | 4 |
| 4 | 0 |

### Integer comparator



Generic parameters:

* Number\_range: maximum value of input signals

Inputs and Outputs:

* Term1: integer input
* Term2: integer input
* Result: std\_logic output

This component implements a basic comparator between two variables of integer type. It returns an std\_logic signal as an output which is ‘1’ if *term1* is strictly lower than *term2*, otherwise *result* is 0.

## Main Project Modules

### Frequency divider

Block diagram:

Internal schematic:

A screenshot of a cell phone

Description automatically generated

Generic Parameters: none

Inputs and Outputs:

* Clk\_in: std\_logic input
* resetDivider: std\_logic input
* clk\_out: std\_logic input

Notations used:

* Inter [1:0]: std\_logic\_vector internal signal, represent the output of the counter component inside the frequency divider

This module implements a frequency divider using as an internal component a 2-bit counter. The aim of the module is to obtain the pixel clock (which for the 640x480 resolution should have a value of 25MHz). In order to do that, the *clk\_in* signal is connected to the internal clock of the FPGA board. For a Nexys 4 DDR board, this clock has a frequency of 100MHz, which means it should be divided by 4 to obtain a frequency of 25MHz. This is done through the usage of the 2-bit counter. Since 4 = 22, we only need to connect to most important bit of the output of the counter to *clk\_out*. The output of the frequency divider will therefore be the pixel clock. The *resetDivider* input of the frequency divider is connected to the *reset* of the counter and when it has value ‘1’ it would reset the counter to 0. However, in this project the divider should work continuously without interruption so *resetDivider* is connected to the ground.

### Debouncer

Block diagram:

A screenshot of a social media post

Description automatically generatedInternal schematic:

Generic parameters:

* Nr\_bistabile: gives the number of flip flops inside the debouncer

Inputs and Outputs:

* Btn\_in: std\_logic input
* Clk: std\_logic input, clock signal of component
* Btn\_out: std\_logic output

Notations used:

* Inter [1:nr\_bistabile]: std\_logic\_vector, each element of the vector represents the output of a flip flop

Note: in the internal schematic scheme, *n* is used instead of *nr\_bistabile* for simplicity

The term ‘bouncing’ refers to the situation when a button is pressed and its corresponding signal switches from a low voltage to a high voltage and then back several times before it steadies on the high value. This happens due to mechanical reasons, since the contact between the metal pieces of the button is not perfect. If, for example, the button would be connected to a counter as the clock signal, it would cause the counter to jump several states on a single button press instead of just one state, which is the expected effect.

In an ideal situation where all the physical circuits would only have perfect contacts between their components the signal triggered by a button press would look something like this:

A close up of a logo

Description automatically generated

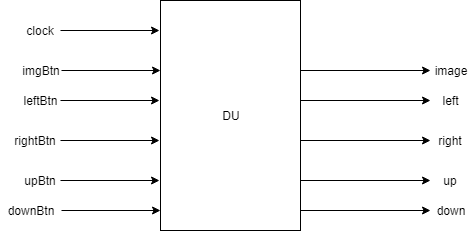
A close up of a logo

Description automatically generatedThis is what we expect to happen when a button is pressed, but what the waveform of the signal looks like in reality is more like the next graphic:

In order to avoid this situation, the button signal must first go through a debouncer – a component whose purpose is to ‘clear’ the signal and avoid the bouncing phenomena. The output of the debouncer should have a waveform like the first one presented previously (the one without any bounce periods), but with a small delay between the moment the button is pressed and the moment when the debouncer’s output switches from ‘0’ to ‘1’.

The debouncer implemented for this project consists of a several D-flip flops and an and-gate. The number of flip flop inside the debouncer is given by a generic parameter, *nr\_bistabile*, which would also give the size of the input bus of the and-gate. All flip flops have the same clock signal, *clk*. The input of the first one is connected to *btn\_in*, which is the button pressed. For all others, the input is connected to the output of the previous flip flop. All the outputs represent wire of *inter*, which will then be linked to an and-gate, whose output will be the output of the entire module. Basically, *btn\_out* will be ‘1’ only when all the flip flops will have value ‘1’, which means the button signal stopped switching between high and low voltages.

### DU – debounce unit

Block diagram:

Internal schematic:

A close up of text on a black background

Description automatically generated

Generic parameters: none

Inputs and Outputs:

* Clock: std\_logic input, clock signal of the component
* imgBtn: std\_logic input, button
* leftBtn: std\_logic input, button
* rightBtn: std\_logic input, button
* upBtn: std\_logic input, button
* downBtn: std\_logic input, button
* image: std\_logic output, debounced signal corresponding to imgBtn
* left: std\_logic output, debounced signal corresponding to leftBtn
* right: std\_logic output, debounced signal corresponding to rightBtn
* up: std\_logic output, debounced signal corresponding to upBtn
* down: std\_logic output, debounced signal corresponding to downBtn

This component represents a series of debouncers, one for each button from the user interface of the project. An internal constant called *nr\_bistabile* will give the number of flip flops inside the debouncers. Thus, this value can be easily changed.

### VGA Controller

Block diagram:

A close up of text on a white background

Description automatically generatedInternal schematic:

### Top Module File

A close up of text on a white background

Description automatically generatedInternal schematic:

# Justification of the Chosen Solution

We chose to implement the project in a modular and easy to understand fashion. The solution is optimal for several reason. Firstly, the modules are built in such a way that any future improvement or modification would need a minimum amount of changes. Depending on what we want to change, we might only need to update some values used in the controller of maybe some lines of code. At most it might be necessary to change or implement new modules, but since all the major components of the project are independent of each other it is not needed to build a new project from scratch.

Secondly, the code written has a general character meaning that it could be used as it is for similar projects with only few adjustments. The algorithm implemented is the same for any VGA controller no matter what resolution, FPGA board or what image\_generator module is used, so the project has a high portability.

To sum up, the solution this project gives for a VGA controller is modular, easy to modify and portable to other types of FPGA boards; all these characteristics justify why we chose to implement the project in the manner presented in this documentation.

# Usage and Maintenance Instructions

If we want to see the way the project functions, the first step that must be done is to connect the FPGA board to a display through the VGA port. After that we can load the code on the FPGA board and after a few moments the image of a circle will appear on the screen. From this point forward the user will control what happens next using the buttons and switches available on the board.

There are four different images to be displayed: a circle, a square, a triangle and vertical lines. To switch from image to the next one, button 1 must be pressed once.

The images can be moved within the bounds of the display using four more buttons: buttons 3 and 5 for the x-axis (left and right respectively) and buttons 2 and 4 for the y-axis (up and down respectively).

At any time while the project is active, the color of the objects can be changed using 4 sets of switches. The background will always remain white. The rightmost four switches of the board correspond to the blue component of the color, the next four switches control the green component and the next four control the red component. (Note that the leftmost four switches are not used so changing their state will not have any effect). Within each of these sets of four, the leftmost switch controls the least significant bit of the color encoding, while the rightmost switch controls the most significant bit of the color. Having all the switches set on ‘0’ will make the object black, while having all the switched on ‘1’ will make the object white, which is the same color as the background so in this case the object will no longer be visible.

# Further Development Possibilities

There are several improvements that could be brought to this project. For examples, instead of having a component that decides the color of each pixel based on its position on the screen, the images could be stored into a memory and then received from there when they should be displayed. Since no more computations would be needed in this case, the images could also be more complex, not only geometric shapes. Furthermore, depending on the capacity of the memory used, there could be more images, not just four. Of course, with enough images and with the right timing, instead of displaying independent images, the controller could be programmed to display a movie by displaying related and nearly identical images fast enough so that it gives the viewer the impression of movement. All these changes could be achieved by replacing the image\_generator module from the project with another appropriate component. If the user is no longer given the opportunity to move the images in the x- and y-axis, then the two instances of positionCalculator from the top module could also be removed. This could be the case when the VGA controller projects a movie on the screen and the user does no longer interact with it, they only watch the images displayed.

Another idea of development would be to change the resolution of the images displayed. In order to do this, the only changes needed are the values of some constants inside the vga\_controller module so that they match the characteristics and the timing constraints of the resolution we want to use.

Finally, this project only implements a module that displays images on a screen. It could be integrated into a bigger and more complex project that needs a VGA controller to display images on a screen.