Instructions to Perform Post-Route Simulation using Xilinx Project Navigator (10.1)

1. Create a New Project with a VHDL Source File.
2. On the ***Sources For*** drop down menu, click on ***Post-Route Simulation***.
3. Under the project device, if the Behavioral Source file is present, right click on VHDL file and click ***Remove***.
4. Click on ***Add Existing Source*** and add the original VHDL source file again. This time the Behavioral file should not show up in the ***Post-Route Simulation*** menu.
5. Click on the ***Source For*** drop down menu and select ***Implementation***.
6. Select the VHDL file. After completing the code for the file, double click on ***Generate Post-Place & Route Simulation Model*** in the ***Processes*** window under the ***Implement Design*** -> ***Place & Route*** tab.
7. On the ***Sources For*** drop down menu, click on ***Post-Route Simulation***.
8. This time only the Structural VHDL file should be present under the device. Click on the Device name and expand the ***Design Utilities*** tab. Double click on ***Compile HDL Simulation Libraries***.
9. After the library compilation is complete, click on the Structure VHDL file, expand the ***ModelSim Simulator*** tab and double click on ***Simulate Post-Place & Route Model***.
10. This will open up ModelSim and allow a real time simulation of the project.