|  |  |  |
| --- | --- | --- |
| PC | FPGA |  |
| |  |  |  |  | | --- | --- | --- | --- | | A | 0 | 0 | 0 | | 0,360081102030721 | 1 | 0,737192965930063 | | 0 | 0 | 0 | | B | 0 | 0 | 0 | | 0,395560366907624 | 0,683415866967978 | 0,704900321963127 | | 0 | 0 | 0 | | I | 0 | | | | |  |  |  |  | | --- | --- | --- | --- | | A | 0 | 0 | 0 | | 0,9541015625 | 1 | 0,513671875 | | 0 | 0 | 0 | | B | 0 | 0 | 0 | | 0,52734375 | 0,8642578125 | 0,970703125 | | 0 | 0 | 0 | | I | 0 | | | | |  |  | | --- | --- | | Step size | 0.01 | | Maximum iteration number | 10 | | Number of pixels | 30 | | Number of learning loops | 100 | | Learning rate | 0.01 | |

