Middle East Technical University
Department of Electrical and Electronics Engineering

EE348 INTRODUCTION TO LOGIC DESIGN
FINAL EXAM

June 11, 2023
Duration: 150 min.

PLEASE READ BEFORE STARTING

- This is a closed-book exam.
- There are five questions; attempt all.
- Use the reserved spaces to answer each question.
- Show all steps of your work.
- You cannot use earphones, calculators, cellular phones, or any other electronic device during the exam.
- Do not leave the classroom for the first 30 minutes and the last 15 minutes.
- Please scan and upload your final paper on odtuclass before returning it.

GOOD LUCK

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Name : Erdem
Student No : 2374676
Signature : Eeny
Section : I forget my section

QUESTION	CREDIT	GRADE
Q1	20	
Q2	20	
Q3	20	
Q4	20	
Q5	20 + 5	
TOTAL	100 + 5	

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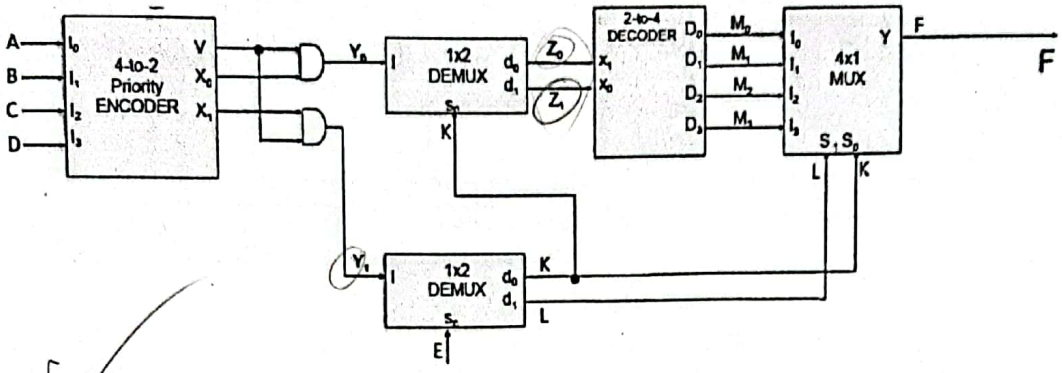
Q1 [20P]: The circuit below has five input signals, A, B, C, D, and E, and one output signal, F. Also note the naming of the intermediate signals and enumerating of the input/output pins of the components.



a. **[3P]** Write the truth table of the 4-2 priority ENCODER where the inputs are I_0=A, I_1=B, I_2=C, and I_3=D, and the outputs are V, X_0, and X_1. Then, write Y_0 and Y_1 in terms of A, B, C, and D. Note that the input priority order is $I_3>I_2>I_1>I_0$.

b. **[2P]** Write the truth table of the DEMUX with the variables I, s_0, d_0, and d_1. Then, write Z_0 and Z_1 in terms of Y_0 and K, and K and L in terms of Y_1 and E.

c. **[3P]** Write the truth table of the 2-to-4 DECODER where the inputs are $x_1=Z_0$ and $x_0=Z_1$, and the outputs are $D_0=M_0$, $D_1=M_1$, $D_2=M_2$, and $D_3=M_3$. Then, write M_0, M_1, M_2, and M_3 in terms of Z_0 and Z_1.

d. **[3P]** Write the truth table of the 4x1 MUX where the inputs are $I_0=M_0$, $I_1=M_1$, $I_2=M_2$, and $I_3=M_3$, and the select bits are S_0=K and S_1=L, and the output is Y=F. Then, write F in terms of M_0, M_1, M_2, M_3, K, and L.

e. **[5P]** Based on the expressions you have found in the previous parts, obtain the input-output relation of the whole circuit, i.e., write F in terms of A, B, C, D, and E.

f. **[2P]** Now assume that the output is connected to one of the DEMUXs instead of the input signal E. Namely, E=F, as shown in the figure next page. Then, try to obtain the input-output relation of the modified circuit, i.e., write F in terms of A, B, C, and D.

g. **[2P]** Based on your answer in part **(f)**, comment on the characteristics of this circuit. Is it working as a combinational or sequential circuit?

Note: While providing the truth tables, you may use some groupings to reduce the number of rows when possible.

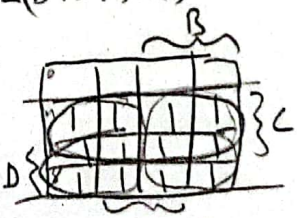
(a)

D C B A	X_1 X_0 V
0 0 0 0	0 0 0
0 0 0 1	0 0 1
0 0 1 X	0 1 1
0 1 X X	1 0 1
1 X X X	1 1 1

D C B A	X_1 X_0 V	
0 0 0 0	0 0 0	0
0 0 0 1	0 0 1	1
0 0 1 0	0 1 1	2
0 0 1 1	0 1 1	3
0 1 0 0	1 0 1	4
0 1 0 1	1 0 1	5
0 1 1 0	1 0 1	6
0 1 1 1	1 0 1	7
1 0 0 0	1 1 1	8
1 0 0 1	1 1 1	9
1 0 1 0	1 1 1	10
1 0 1 1	1 1 1	11
1 1 0 0	1 1 1	12
1 1 0 1	1 1 1	13
1 1 1 0	1 1 1	14
1 1 1 1	1 1 1	15

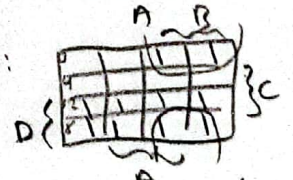
$V=(D+C+B+A)$

X_1:



$X_1 = D+C$

X_0:

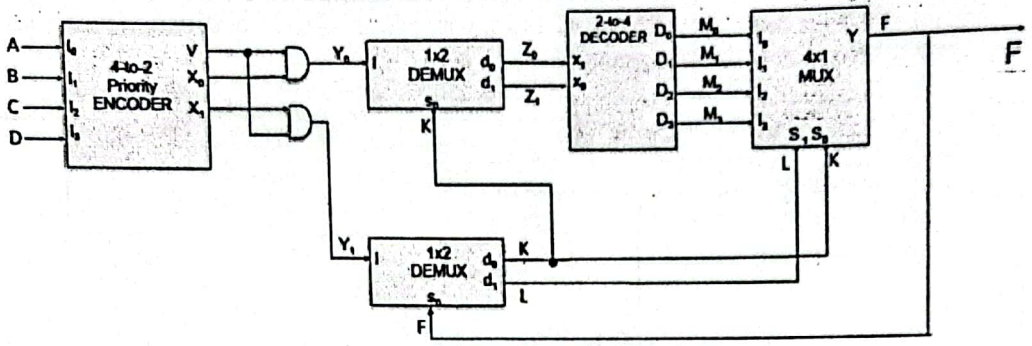


$X_0 = D+C'B$

$Y_0 = V \cdot X_0 \rightarrow (D+C+B+A)(D+C'B)$

$Y_1 = V \cdot X_1 \rightarrow (D+C+B+A)(D+C)$ //

Modified circuit figure for part (f)



(b) demux truth table, write Z_0 & Z_1 into K & Y_0
K & L into Y_1 & E

S_0	I	d_1	d_0
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

$Z_0 = K'Y_0$ $Z_1 = KY_0$

$K = E'Y_1$ $L = EY_1$

(c) 2-4 decoder truth table

X_1	X_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

for $X_0 = Z_1$ & $X_1 = Z_0$, write M_i's

$M_0 = X_1'X_0' = Z_0'Z_1'$ $M_2 = X_1X_0' = Z_0Z_1'$

$M_1 = X_1'X_0 = Z_0'Z_1$ $M_3 = X_1X_0 = Z_0Z_1$

(d) 4x1 MUX truth table

S_1	S_0	F
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

write F in terms of M_i, K & L

$S_1 = L$, $S_0 = K$, $I_i = M_i$

$F = S_1'S_0'M_0 + S_1'S_0M_1 + S_1S_0'M_2 + S_1S_0M_3$

$F = L'K'M_0 + L'KM_1 + LK'M_2 + LKM_3$

(e) $F = L'K'M_0 + L'KM_1 + LK'M_2 + LKM_3$

$L = EY_1 = E(D+C+B+A)(D+C)$

$K = E'Y_1 = E'(D+C+B+A)(D+C)$

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Q2 [20P]: Using **only six 1-bit binary full adders**, design a magnitude comparator with the following specifications:

The inputs to the comparator are 2-bit unsigned binary numbers ($A=A_1A_0$, $B=B_1B_0$).

The comparator has 3 outputs such that

if A=B than E=1, G=0, L=0

if A<B than E=0, G=0, L=1

if A>B than E=0, G=1, L=0

$E = (A_1 \odot B_1) \cdot (A_0 \odot B_0)$

$A>B = (A_1 B_1') + (A_1 \odot B_1)(A_0 B_0')$

$A<B = [E + (A>B)]'$

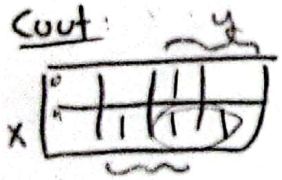
No additional components are available. Logic levels 1/0 are available.

Make the connections and write the Boolean expressions for each connection.

*Some inputs and outputs are already labeled.

X	y	Cin	S	Cout	
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	2
0	1	1	0	1	3
1	0	0	1	0	4
1	0	1	0	1	5
1	1	0	0	1	6
1	1	1	1	1	7

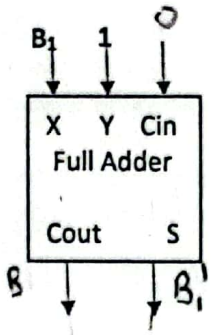
Cout:

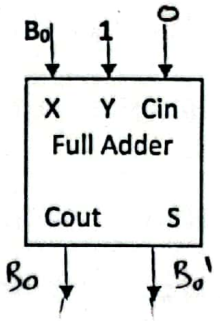


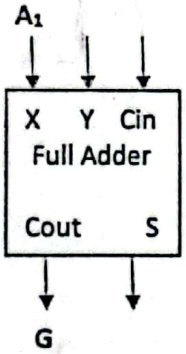
$Cout = Cin(x \oplus y) + xy$

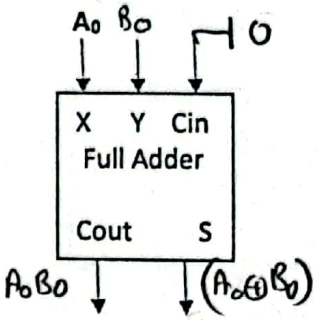
S:

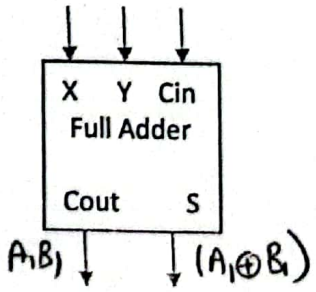
$S = x \oplus y \oplus Cin$

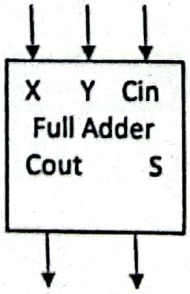












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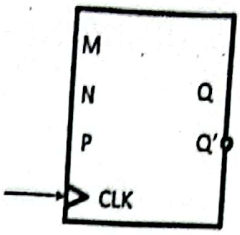
Q3 [20P]: A special type of Flip Flop that has three inputs (called MNP Flip Flop) has the following characteristics.

M	N	P	Q(t+1)
0	0	0	1
0	0	1	Q(t)
0	1	0	Q'(t)
0	1	1	NA
1	0	0	1
1	0	1	Q(t)
1	1	0	Q'(t)
1	1	1	NA



a. Find the characteristics equation in the simplest form as sum of products (SP) with K-map for the input order Q, M, N, P.

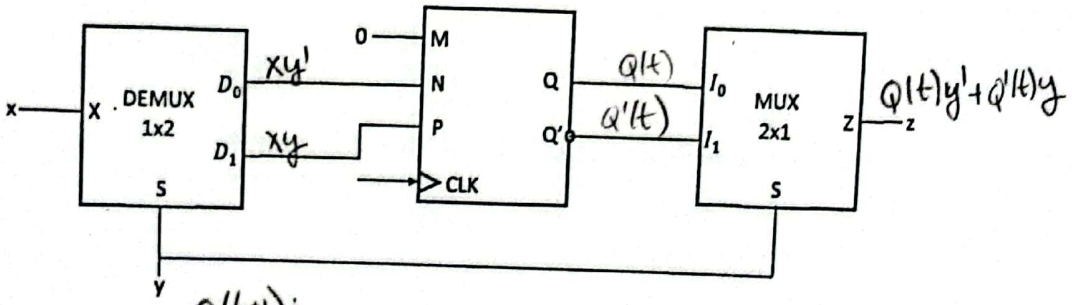
b. Obtain the excitation table of the MNP flip-flop. Use don't care where applicable.

c. Consider the below sequential circuit for analysis.

   i. Find the next state equation in terms of the inputs x, y and the present state.

   ii. Find the output z in terms of the inputs x, y and the present state.

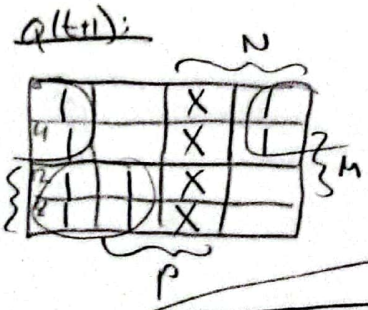
Do all the simplifications where applicable and obtain the simplest expression for both i and ii.



(a)

Q(t)	M	N	P	Q(t+1)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	X
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	X
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	X
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	X

Q(t+1):



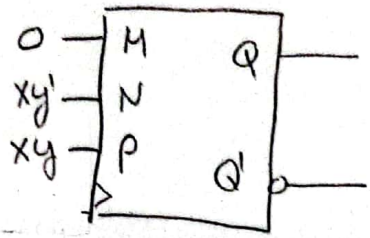
$$Q(t+1) = Q(t)N' + Q'(t)P'$$

(b)

Q(t)	Q(t+1)	M	N	P
0	0	X	X	1
0	1	X	X	0
1	0	X	1	X
1	1	X	0	X

00, 01, 10, 11
00, 01, 10, 11
00, 01, 10, 11
00, 01, 10, 11

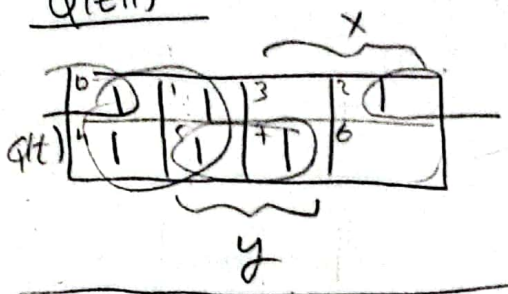
C-i



Q(t)	Q(t+1)	M	N	P
0	0	X	X	1
0	1	X	0	0
1	0	X	1	X
1	1	X	0	X

	Q(t)	x	y	N	P	Q(t+1)
0	0	0	0	0	0	1
1	0	0	1	0	0	1
2	0	1	0	1	0	1
3	0	1	1	0	1	0
4	1	0	0	0	0	1
5	1	0	1	0	0	1
6	1	1	0	1	0	0
7	1	1	1	0	1	1

Q(t+1):



$$Q(t+1) = x' + Q'(t)y' + Q(t)y$$

C-ii

$$Z = Q(t)y' + Q'(t)y$$ //

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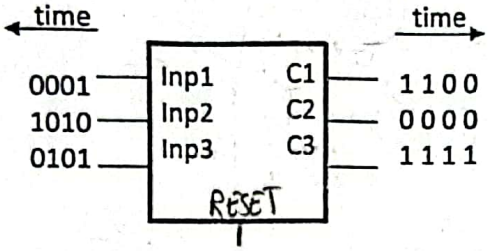
Q4 [20P]: Consider a sequential circuit that operates in serial mode and accepts 3 4-bit unsigned numbers. This circuit is a serial comparator that determines the maximum of 3 numbers (I1, I2, I3) and outputs 3 bits (C1 C2 C3) which shows the place(s) of the maximum(s) of the numbers received up to that time. MSB bits are fed first. Initially C1=1, C2=1, C3=1
For example, if I1=1000, I2=0101, I3=1010



Time	I1	I2	I3	C1	C2	C3
0	X	X	X	1	1	1
1	1	0	1	1	0	1
2	0	1	0	1	0	1
3	0	0	1	0	0	1
4	0	1	0	0	0	1

a. **[2P]** How many states are there in the state machine defined by the described algorithm. How many flip flops are needed in designing such a circuit?

There are 8 states that can be generated by 3 flip flops and required basic gates, note that one of the states (i.e 000) is unused.

b. **[4P]** Fill in the blank spaces in the timing diagram below.

↳ atleast one should be larger or two should be equal

Time	I1	I2	I3	C1	C2	C3
0	X	X	X	1	1	1
1	1	0	1	1	0	1
2	1	1	1	1	0	1
3	0	0	1	0	0	1
4	0	1	0	0	0	1

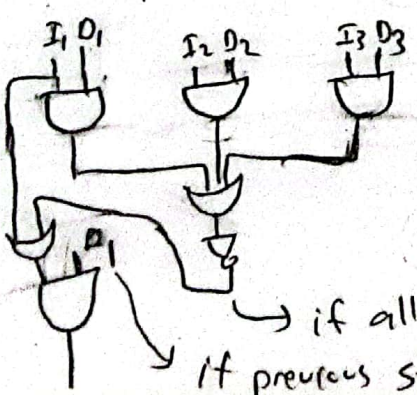
c. **[4P]** Assume your circuit is in the present state 101. Determine all next states and the corresponding state transitions from this state.

I assume that there is an async reset so that the circuit can be returned to time 0 state, then possible states are;

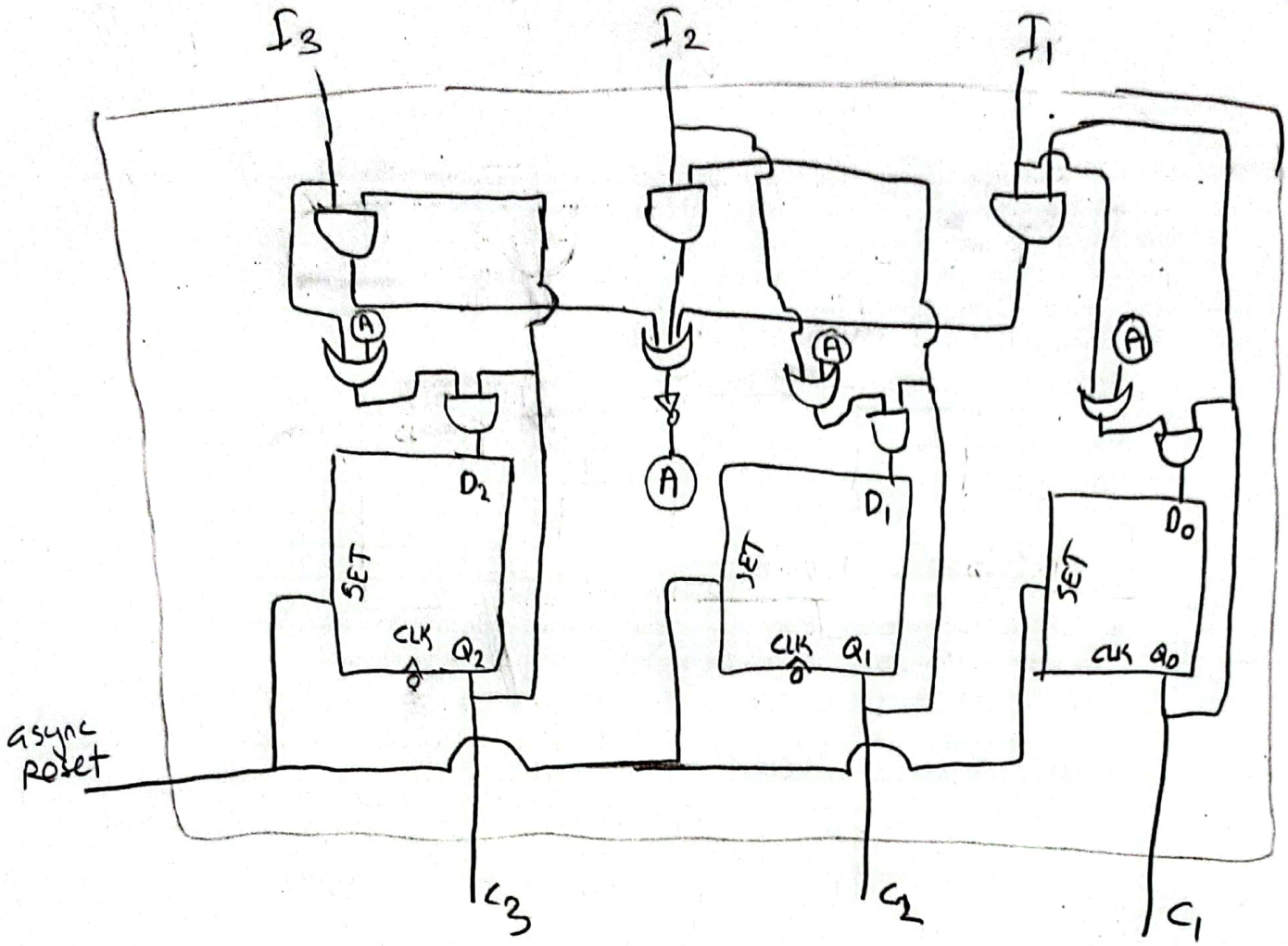
sync → 101, 100, 001 · async → 111

d. **[8P]** Design the circuit by using positive or negative edge-triggered D Flip Flops. You may use NOT, AND, OR gates (multi-input allowed).

* initially state is 1
* reset state if
  ↳ previous state is 0 → $Q(t+1) = Q(t)[\cdots]$
  ↳ if previous state is 1
  input is zero & there is nonzero inputs with positive previous state



↳ if all zero → among the remaining ones preserve previous states
If previous state is zero → keep it zero



⊗ if A is 1, all of the remaining candidates have zero input. So that the states should not change

e. **[2P]** Someone claims that this circuit is scalable in that it is possible to find the maximum among 1 million numbers with such a circuit. This claim is not completely correct when delays in the circuits are taken into account. Which part in your design prevents this simple scaling?

I am taking digital electronics course, so that I know we cannot connect ∞ many loads to the output of the gate (capacitor charge & discharge time causes delays) in drawings the gate level is the same even for ∞ many numbers, however as # gates increases, the rise & fall time also increases → clock becomes relatively fast. At that moment, we should screams and all kind of unexpected results are seen.

help!

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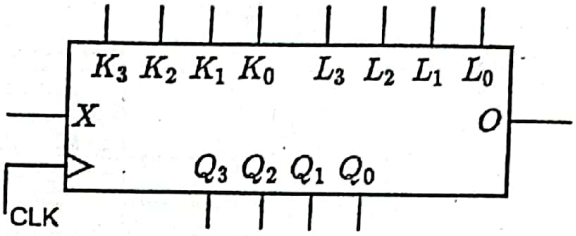
Q5 [20P + 5P Bonus]: We want to design a synchronous sequential circuit that can be used for a mathematical operation on 4-bit unsigned numbers.

a. **[10P]** In the first step, we want to design a circuit with the inputs and outputs shown in the figure on the right-hand side.



- There is one 1-bit input X
- There are two 4-bit inputs K and L
- There is one 1-bit output O
- There is one 4-bit output Q which also represents the state of the circuit
- There is one clock input

The circuit operates as follows:

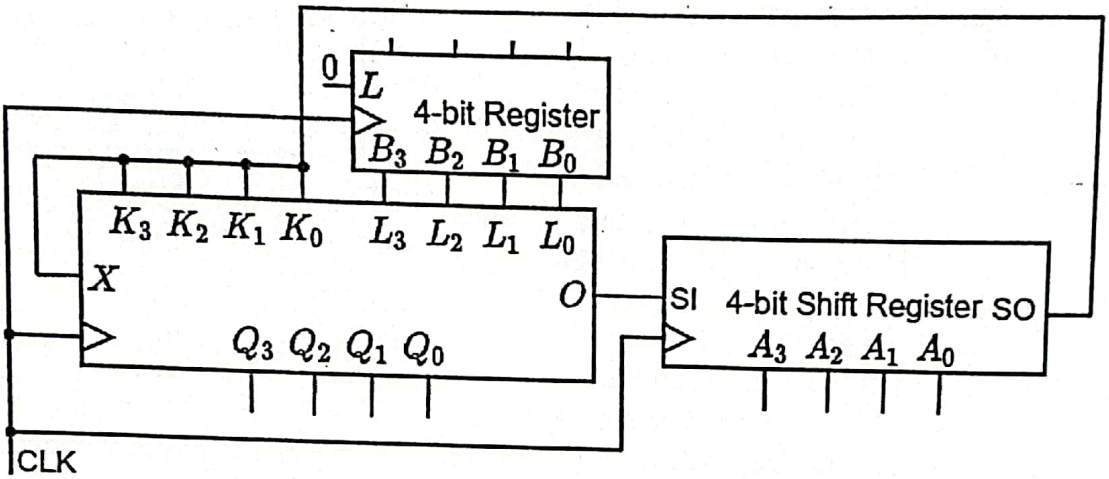
- If $X = 0$, we add up K and Q
- If $X = 1$, we add up L and Q
- In both cases, the least significant bit of the result is available at output O
- In both cases, the most significant bits of the result including the carry bit are transferred to Q with the next positive clock edge

Design and draw the circuit using only the following components:

- One simple 4-bit register with only a clock input built with 4 D-FFs as in the lecture
- One Quad 2 x 1 multiplexer
- One 4-bit binary adder

Note: Do not only draw the circuit but explain your design!

b. **[10P]** We next use the circuit designed in part **(a)** as part of the circuit in the figure below (note that you can answer this question even you could not solve part **(a)**).



In addition to the circuit in part **(a)**, this circuit has one 4-bit shift register and one 4-bit register with parallel load, whereby the load input is constant 0. Assume the 4-bit register with parallel load has the constant value $B_3B_2B_1B_0 = 1101$, the state of the circuit in part **(a)** is initialy $Q_3Q_2Q_1Q_0 = 0000$ and the initial value of the 4-bit shift register is $A_3A_2A_1A_0 = 0101$. Fill in the table below for four successive clock pulses.

CP	Q_3	Q_2	Q_1	Q_0	A_3	A_2	A_1	A_0
Initial	0	0	0	0	0	1	0	1
↑								
↑								
↑								
↑								

c. **[Bonus – 5P]** How would you call the mathematical operation that is realized by the circuit in part **(b)**? **Explain your answer!**
Hint: Compare the values of A, B before and Q, A after the operation.