Middle East Technical University
Department of Electrical and Electronics Engineering

EE464: Static Power Conversion-II

Hardware Project Final Report

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Introduction

This is the final report for the hardware project of the EE464 Static Power Conversion II course prepared by Emine BOOSTancı group.

In this project an isolated DC/DC battery charger is designed according to the following specifications.

- Minimum Input Voltage: 20 V
- Maximum Input Voltage: 40 V
- Output Voltage: 12 V
- Output Power: 60 W
- Output Voltage Peak-to-Peak Ripple: 3%
- Line Regulation (Deviation of percent output voltage when input voltage is changed from its minimum to maximum or vice versa): 3%
- Load Regulation (Deviation of percent output voltage when the load current is changed from 10% to 100% or vice versa): 3%

Firstly, possible topologies are introduced to meet these requirements and the initial design considerations according to the selected design, flyback converter is presented. Then, the magnetic and controller design for this topology is presented. After that, simulation results for the circuit that can be physically realizable are given. Then the selected components are listed. Thermal analysis of the switching devices are also provided. After that experimental results of the designed circuitry are shared. Lastly, cost and compactness analysis of the circuit are presented in this report.

Topology and Design Selection

For this project, the following isolated DC/DC converter topologies are assessed.

Flyback Converter:

Flyback converter topology is suitable for low to medium power applications (typically up to 100 Watts), which fits the 60W requirement.

Advantages:

- Flyback has the minimum number of components. There is only one transformer which is also used as an inductor.
- There is no restriction on the duty cycle.
- Design and control of the topology is the easiest.
- No need for resetting the core’s magnetic flux.

Disadvantages:

- Leakage inductance is a problem since it does not have a discharging path. Using snubbers decrease the efficiency of the converter. Adopting a two switch or interleaved topology will complicate the design and control of the converter.
- For high power topologies efficiency is the lowest compared to the other alternatives.
- Output voltage ripple is higher compared to other alternatives. Thus, additional filtering might be needed.

Forward Converter:

The forward converter is suitable for power levels from 50 Watts to a couple of hundred watts.

Advantages:

- This topology is generally more efficient than the flyback converter.
- This topology has better transient response compared to the flyback converter.
- This topology has better lower output ripple compared to the flyback converter due to the output inductor.
- This is the least complex topology after the flyback converter.
- There are no center tapped windings.

Disadvantages:

- This topology has a more complex magnetic design compared to flyback converter due to the additional inductor. Additional inductor will increase the magnetic and copper losses. Notice that the switching frequency seen by the inductor is twice of the switching frequency.
- Flux of the transformer must be reset in one switching cycle. Otherwise, the flux will aggregate and cause saturation which will result in problems in the power transfer. Therefore, the maximum duty cycle is limited. This will complicate the design and control of the converter. This will complicate the design of the converter.
- There are more components compared to the flyback converter thereby it is more expensive and less compact.

Push Pull Converter:

The push pull converter is suitable for medium power levels (100 Watts to a few kilowatts).,

Advantages

- Transformer size is reduced because the core is utilized more effectively.
- This topology has better lower output ripple and voltage regulation compared to the flyback and forward converter.
- A smaller variation in D can help achieve the desired output voltage with twice the gain compared to a forward converter.

Disadvantages:

- Two switches will have to be controlled with a phase shift of half a period. More difficult control. Deadtime adjustment may be required.
- Same problems with additional inductor are present too.
- Inductors' core losses will happen at twice the frequency of operation.
- The duty cycle is also limited for this topology.
- This topology has more components than the flyback and forward converter.
- This topology is more complicated than the other two topologies.

Half Bridge and Full Bridge Converter:

The Half Bridge and Full Bridge Converters are suitable for medium to high power ranges (typically 100 Watts to over 500 Watts).

Advantages

- Same advantages as push-pull but better efficiency and power density.
- Furthermore, the fill factor challenge eased compared to a push-pull converter since there is a single primary.

Disadvantages

- Same disadvantages as push-pull but complexity of the converter is increased.
- For full bridge converter additional switches increase the losses.
- For half bridge converter nonidentical switches might cause problems in terms of voltage division.

Push-pull, half and full bridge converter topologies are overdesign for this project since the output power is 60W. Therefore, the real candidates are flyback and forward converter topologies. Since there is a limit on the duty cycle and risk of flux accumulation on the core, the design and control of the forward converter. Also, additional inductance and 3rd winding increase the complexity of the magnetic design. Although the flyback converter's efficiency is inferior due to the snubber circuit for leakage inductance discharge, an optimization or an application note can be utilized to optimize the efficiency of the converter. Moreover, two switch flyback topology can be used. Although this will increase the complexity due to the drive of the high side switch it will enable us to feed the stored energy on the leakage inductor back to the input capacitor instead of dissipating it on the resistor in the snubber circuit. This will increase efficiency. Another disadvantage of the two switch flyback is the fact that the duty cycle is limited to 0.5 due to the diodes on the input side. For now, the snubber design will be selected as the solution of the discharge path of the leakage inductor. It is aimed to complete the first design as soon as possible so that the design can be changed to two switched flyback is efficiency would be smaller than the aimed one.

Another important decision is whether to operate at CCM or DCM. Since flux drops zero at DCM of operation the magnetic core is utilized better. Also, control of the converter is easier due to the linear relationship between output voltage and duty cycle as can be seen in Figure 1. However, the

analytical understanding of the DCM operation is harder in terms of equations therefore the design is more complex. In addition to this, the current ripple is higher for DCM operation. This will increase semiconductor losses. Furthermore, the output voltage ripple will increase, and an additional filter might be used to meet the 3% voltage ripple condition. Since a controller that can operate at CCM is found, to meet voltage ripple and load regulation criteria CCM operation is chosen.

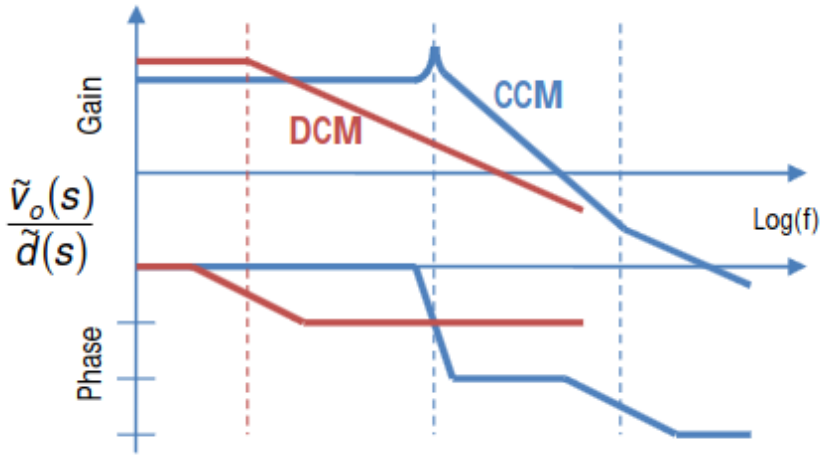


Figure 1 Bode Plots For DCM and CCM Mode of Operation

After selecting the topology and the mode of operation, switching frequency, turns ratio and duty cycle range are determined.

- Switching frequency (f_s) selection: Switching frequency is chosen as 100 kHz. Increasing the switching frequency will enable us to have a smaller ripple at the output and give us the chance to decrease L_m. Decreasing L_m will enable us to utilize the core more efficiently. However, increasing frequency will increase the switching losses of the transistors, core losses and conduction losses. In addition to these, increase in switching frequency will increase the leakage inductances. Therefore, an optimal choice is made as 100 kHz. Also, it is aimed to complete the project in PCB which will solve the leakage inductance problem compared to Pertinax.
- Turns Ratio (N) and Duty Cycle Range (D) Selection: The input output specifications shows that the voltage will be decreased. Hence, choosing duty cycle below 0.5 is more logical and will ease turns ratio selection. Also, selecting maximum duty cycle high will increase the effects of the parasitic inductances and resistances which will magnify the effect of the nonidealities to the input output relation. The voltage relationship for the flyback topology is given below. According to this equation, the maximum and minimum duty cycle for different turns ratio is plotted in Figure 2. The turns ratio is selected as 1 since the understanding will be much easier and the maximum and minimum duty cycles are computed as 0.375 and 0.23 which are smaller than 0.5.

$$\frac{V_{out}}{V_{in}} = N\frac{D}{(1-D)}$$

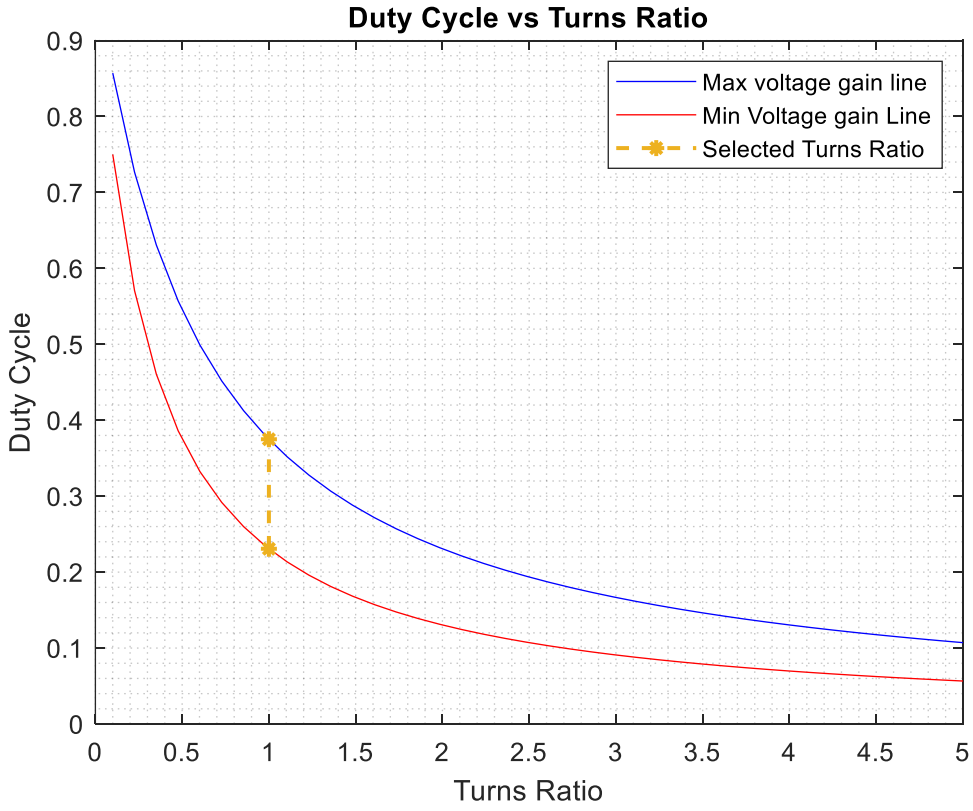


Figure 2 Duty Cycle vs Turns Ratio wrt Max and Min Voltage Gain

Magnetic Design

In this part, we need to decide the magnetizing inductance on the primary side L_m, a magnetic core, number of turns and the winding cables. Then, the magnetic and copper losses of the transformer are calculated. Lastly, the transformer is wound and magnetizing and leakage inductances and primary and secondary winding resistances are measured by LCR meter.

Before selecting the core, the magnetizing inductance in the primary side L_m is determined. The L_m decided so that the converter does not work in DCM mode but also the peak inductor current is not too high so that the core is not saturated. For these conditions the average inductor current and the current ripple are important. The average inductor current depends on the average current and duty cycle. To find the average input current the efficiency of the converter must be known. For now, the efficiency of the converter will be estimated as 70%.

$$P_{in} = \frac{P_{out}}{\eta} = 86\ W$$

$$I_{in,avg,max} = \frac{P_{in}}{V_{in,min}} = 4.29\ A$$

$$I_{in,avg,min} = \frac{P_{in}}{V_{in,max}} = 2.14\ A$$

Input current is equal to the primary side inductor current for DT_s and zero for the rest of the switching period. The relationship between the primary side inductor current and the input current is given as follows.

$$I_{Lm,avg} = \frac{I_{in,avg}}{D}$$

Maximum and minimum average primary side inductor current are calculated as 11.43 A and 9.29 A respectively.

For the current ripple K_{rf} is defined as the ripple factor as given in Figure 3.

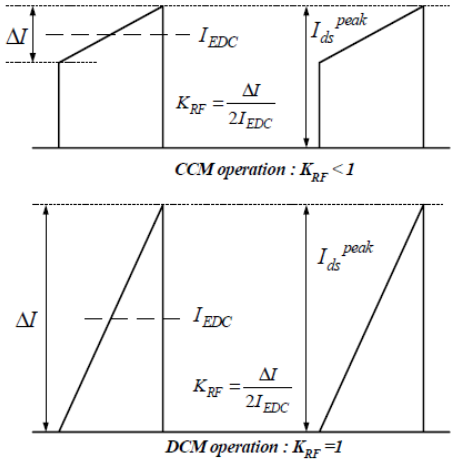


Figure 3 Ripple Factor

In order to avoid DCM operation K_{RF} must be smaller than 1. Also, smaller K_{RF} will decrease the output voltage ripple. However, lower K_{RF} might increase the transformer flux which will lead to the saturation of the core. For safety 0.5 K_{RF} is avoided. The needed inductance can be calculated as follows.

$$L_m > \frac{(V_{in}^{max}\ D_{min})^2}{2\ P_{in} f_s K_{RF}} = \frac{(40V\ 0.238)^2}{2\ (86W)(100kHz)0.5} = 10\ \mu H$$

Primary side inductance is selected as 20 µH.

The saturation must be avoided to transfer power efficiently. The saturation is determined by the peak current. The primary peak current is plotted with respect to the input voltage in Figure 4.

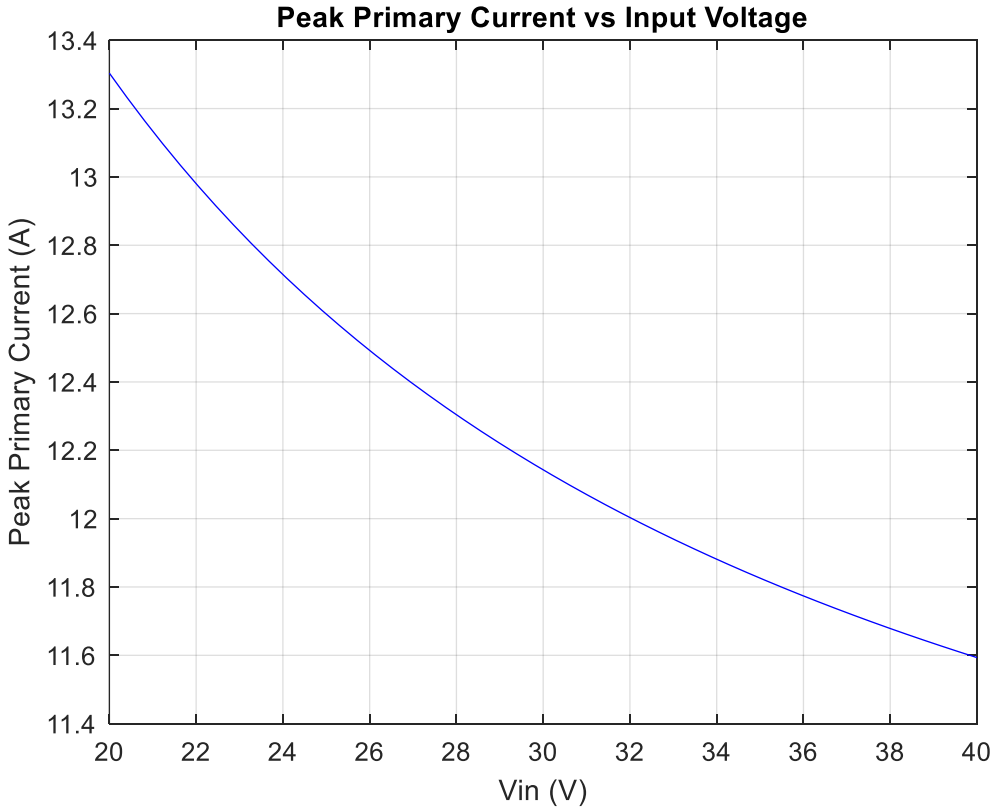


Figure 4 Peak Primary Current vs Input Voltage

From Figure 4 it can be seen that the maximum peak current occurs when the input voltage is minimum. This value is calculated as 13.3 A.

Now it is time for magnetic core selection. For core selection there are two options, a distributed gap core or a ferrite core. The relative permeability of the distributed gap cores is small, the leakage inductance is higher with respect to the ferrite core. Since the leakage inductance is dangerous for the switches a ferrite core 0R45530EC which is available in the laboratory is selected. One of the reasons to select this core is that its cross section area is high thus the saturation of the core can be easily avoided. Also, operating around 100 mT is aimed so that the core losses will be minimized although the volume of the core is increased. Another reason for selecting this core is the fact that its window area is the largest. This will ease the winding procedure.

To decide the number of turns in the primary side the core flux density and the length of the air gap will be considered. Half of the flux passing through the center leg of the core will be passing through the side legs. Nevertheless, the cross section area of the side legs is not exactly half of the cross section area of the center leg. Therefore, the magnetic field density will not be equal in the center leg and the side legs. It is known that the maximum primary current will occur when the duty cycle is maximum. Thus, the maximum magnetic field density will occur in the maximum duty cycle. The relationship between primary turns number and magnetic field density is given below.

$$R_{core} = \frac{N_1^2}{L_m}$$

$$\emptyset = \frac{N_1 I_{Lm,peak}}{R_{core}} = \frac{L_m \, I_{Lm,peak}}{N_1}$$

$$B = \frac{\emptyset}{A} = \frac{L_m \, I_{Lm,peak}}{A \, N_1}$$

To illustrate the relation between magnetic flux density and primary turns number these two are plotted with respect to each other in Figure 5. It can be seen that the center leg saturates more than the side legs.

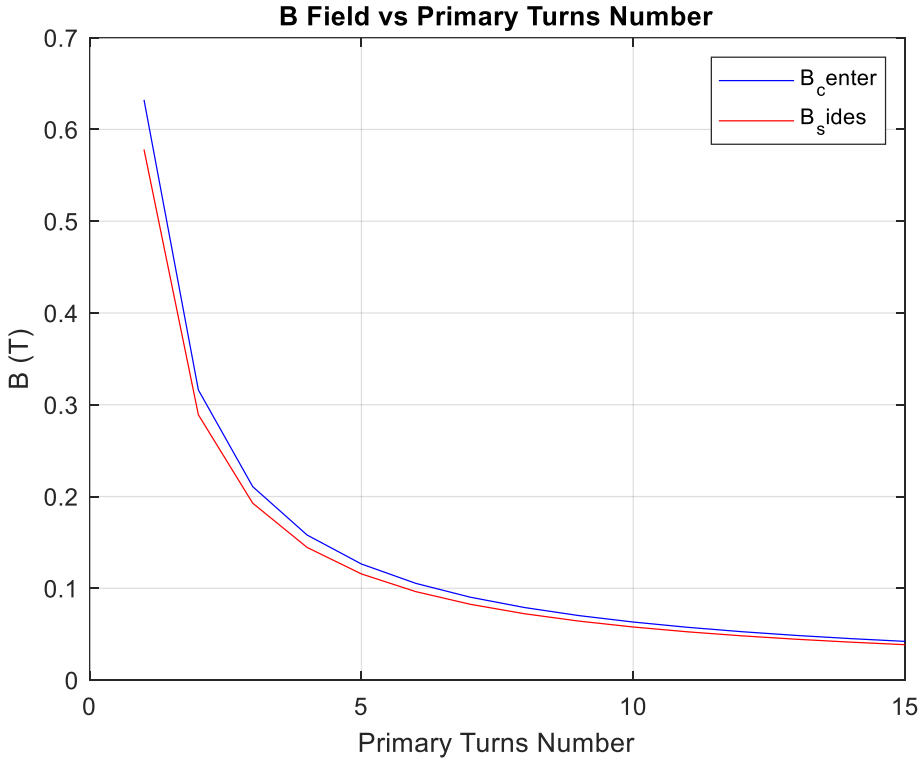


Figure 5 Magnetic Field Density vs Primary Turns Number

Before selecting the primary turns number, we need to also consider the air gap length. Since the relative permeability of the core is 2300 the reluctance of the core is negligible with respect to air gap reluctance. The magnetic circuit of the transformer is given in Figure 6. Reluctance of the side legs and center leg can be found as follows.

$$R_{side} = \frac{l_{gap}}{\mu_0 A_{side}}$$

$$R_{center} = \frac{l_{gap}}{\mu_0 A_{center}}$$

$$R_{core} = R_{center} + \frac{R_{side}}{2} = \frac{N_1^2}{L_m}$$

$$l_{gap} = \frac{N_1^2}{L_m} \frac{2\mu_0 A_{center} A_{side}}{A_{center} + 2A_{side}}$$

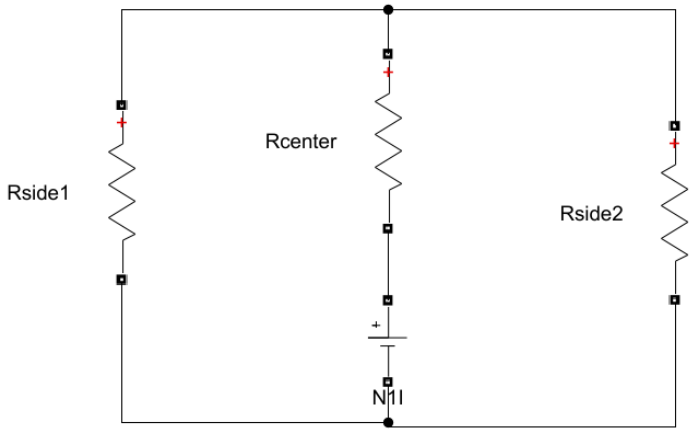


Figure 6 Magnetic Circuit of the Transformer

In order to determine the primary turns number, the air gap length is plotted with respect to the primary turns number in Figure 7.

From Figure 5 it can be seen that increasing the primary turns number will decrease the magnetic field density. However, increasing the primary turns number will also increase the air gap length. This is not desired due to the increasing fringing fields with increasing airgap length which can be seen from Figure 7. From both of these figures, the primary turns number is selected as 6. It can be seen that maximum magnetic flux density of the center leg is 1.05 T and air gap length is 5 mm for the selected turns number. The peak magnetic flux density is small enough to minimize the core loss and also the air gap length is small enough to ignore the fringing fields.

$$N_1 = 6\ turns$$

$$N_2 = \frac{N_2}{N_1} N_1 = 1 * 6 = 6\ turns$$

Magnetic field density vs the duty cycle for center and side legs are given in Figure 8.

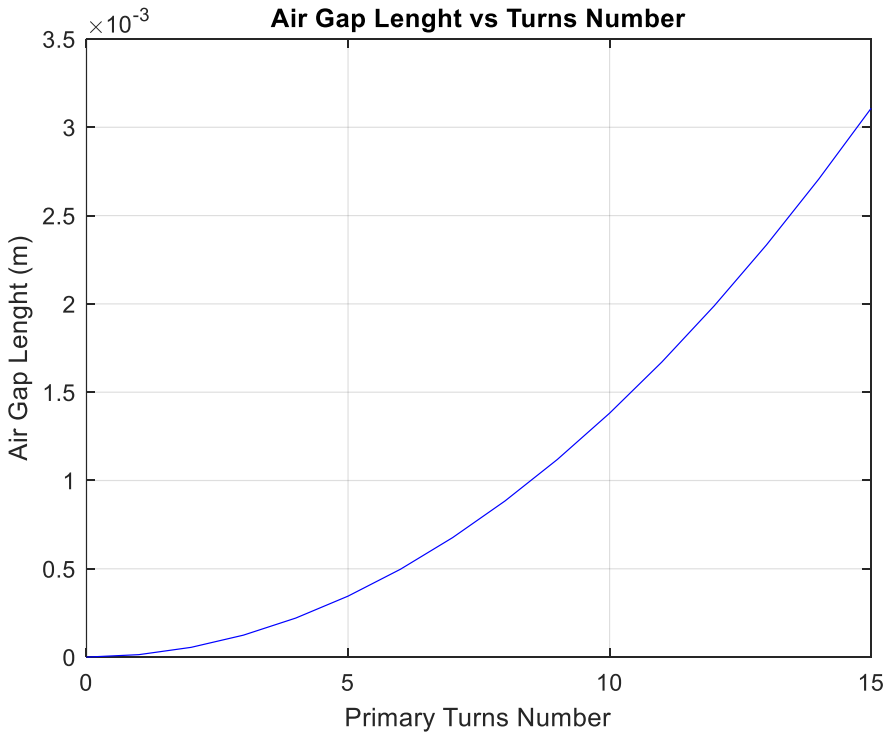


Figure 7 Air Gap Length vs Primary Turns Number

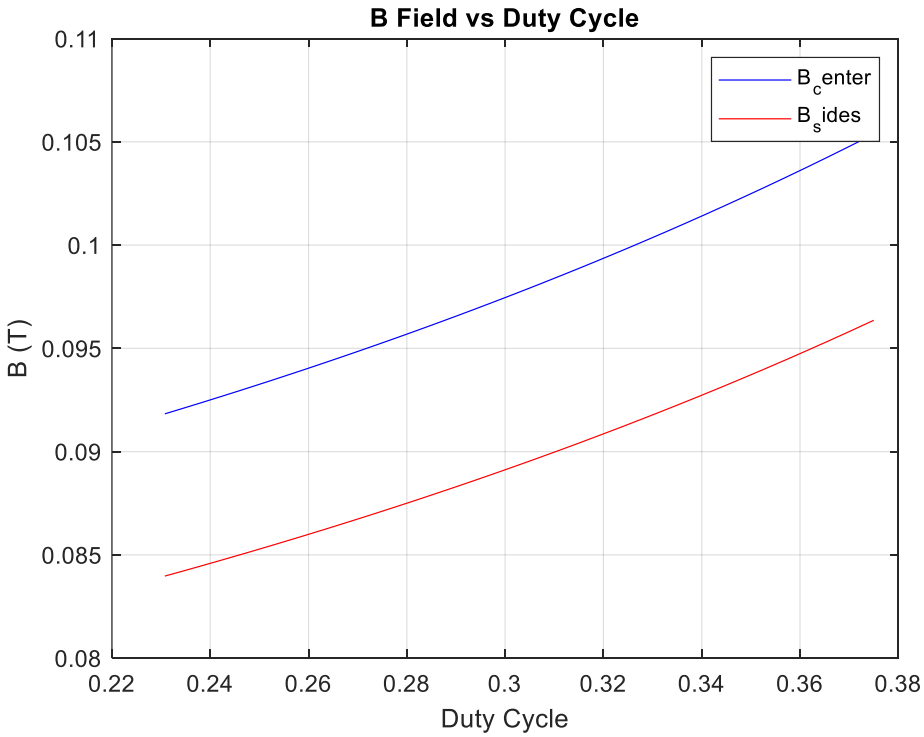


Figure 8 Field vs Duty Cycle

Now we need to choose an AWG cable for primary and secondary. First, the skin depth is calculated for the switching frequency which is 100 kHz.

$$\delta = \sqrt{\frac{\rho_{Cu}}{\mu_0 \pi f_s}} = \sqrt{\frac{1.724\ 10^{-8}}{\mu_0 \pi\ 90\ 10^3}} = 0.21\ mm$$

$$A_{strand} = \pi\delta^2 = 0.1372\ mm^2$$

The copper area must be equal or smaller than the strand area. A litz wire found in the laboratory with AWG 28 is used whose strand section is 0.08 mm^2.

Now we need to find how many cables to parallel in order to carry primary and secondary currents. Thereby, the rms value of the primary and the secondary currents are calculated. RMS value for an inductor current given in Figure 9 can be calculated as follows.

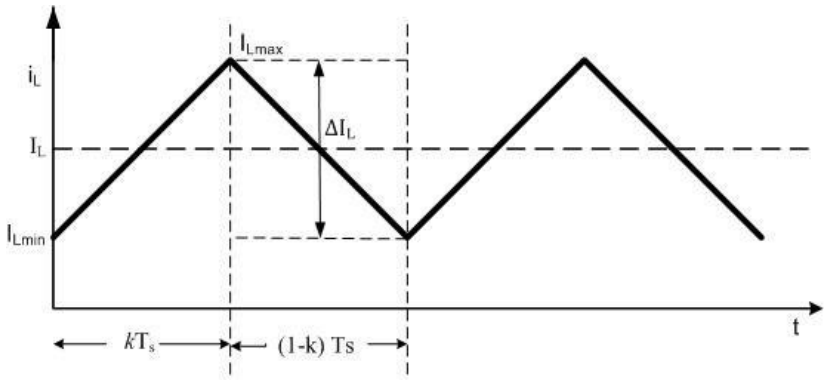


Figure 9 Typical Inductor Current

$$I_{L,rms} = \sqrt{I_L^2 + \frac{\Delta I_L^2}{12}}$$

According to this formulation rms primary current vs input voltage is plotted in Figure 10. From Figure 10 it can be seen that the rms primary and secondary currents reach their maximum value of 11.5 A at minimum input voltage.

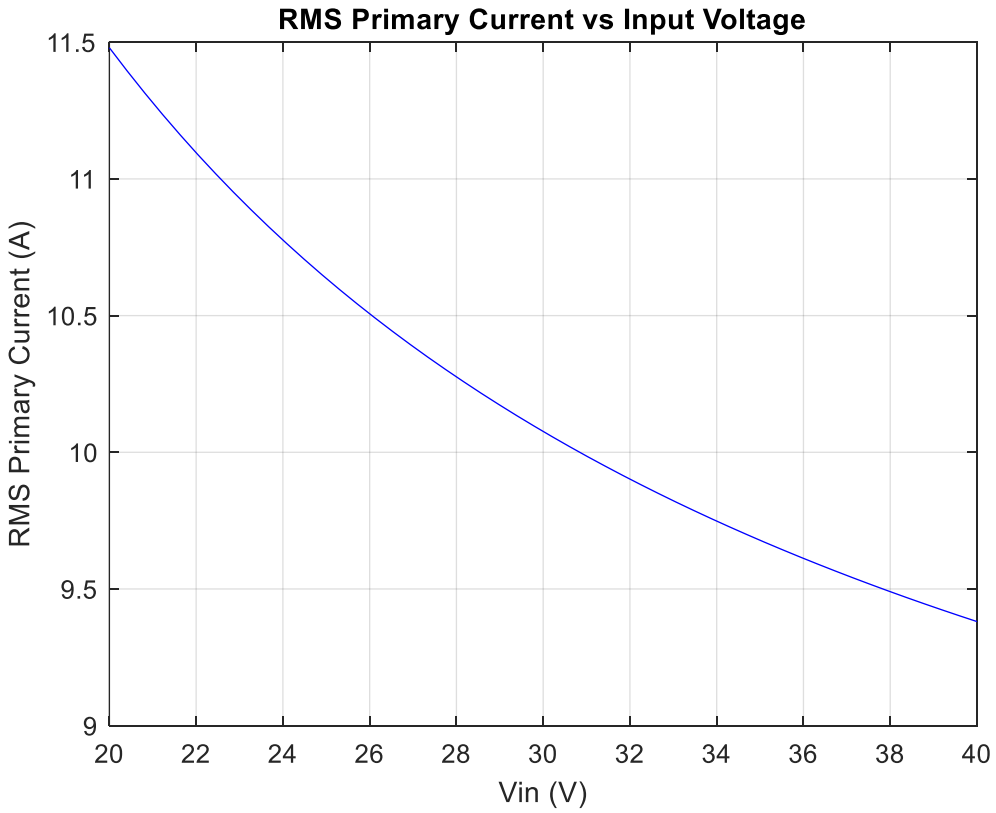


Figure 10 RMS Primary Current vs Input Voltage

The current density is chosen as 3.5 A/mm^2.

$$\#parallel\ cables = nearest\ integer\left(\frac{I_{rms\ max}}{J\ A_{strand,AWG28}}\right)$$

For primary and secondary the number of parallel cables is calculated as 41. There are more than 50 parallels in the litz wire found in the laboratory. Since the total number of wires cannot be counted for fill factor calculation it is taken as 70 and for loss calculation it will be taken as 50. Henceforth, worst case scnerio will be assessed. The area of an AWG28 cable is 0.08 mm^2. Total cable area can be calculated as follows.

$$A_{Cable} = A_{AWG26}(N_1\ \#primary\ parallel\ cables + \ N_2\ \#secondary\ parallel\ cables)$$

$$A_{Cable} = 67.2\ mm^2$$

The window area of the core is calculated from its dimensions as 375 mm^2.

$$Fill\ Factor = \frac{A_{Cable}}{A_{window}} = 0.1789$$

The fill factor is acceptable up to 0.3 to 0.4. Although our choice might seem like an overdesign, increasing the fill factor will complicate the wounding process. Thereby, the leakage inductance might be increased due to a poor wounding process.

Since the radius of the conductor is chosen smaller than the skin depth both AC resistance is quite the same as the DC resistance. This is verified by a website that measures the AC resistance of a specified cable [1]. The mean length turn of the core is calculated from the geometry in order to find the length of the wounded cable. Also, a safety factor of 1.5 is taken due to the cable thickness. This mean length turn is multiplied by the turns number to find the total length of the cables.

$$R_{primary} = \rho \frac{l}{A} = 3.7\ m\Omega$$

$$R_{secondary} = R_{primary} = 3.7\ m\Omega$$

Maximum copper losses can be calculated from the maximum rms current which is found as 11.5 A for primary and secondary.

$$P_{copper,primary} = I^2_{primary\ rms} R_{primary} = 0.4914\ W$$

$$P_{copper,secondary} = I^2_{secondary\ rms} R_{secondary} = 0.4914\ W$$

$$P_{copper} = P_{copper,primary} + P_{copper,secondary} = 0.983\ W$$

For core losses an excel file is obtained for ferrite materials from [2]. In this Excel file, Steinmetz coefficients are available. Steinmetz equation and coefficients for the R type material are given below.

$$P_{CL} = \frac{a\, f^x B^y L(T)}{100}\ mW/cm^3$$

$$L(T) = b - cT + dT^2$$

Material	Frequency Range	a	x	y	b	c	d	P_{CL}
								(mW/cm3)
R Material	20kHz-150kHz	3.53	1.420	2.880	1.970000000	0.022260000	0.0001250000	3.35
	150kHz-400kHz	5.88E-04	2.120	2.700	2.160000000	0.023270000	0.0001170000	

Figure 11 Steinmetz Coefficients for R Material

For maximum core loss, the maximum peak to peak ripple flux density which is 0.036 mT has been chosen. For operating temperature and frequency, 60°C and 100kHz are chosen respectively. Core loss density is calculated as 3.35 mW/cm^3 for this operation condition. To find the core loss the core loss density is multiplied by twice the volume of the core (volume of the core is 208 cm^3). Since two EC cores are used. Total core loss is found to be 0.364 WSince we operate at high

frequencies this is expected. In order to use in unideal modelling of the converter R_{core} can be found as follows.

$$R_{core} = \frac{V_{out}^2}{P_{core}} (\frac{N_1}{N_2})^2 = 49.8\ \Omega$$

After wounding the transformer LCR meter is used to calculate the leakage and magnetizing inductance. Since the LCR meter is not reliable for resistance calculations, to calculate the resistance windings are connected to the power supply and the maximum current is set to 5A. Then the voltage across the windings is measured by the multimeter and resistance is calculated from the Ohms Law. Supplied voltage is not used since the resistance of the cables that are used to connect the power supply and transformer is comparable with the winding resistance. For both windings voltage is measured as 0.023 V when 5A is supplied by the DC power supply. This means the resistance of the primary and secondary windings is 4.6 mΩ which is close to our calculations.

To understand the logic of the measurement technique of the leakage and magnetizing inductance equivalent model of the transformer given in Figure 12 is investigated. First, the secondary side is left open circuited. The measurement gives us the sum of primary leakage inductance and magnetizing inductance. Nevertheless, the measurement can be taken as magnetizing inductance since leakage inductance is much smaller than the magnetizing inductance. Magnetizing inductance is measured as 21.97 µH. For leakage inductance calculation, the secondary is kept short circuited, and inductance is measured. This measurement corresponds to primary leakage inductance plus secondary leakage paralleled magnetizing inductance. Since leakage inductance is much smaller than the magnetizing inductance, secondary leakage paralleled magnetizing inductance can be approximated as secondary leakage inductance. Thus, measured inductance 0.24 µH is the sum of primary and secondary leakage inductances. Since the turns ratio is 1, we can assume that leakage inductances are equal. This will yield primary and secondary leakage to be 0.12 µH. Measurements for open and short circuited secondary are given in Figure 13 and 14 respectively.

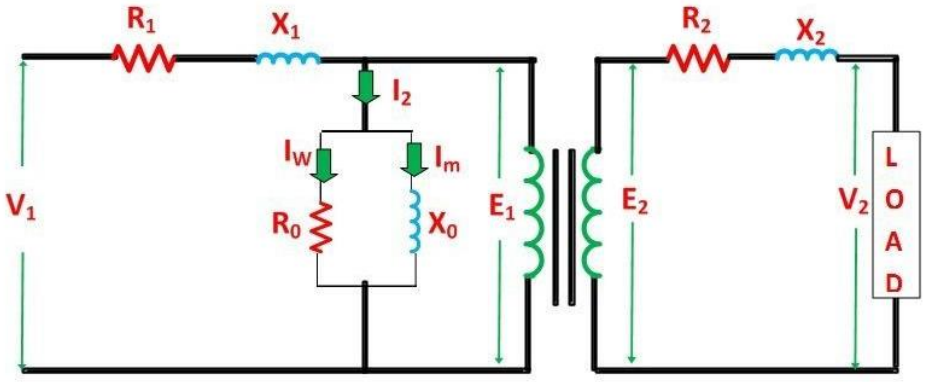


Figure 12 Equivalent Circuit of the Transformer

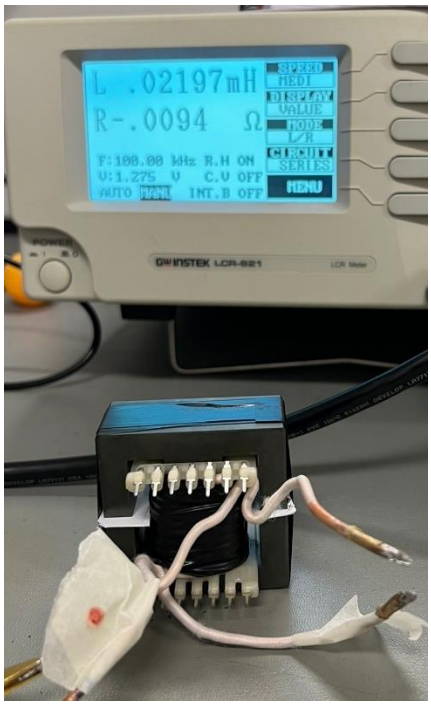


Figure 13 Open Circuit Measurements

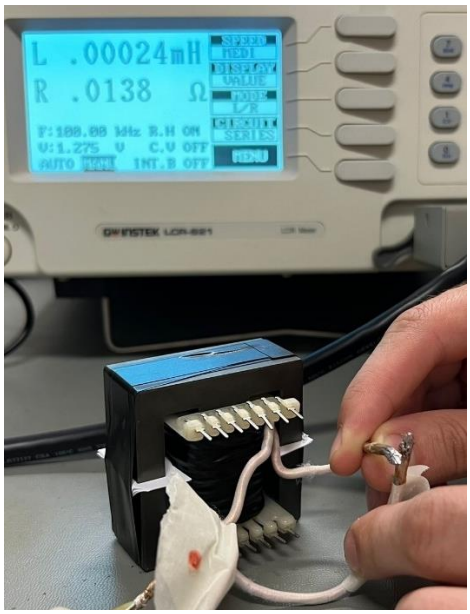


Figure 14 Short Circuit Measurements

Controller Design

UC3843 is selected for output voltage control since it is commonly used for voltage control of DC/DC converters. UC3843 has peak current and voltage control features which are both used at our design. Moreover, UC3843 can provide up to full duty. For simulations LTSpice counterpart of the UC3843 which is LT1243, is used. The basic schematic of the controller network is given in Figure 15.

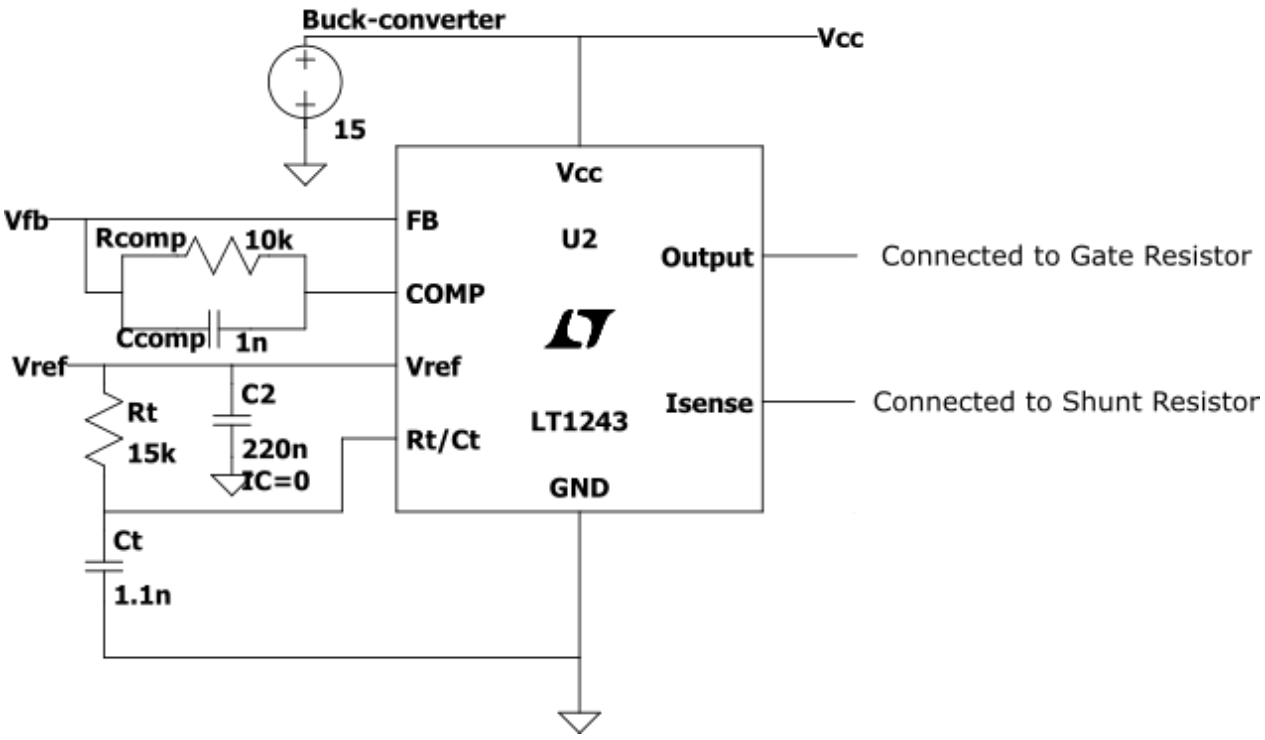


Figure 15 Controller Network

According to the datasheet of UC3843 [3] supply voltage of the controller must be between 8V to 30V. Since input voltage is between 20V to 40V the input cannot be directly used to feed it. Hence, a controlled buck converter with 10V to 40V rated input capability is used for this purpose. The controller gives gate signals at the output pin and 5V output at V_{ref} terminal. The remaining parts of the controller are explained below.

R_t/C_t Oscillator: R_t/C_t oscillator generates the sawtooth signal that is used for generating the switching signal. Frequency of the R_t/C_t oscillator sets the CCM mode switching frequency. The formula for the R_t/C_t oscillator frequency is as follows:

$$f_{osc} = \frac{1.72}{R_t\, C_t}$$

R_t and C_t are chosen 15 kΩ and 1.1 nF respectively. This will yield switching frequency to be equal to 104 kHz.

Voltage Feedback Network: Controller sets the duty of the gate signals according to the voltage error generated by the internal error amplifier. This error amplifier is a basic subtracter designed with an op amp whose inputs are internally generated 2.5V and voltage at V_{fb} pin. To set output voltage optocoupler network given in Figure 16 is used.

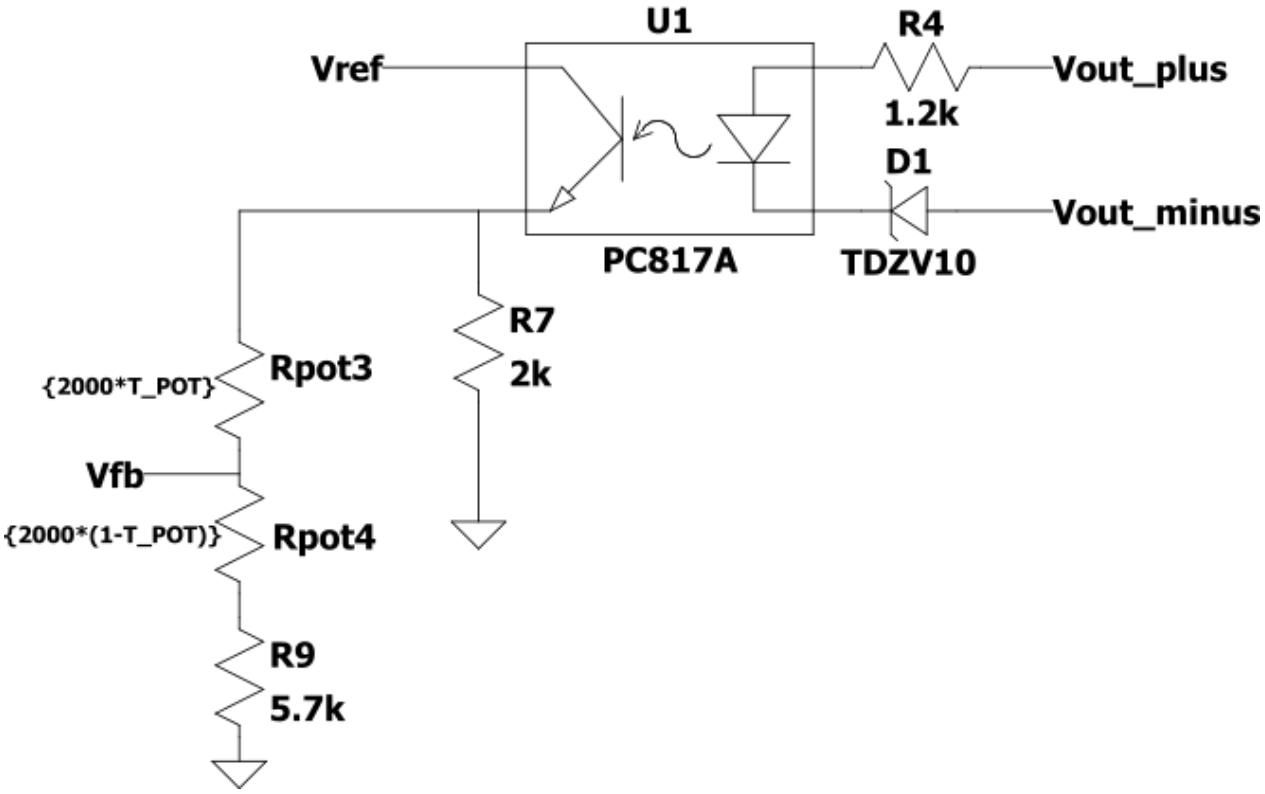


Figure 16 Optocoupler Network

The current transfer ratio of the PC817A optocoupler is very close to 1. Furhermore, resistance of the branch with potentiometer is relatively higher than 2 kΩ. Therefore, it can be assumed that current on the 2 kΩ branch is same as the 1.2 kΩ resistor. The branch with potentiometer enables us to set the output voltage reference to a value between 12.2 V to 13.1 Volt.

At steady state average voltage of the V_{fb} must be 2.5 Volts so that the output of the error amplifier will be zero and keep the duty constant. T_{pot} indicates the percentage of the potentiometer. According to this definition voltage and current of the 2 kΩ resistor can be found as follows.

$$V_{2k\Omega} = \frac{2\,T_{pot}}{5.7 + 2\,(1 - T_{pot})} V$$

$$I_{2k\Omega} = I_{1.2k\Omega} = \frac{2\,T_{pot}}{2\left[2.7 + 2\,(1 - T_{pot})\right]} mA$$

The voltage on the 1.2 kΩ resistor can be expressed as follows.

$$V_{2k\Omega} = 1.2\ \frac{2\ T_{pot}}{2\left[2.7 + 2\ (1 - T_{pot})\right]} V$$

The output voltage can be expressed as follows.

$$V_{out} = V_{2k\Omega} + V_{opto\ diode} + V_{zener} = \left(11 + 1.2\ \frac{2\ T_{pot}}{2\left[2.7 + 2\ (1 - T_{pot})\right]}\right) V$$

From the output voltage expression it can be seen that output voltage can be set to the desired value with potentiometer. The zener diode is used to apply full duty until output voltage reaches 11V which will increase the transient speed of the converter.

Compensator: 10 kΩ resistance and 1 nF capacitor are paralelled between V_{ref} and Compensator pins of the UC3843 as shown in Figure 15. This adds a zero to the system which increase the phase margin and advance transient response.

Peak Current Conrtol: UC3843 controller has a current sense pin to limit the maximum switch current. Limiting the maximum switch current, which is also the transformer current, will enable to set the maximum power that will be transferred to the secondary. Also, it can be used for safety and preventing core saturation. UC3843 cuts the PWM output when the voltage of the current sense pin is 1V. Therefore, the sense resistor placed under the switch must be selected so that it will have 1V voltage drop when limiting current pass through it. In the magnetic design section the maximum primary transformer current is determined as 13.3 A. However, parasitic resistors series with the sense resistor will change the current sense pin since the resistance of the sense resistor is quite low. In addition to this the efficiency is approximated as 70% in magnetic design section. If the resultant efficiency is lower than the anticipated efficiency, the core will not be able to transfer the rated power. Therefore, the maximum current is chosen as 18A. The selected mosfet can carry 35A at 100 °C and the core remains unsaturated at 18 A (0.18 T). 18 A will result in 1V drop for 55mΩ. For sense resistor four 15 mΩ resistors are connected in series.

Simulation Results

The circuit that is simulated in LTspice can be found in Fig. 17.

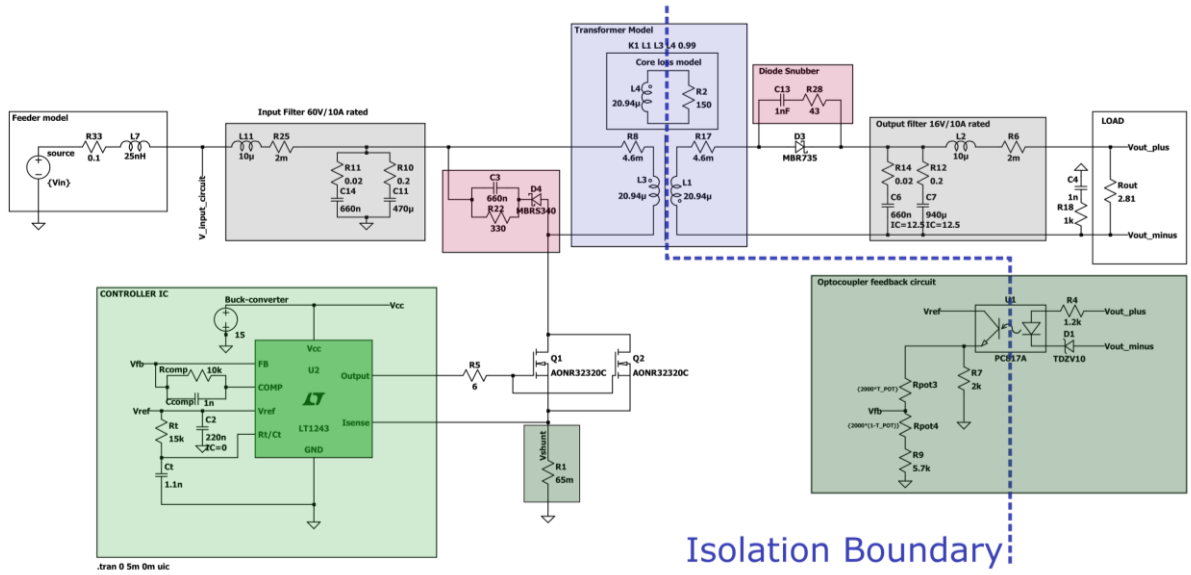


Figure 17 Simulated Circuit

The simulation was conducted using input voltages of 20, 25, 30, 35, and 40 volts, along with a set output voltage reference of 13V. The results show that our circuit achieves an efficiency of approximately 75-80% when implemented practically. The distribution of the input power averaging all results is shown in Fig 18. Detailed simulation results are shown in the Table 1.

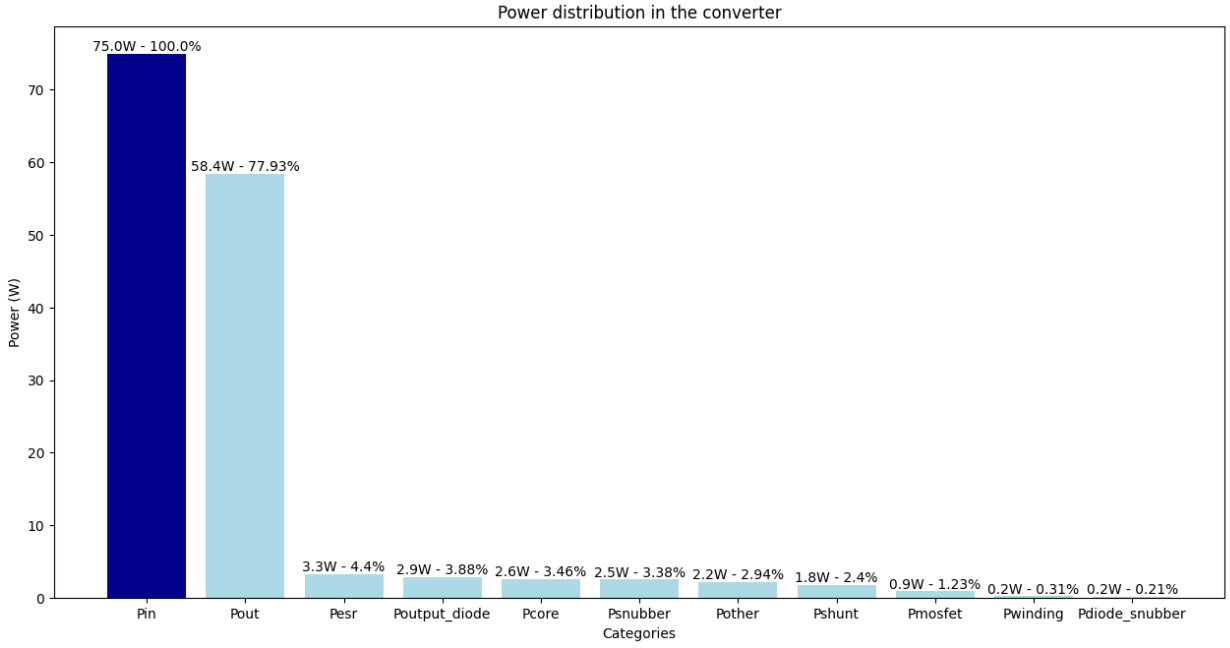


Figure 18 Power distribution in the converter

Vin	Vset	Efficiency	Duty	Iin-mean	Iout-mean	Pin(w)	Pout(w)	Psnubber	Pdiode_snubber	Pmosfet	Pcore	Pwinding	Psnubber_diode	Vds	Vout_ripple	pdiode_rect	Pshunt	Pesr
20.0	13.0	71.2	46.0	3.9	4.6	80.2	57.1	3.0	0.1	0.9	1.7	0.3	0.6	53.0	0.5	3.0	2.2	5.3
25.0	13.0	77.6	41.0	3.0	4.6	74.8	58.1	2.6	0.1	0.9	2.2	0.3	0.6	56.0	0.4	2.9	1.6	4.2
30.0	13.0	80.1	35.0	2.4	4.6	73.6	59.0	2.5	0.2	0.9	2.6	0.2	0.5	60.0	0.4	2.9	1.2	3.5
35.0	13.0	80.5	31.0	2.1	4.6	73.2	59.0	2.3	0.2	0.9	3.0	0.2	0.5	63.8	0.4	2.9	3.0	1.0
40.0	13.0	80.8	28.0	1.8	4.6	73.0	59.0	2.3	0.2	1.0	3.5	0.3	0.4	68.0	0.3	2.8	0.8	2.7
Mean Values		**78.06**	NA	**2.64**	**4.58**	**74.95**	**58.41**	**2.53**	**0.16**	**0.92**	**2.59**	**0.23**	**0.52**	**60.15**	**0.40**	**2.91**	**1.8**	**3.3**

Table 1 Detailed Simulation Results

Component Selection

According to the waveforms, shown in the Simulation part, we have decided on the important components. The core selection was justified in the Magnetic Design part; thus, there will not be any information about the magnetic core in this section.

- **MOSFET:** IRFU3710ZPbF [4]
  As shown in the Simulation section, the MOSFET has a peak voltage level of around 70V, due to ringing, which means the MOSFET should endure a voltage stress much higher than the input voltage. Moreover, this value is changing according to the designed snubber which is not finalized in this project for the time being. To account for all of this, a relatively high safety margin must be considered while choosing a MOSFET. IRFU3710ZPbF can bear 100V and 39A while having an 18mΩ which is quite good for our design; thus, we have chosen this MOSFET.

- **IC:** UC3843B [5]
  UC3843B is a current-mode PWM controller. It has a low start-up current (< 0.5 mA), which is advantageous for the flyback converter. It can operate up to 500kHz and can provide up to a full-duty cycle. Moreover, it is selected since its usage in isolated power converters is highly known and a high number of sources can be found on its driving circuitry.

- **Diode:** DSA30C100PB [6]
  While the design includes 4 diodes, three Schottky and one Zener, the most important ones are the one at the secondary winding side and the one at the snubber. The snubber diode has a peak voltage of 70V, just like the MOSFET. However, it has a lower forward current than the MOSFET with a 7A peak. The chosen diode can withstand 100V and it has an I_F rating of 15A. The voltage drop in the conduction is 0.73V which is one of the lowest values we could find; thus, we have chosen this diode since efficiency is one of the main concerns in this project. Also, since both diodes have similar waveforms, we will be using this for both of the diodes.

- **Optocoupler:** PC817X [7]
  We have chosen a single channel optocoupler since we need only one channel and cost can increase with the increasing number of channels. Moreover, we have chosen this optocoupler since it is easy to find and economically feasible.

- **Output Capacitor:** PKLH-016V471MG125 [8]
  We have chosen this one as the output capacitor. It is an Aluminum Electrolytic Capacitor with a voltage rating of 16V. While only one of them is 470μF, we will parallel four of them to reduce ESR while having the wanted capacitance rating at the output side.

Aside from the components mentioned above, various resistors and capacitors will be used.

Test Results

When we implemented the circuit we simulated, we saw that under full load at 20V input condition, the MOSFET can heat up to 110℃ under ten seconds. As a precaution, we have added a cooling fan to the circuit. Moreover, to drive the fan and supply the controller, we have used a 15V out buck converter that can easily operate at 40V input voltage. After implementing the fan, we observed that despite cooling via a fan, the MOSFET still heats up to 100℃ after some run time. To solve the heating of the MOSFET, we have added a second MOSFET in parallel to the first one. While paralleling MOSFETs is not considered as a good practice, by paralleling we have successfully reduced the current in a MOSFET to half of its original value and the MOSFET heats stabilized around 50-60℃. After finalizing the circuit, we have moved to conduct the tests. In Figure 18 finalized converter picture is given.

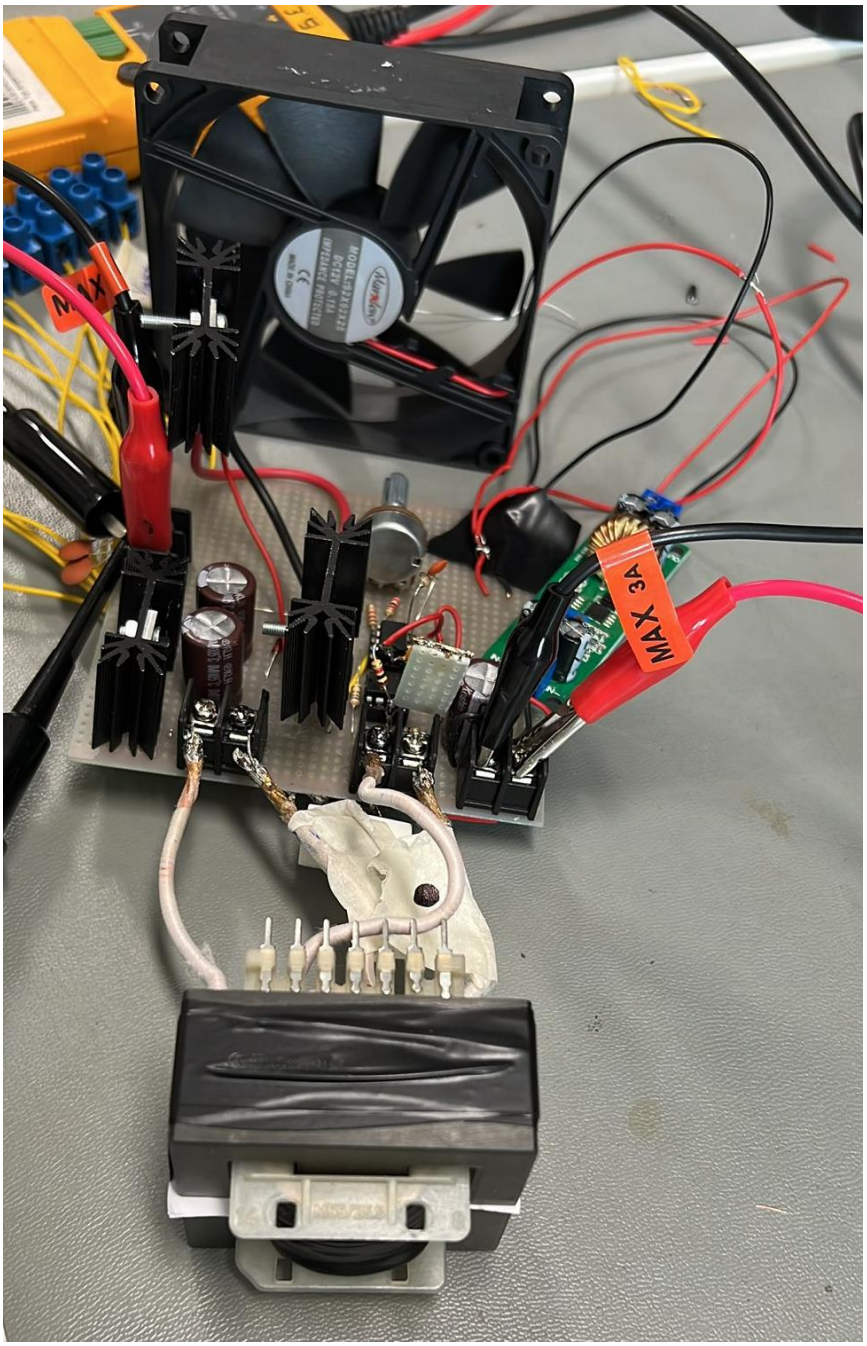


Figure 18 Finalized and implemented design

The converter displays different characteristics at different input voltage and loading conditions; thus, a comprehensive analysis is needed. The first analysis we made was to compare output voltage, input power, temperatures, line regulation and efficiency for different loading conditions. In Table 2**,** you can see the converter data gathered from the initial test.

P_{out}(W)	V_{in}(V)	V_{ref}(V)	V_{out}(V)	P_{in}(W)	T_{max} (°C)	T_{MOSFET} (°C)	Regulation	Efficiency (%)
0	30	12.5	12.5	3.6	30	26	0%	0
6	20	12.5	12.46	12.5	32	26	0.32%	48
6	30	12.5	12.48	13.1	35	28	0.16%	45.8
6	40	12.5	12.5	13.5	32	27	0%	44.4
30	20	12.5	12.4	46.2	40	33	0.8%	64.9
30	30	12.5	12.4	47.2	50	35	0.8%	63.6
30	40	12.5	12.5	49.5	52	37	0%	60.6
45	20	12.5	12.3	77	67	55	1.6%	58.4
45	30	12.5	12.4	69.5	60.3	45	0.8%	64.7
45	40	12.5	12.4	75.5	57	40	0.8%	59.6
60	20	12.5	12.2	99	95	70	2.4%	60.6
60	30	12.5	12.2	95.1	67.2	57	2.4%	63.1
60	40	12.5	12.2	92.3	67	55	2.4%	65

Table 2 Gathered power, voltage and temperature data of the converter

As can be seen from the above table, the optimum operating condition of the converter is at the rated load while the input is 40V. Moreover, we can see that the voltage regulation of the converter is inside the specified region for all the operating conditions. While the peak efficiency was reached at rated load, line regulation is better at low output power conditions. Due to forced cooling, there is not any heat problem, as can be understood from the given temperature data.

From the given table, the following graphs that show the behavior of the converter can be deduced.

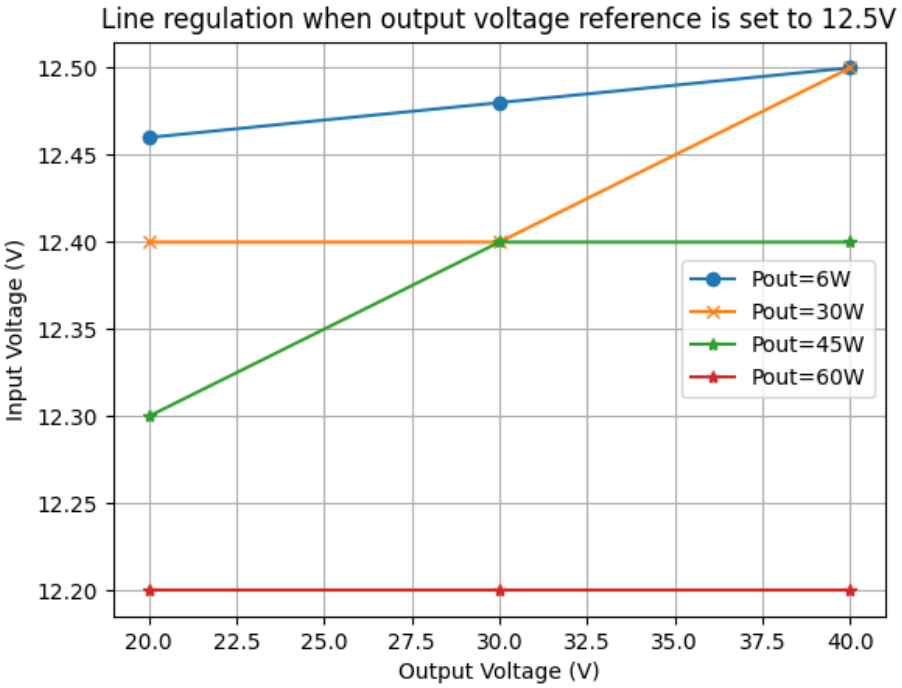


Figure 19 Line regulation at various output power

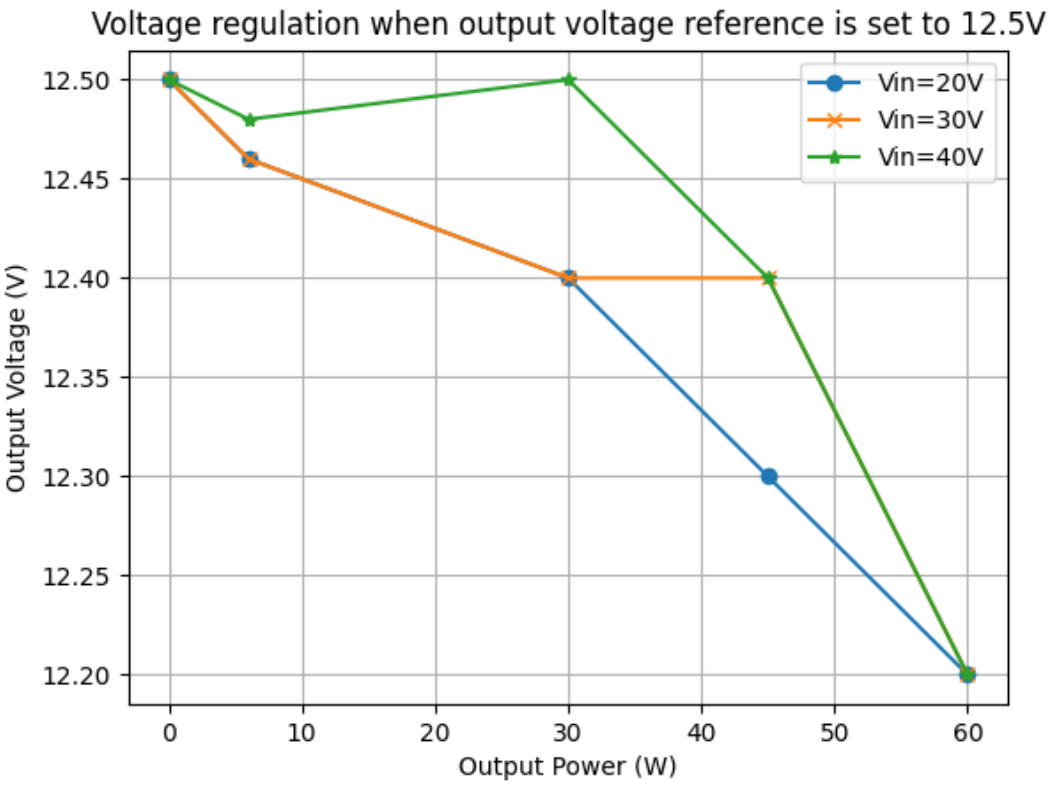


Figure 20 Load regulation

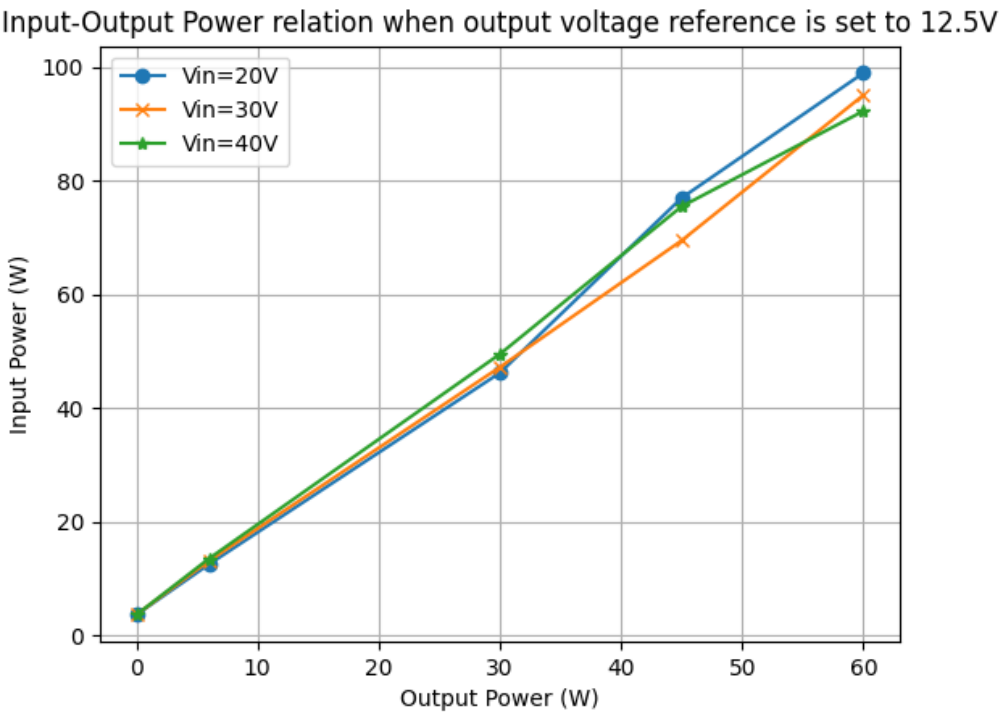


Figure 21 Input power to output power

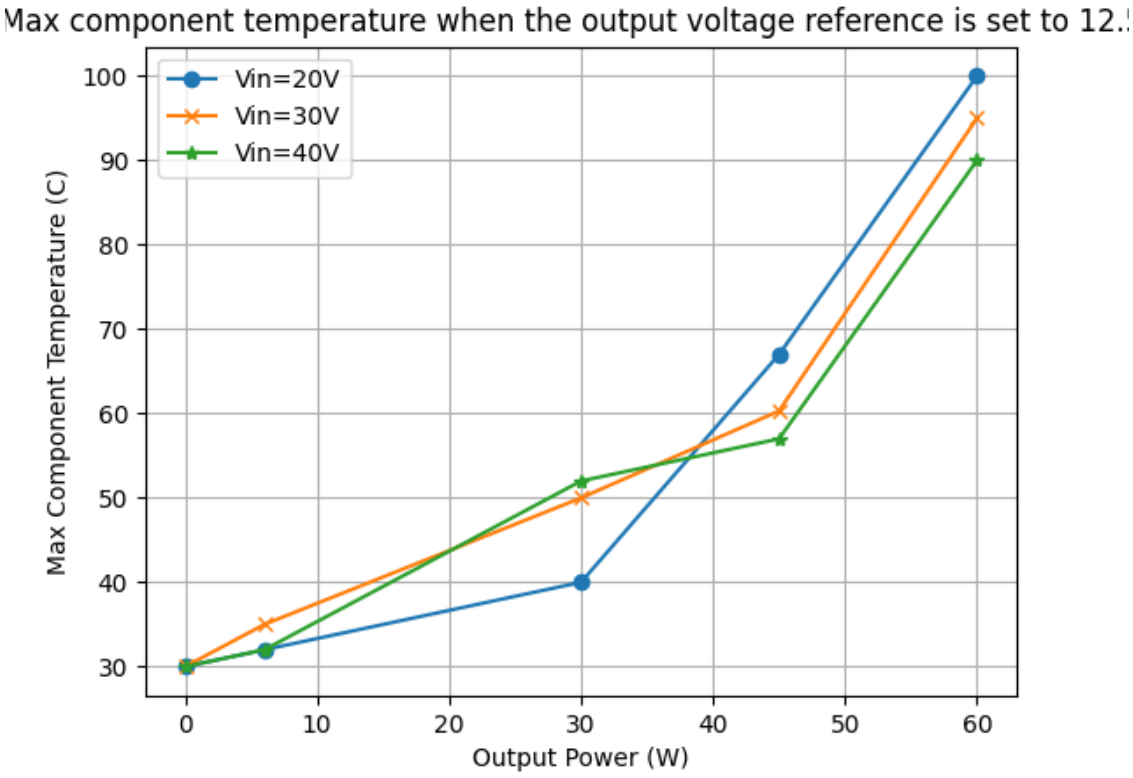


Figure 22 Maximum temperature inside the converter according to output power

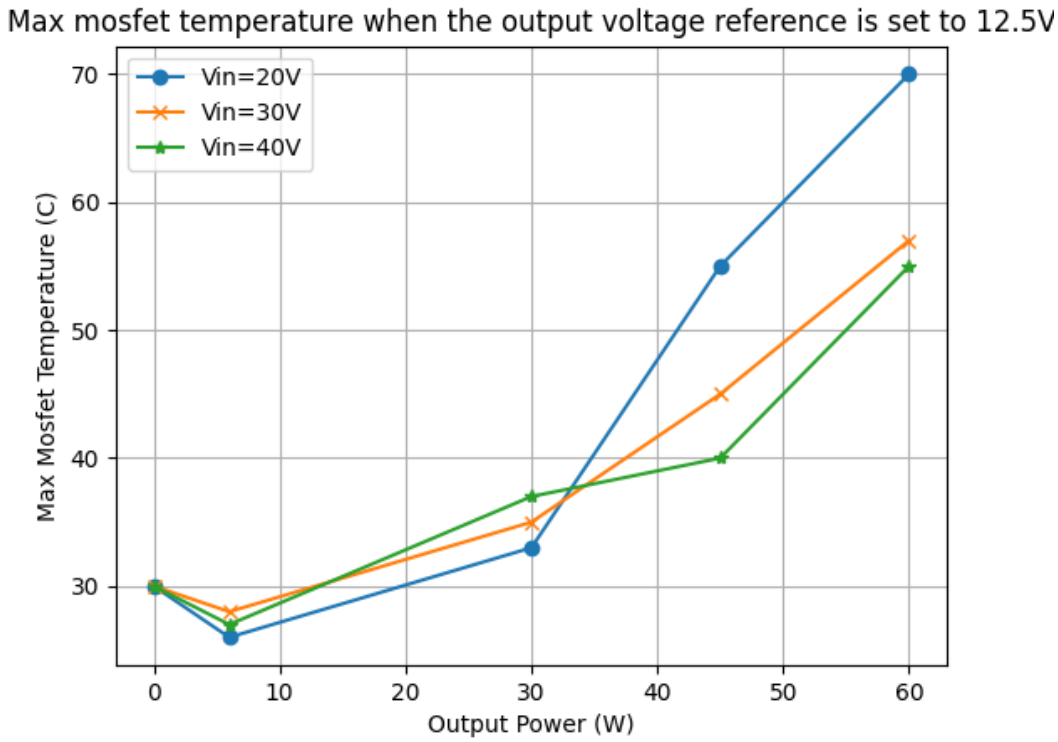


Figure 23 Maximum temperature of MOSFETs' according to output power

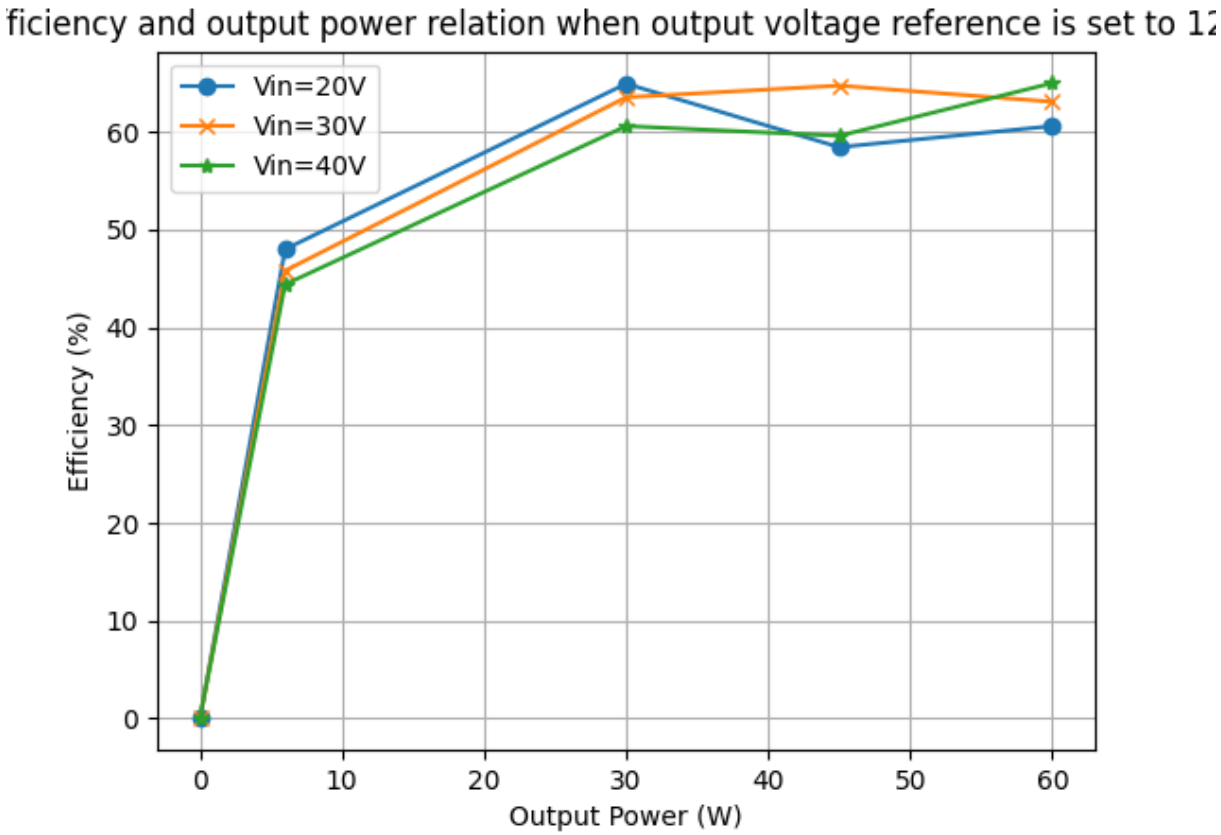


Figure 24 Efficiency according to output power

In Figure 19, the output voltage at different input voltages for various output powers is given. Figure 20 shows the output voltage to output power correlation for different input voltages. Figure 21 shows the linear behavior of the system and the input-output power relationship. The remaining figures give information about the component temperatures and efficiency. As can be observed, with the fan added, the component temperatures are kept at suitable levels. Moreover, it is obvious that after a certain point, 30W output power, the efficiency of the converter converges to approximately 66%.

While in the simulations the efficiency of the converter is around 80%, in reality, we have observed an efficiency of 66%. We have identified two main reasons for this efficiency discrepancy between the simulation and the hardware implementation. The first reason is the $R_{DS(ON)}$ difference. While in the datasheet of the IRFU3710ZPbF the $R_{DS(ON)}$ is given as 23mΩ, after some investigation, we believe that IRFU3710ZPbF has a much higher $R_{DS(ON)}$ value than the one given in the datasheet. The fact that the MOSFET heats up drastically without a parallel MOSFET and a fan supports the claim. Since it has a much higher resistance, the power drop on the MOSFET becomes higher than the simulated power drop since the current magnitude is similar in both the simulation and the tests. In the simulation, the power dissipated on the MOSFET is calculated as 2W; however, when we calculated the power dissipation on the MOSFET of the implemented circuit using oscilloscope waveforms, we have seen that it was approximately 7.6W. The second reason is the addition of the fan. As mentioned above, to keep the heat at manageable levels, we have added a cooling fan. The

fan draws 3W in steady-state operation, which reduces the efficiency where 60W is the rated power. In summary, the addition of a fan which is nonexistent in the simulation and the difference between the given $R_{DS(ON)}$ and real $R_{DS(ON)}$ values are the reasons for the reduced efficiency.

For a more comprehensive analysis, we have observed and recorded the waveforms.

No load waveform:

Figure 25 Waveform at no load

10% loading waveforms:

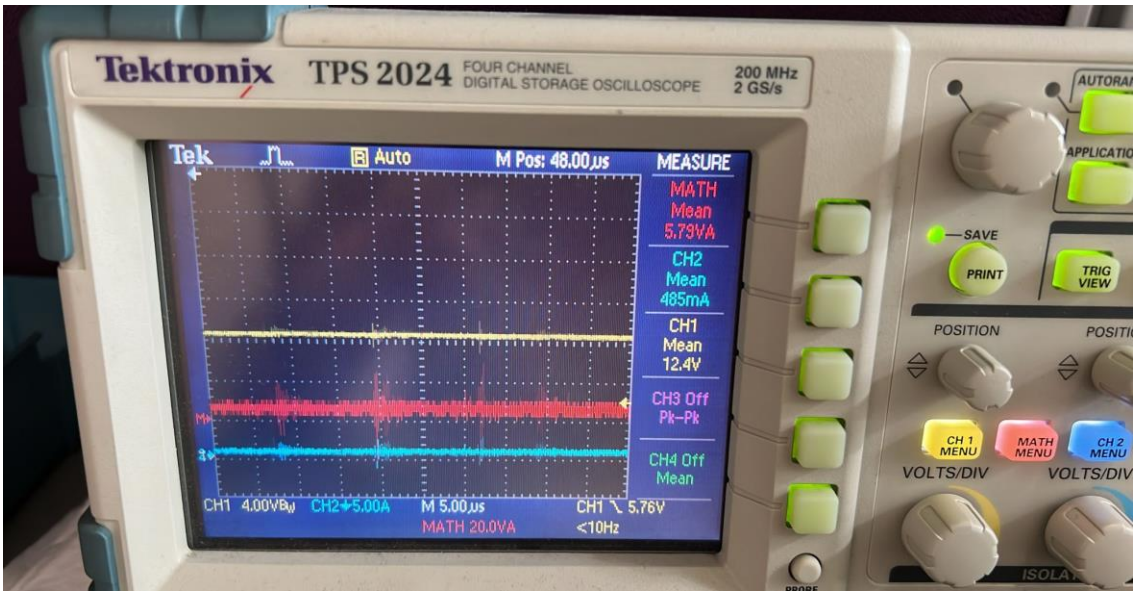


Figure 26 Ten percent loading at 20V input voltage waveforms

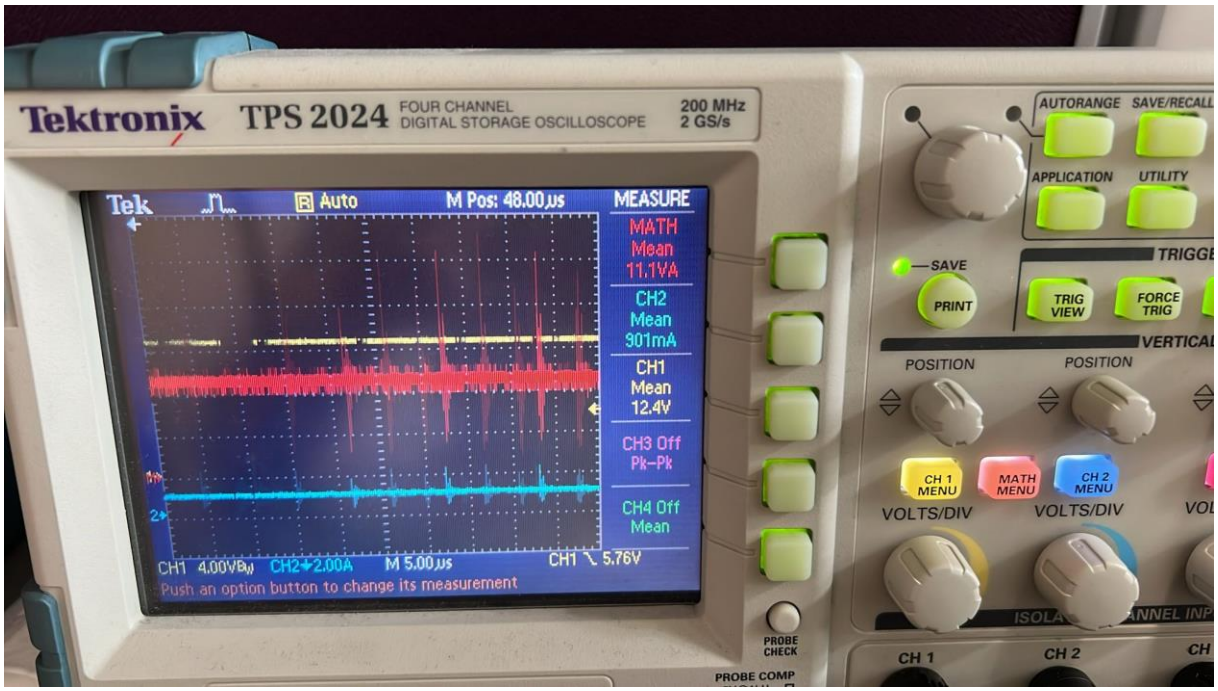


Figure 27 Ten percent loading at 40V input voltage waveform

50% loading waveforms:

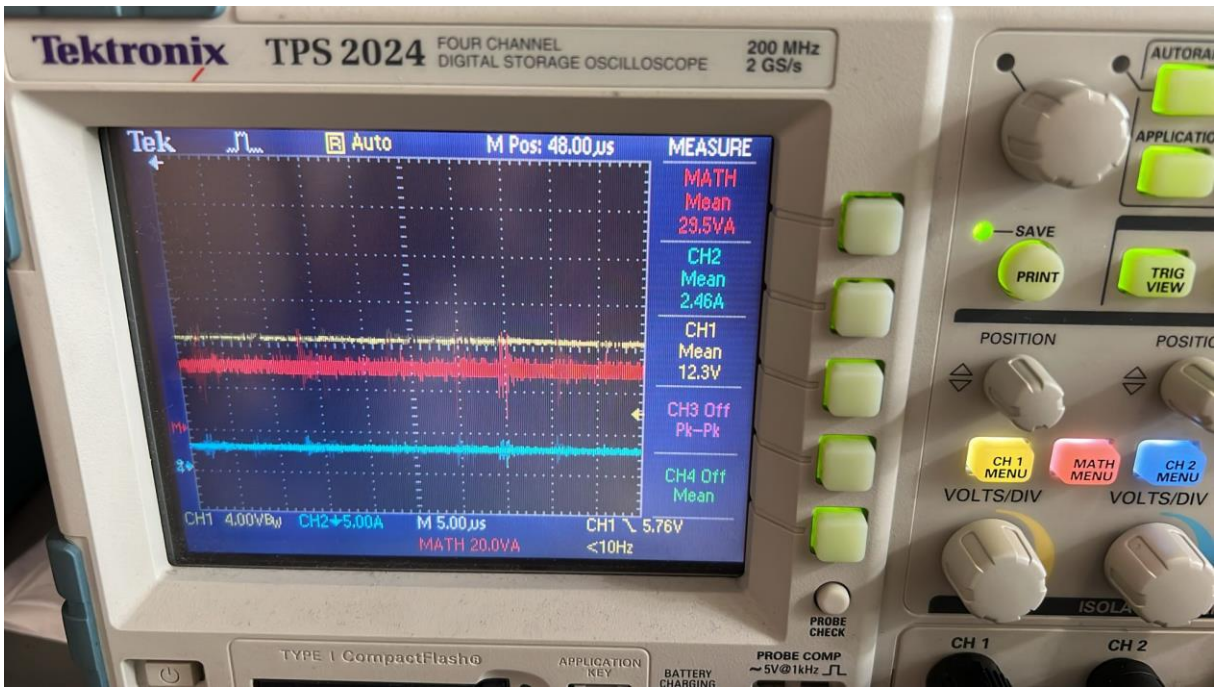


Figure 28 Half-rated loading at 20V input voltage waveform

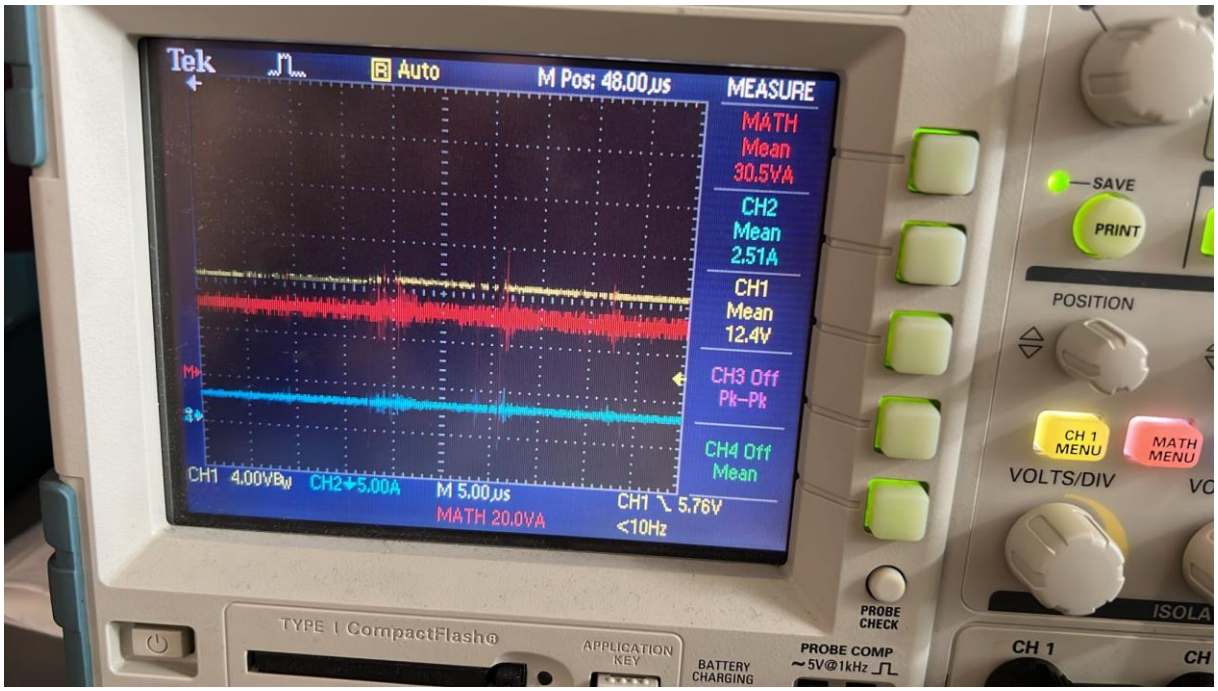


Figure 29 Half-rated loading at 40V input voltage waveform

Rated loading waveforms:

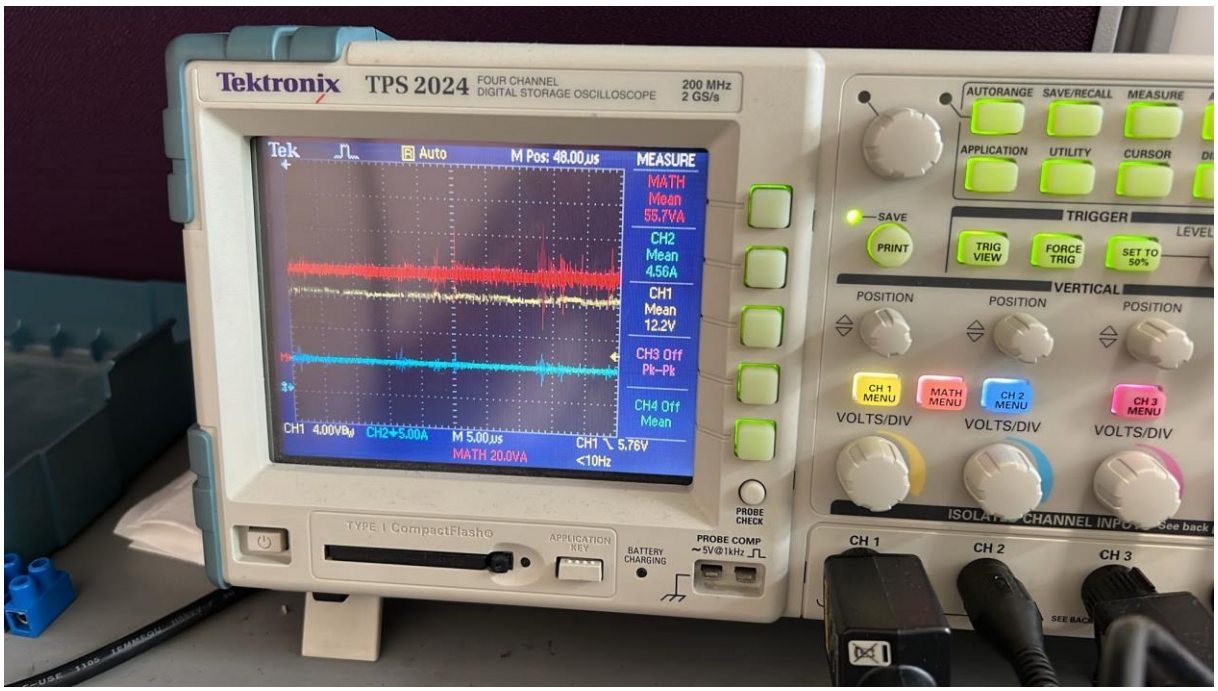


Figure 30 Rated loading at 20V input voltage waveform

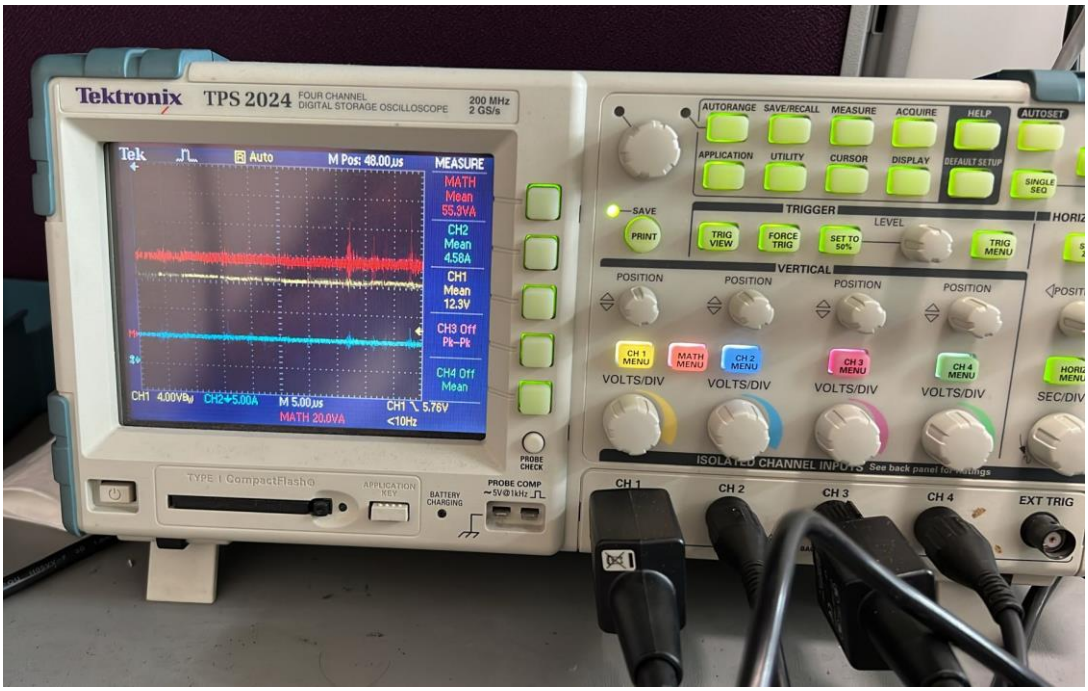
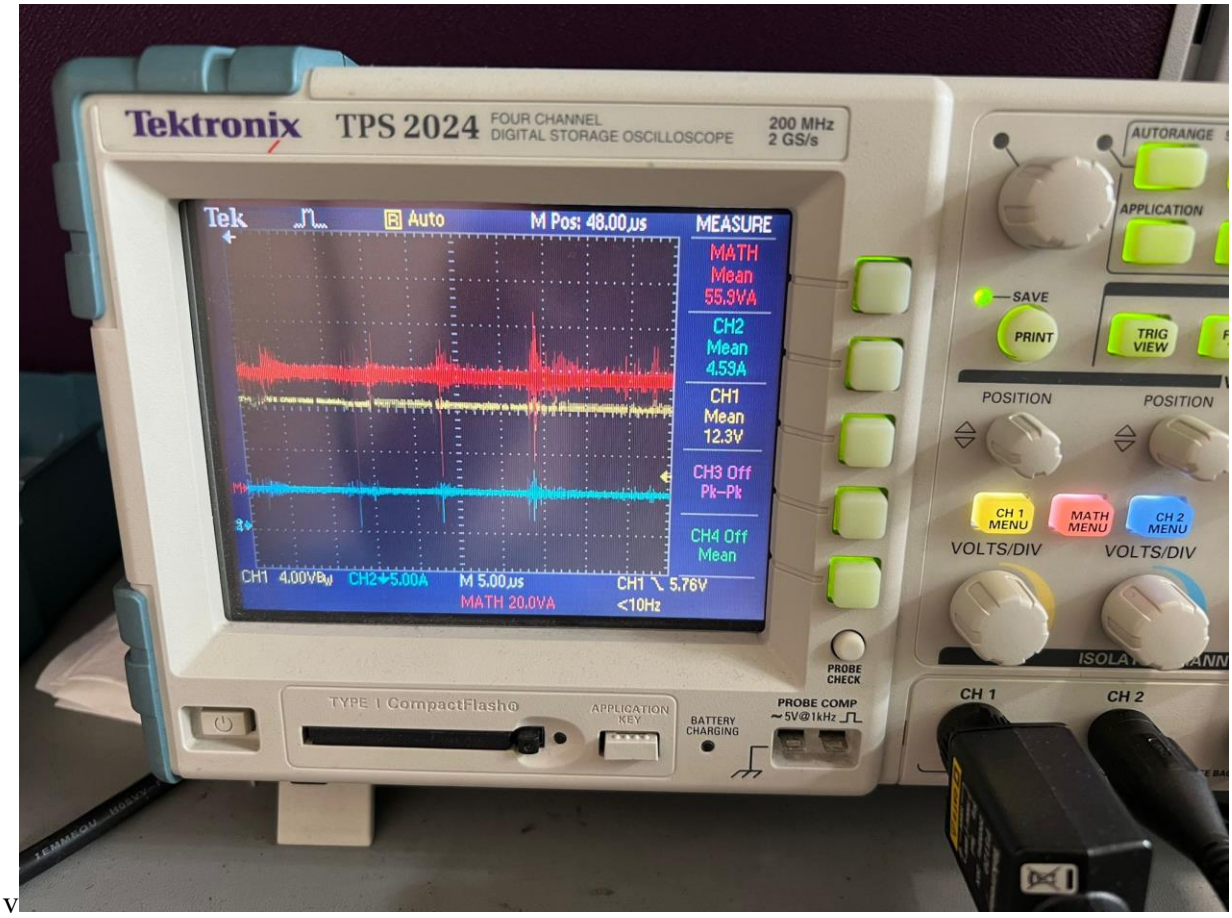


Figure 31 Rated loading at 30V input voltage waveform



V

Figure 32 . Rated loading at 40V input voltage waveforms

In Figures 24-27, it is seen that the converter can hold the voltage while supplying a below-rated output current. Moreover, it can be seen that output voltage decreases slightly as loading increases. The existence of spikes due to switching can be seen especially in CH2 waveforms; however, the spikes were not large enough to jeopardize the operation.

The full loading at 20V input is considered to be the most unsafe operation condition due to the highest current value; nevertheless, in Figure 28, it is seen that the converter can bear the current without a clear difference in the waveforms, which shows the capability of the converter.

After confirming and gathering data on the steady-state operation, the transient behaviors were investigated.

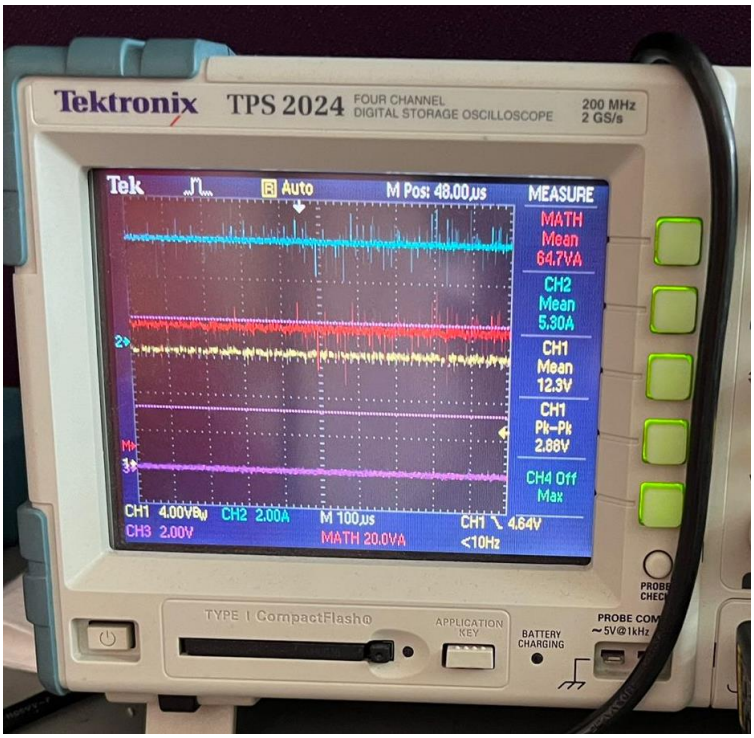


Figure 33 Full load start at 20V

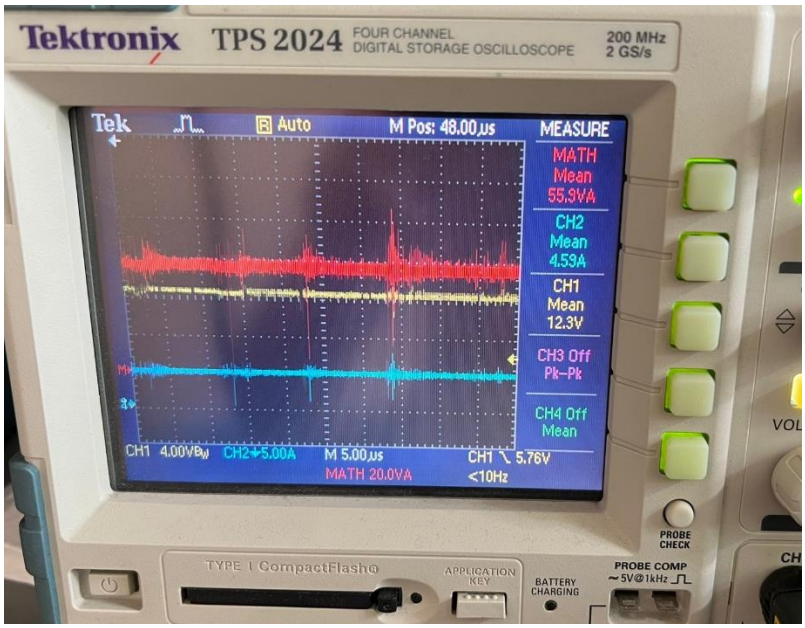


Figure 34 Full load start at 40V

In the above figures, the capability of full load start is shown. Despite drawing a larger current in the start-up than the steady state, the converter can tolerate the current and stabilize itself. However, a soft start is always preferred.

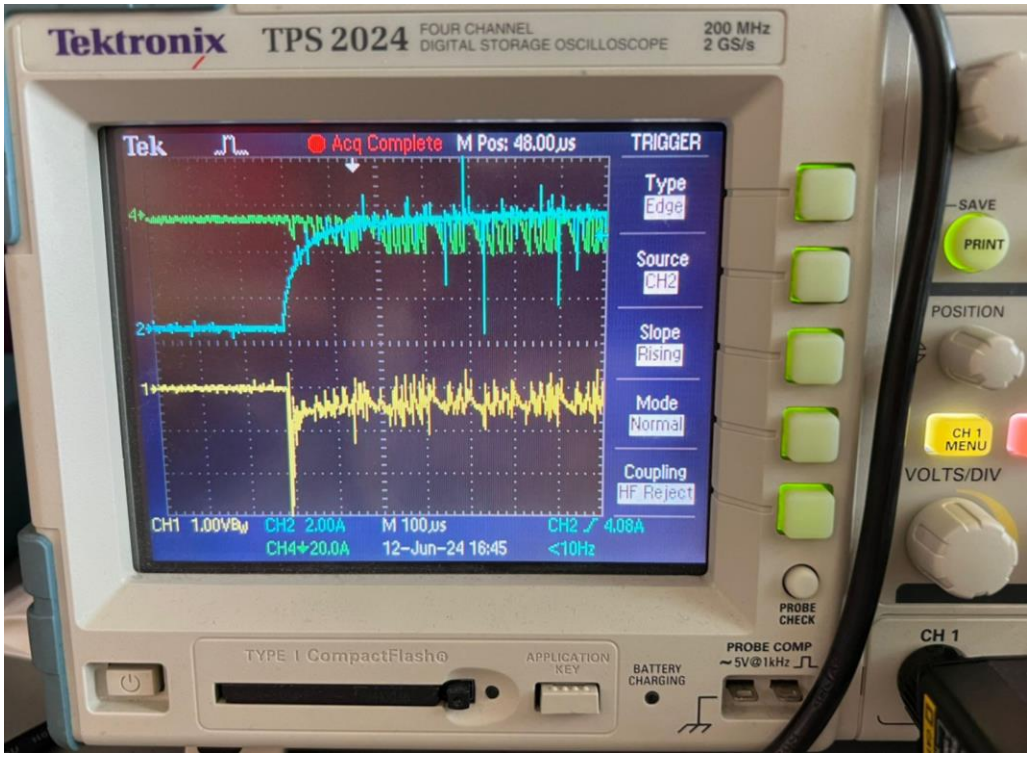


Figure 35 Load turn-on transient waveform

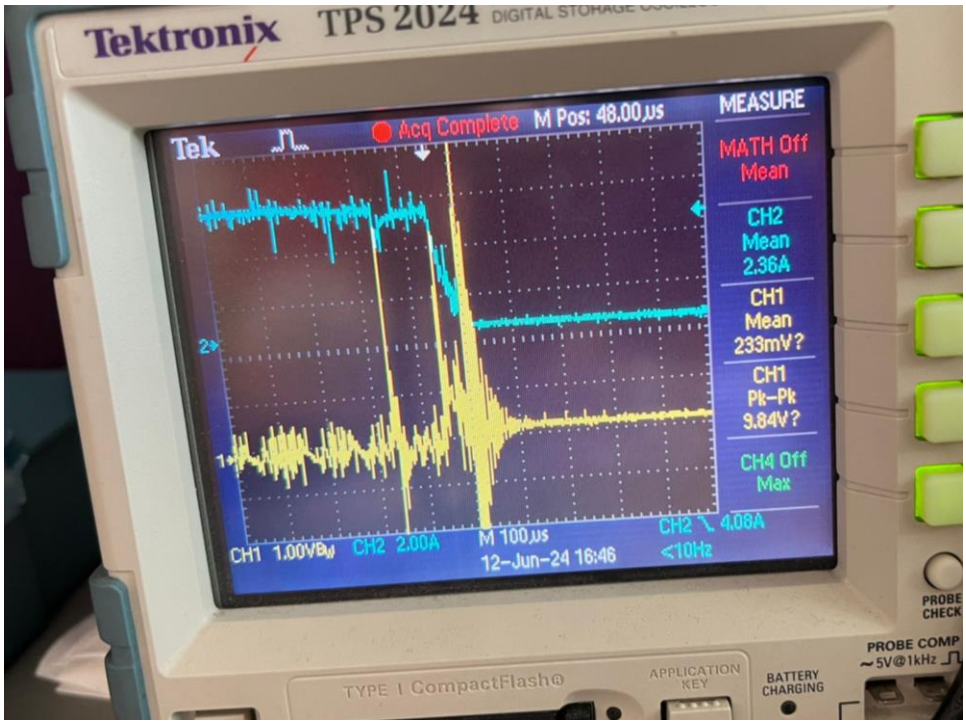


Figure 36 Load turn-off transient waveform

By observing Figures 35 and 36, one can see that the settling time of the system is approximately 200µs. The load turn-on response is quite good since there is a very small steady-state error and the rise time is 170µs. On the other hand, the turn-off transient is not so preferable. During the turn-off response, there is a ringing that can reach up to a 5V ripple. If the component rating were tighter, the ringing could be an issue; however, the components in our design were selected with a safety margin. Thus, despite the ringing, the converter can safely bear the turn off transient.

Thermal Analysis

In this part thermal analysis of the main switching devices, two paralleled MOSFETs and the output diode, are discussed. For all switching devices OZDAS0003EPL25 aluminum heatsink given in Figure 37 is used.

Figure 37 OZDAS0003EPL25 Aluminum Heatsink

All main switching devices show the same thermal lumped parameter circuit behavior given in Figure 38.

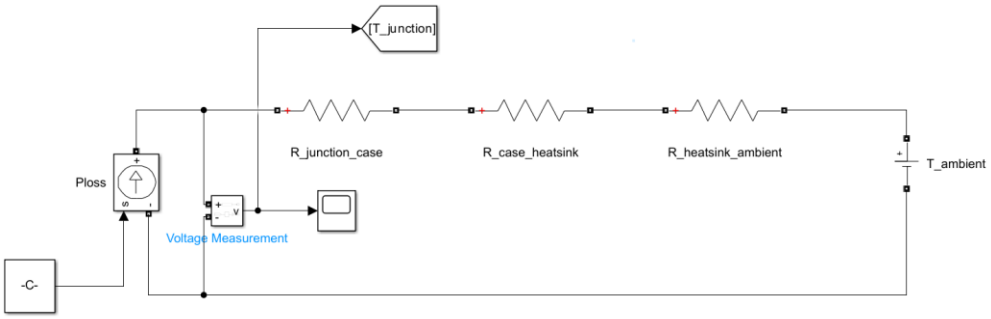


Figure 38 Thermal Lumped Parameter Circuit

The junction temperature of the semiconductor devices can be written as follows:

$$\text{Tjunction} = \text{Tambient} + \text{Ploss}\,(\text{RJC} + \text{RCH} + \text{RHA})$$

Thermal resistance from heatsink to ambient temperature is 7.5 °C/W for OZDAS0003EPL25 aluminum heatsink. The ambient temperature is taken as 30 °C since the demo is conducted in summer. Junction to case and case to heatsink thermal resistances, maximum power loss on the semiconductor devices observed in the simulation and settling junction temperature according to the formula given above are tabulated in Table 3.

Switching Device	**R_{JC} (°C/W)**	**R_{JC} (°C/W)**	**P_{loss} (W)**	**T_J (°C)**
MOSFET	1.05	0.5	1.52	44
DIODE	1.7	0.5	3.13	61

Table 3 Thermal Analysis According to Simulations

Although these results do not require any type of cooling system, in real testing MOSFET temperature is observed to exceed 100 °C. Next, oscilloscope probes are utilized to measure switch current and voltage. The power loss on the MOSFET measured as 7.5 Watts by the MATH and mean functions of the oscilloscopes as mentioned in Test Results Section. According to this measurement and lumped parameter approach MOSFET junction temperature is calculated as 96 °C which is unacceptable. Therefore, a fan is used to cool down the switching devices. In the last design MOSFET operates at 63.6 °C which is shown in Figure 39.

Figure 39 Thermal Photograph of the Converter

Cost and Sizing

The size of the product is 2000cm^3. The dimensions are 10x10x20 cm where 20cm is the height of the converter while 10cm is the width and length of the converter.

The cost analysis of the converter can be found in Table 4.

Component	**Price**
2xE Magnetic Core	156.18 TL
2x IRFU3710ZPbF	180,82 TL
UC3845AN	19,6768 TL
2xDSA30C100PB	72,466 TL
Zener diode	3,875 TL
3x PKLH-016V471MG125	7,23 TL
3x OZDAS0003EPL25	31,0866 TL
Stone resistor	2,83 TL
3xShielded double clemens	20,61 TL
4x15mΩ SMD resistor	140 TL
2xSRI1209-100M	35,53 TL
Buck Converter	200 TL
PC817X1NSZW6	4,45 TL
Fan	15 TL
Transformer cable (1.8m)	36 TL
KLS1-216-08	0,53 TL
Pertinaks 10x10	18,33 TL
Additional	20 TL
TOTAL	964.61 TL

Table 4 Cost analysis

The total cost of the product is 964.61 TL, as given in the table above. It should be noted that the main factor that increased the cost is the quantity of the components. While having similar specifications, topologies with lesser component numbers, such as full-bridge converter, can be implemented at a much lesser cost.

Conclusion

To conclude, this report information about the research, design and implementation of the EE464 term project, isolated DC-DC battery charger, in detail. In the research phase, several topologies are investigated to choose the most suitable isolated DC-DC converter topology for the given specs. The team decided on the utilization of the flyback converter topology due to its simplicity and safe operation. A flyback converter was designed and its operation was confirmed using LTSpice simulations. After some changes to the design that are decided upon in the feedback session, the topology has been implemented. Following the implementation, some unforeseen situations have arisen and discrepancies in the operation of the converter from the simulation have been identified. Due to unpredictable conditions, heating up of the converter, mainly MOSFET, became a problem. To solve this problem a cooling fan and a parallel MOSFET that will share the current with the original MOSFET have been implemented. On the demonstration day, we demonstrated the line regulation, the quickness of response time of the system, rated values, behavior during sudden load turn on/off and battery charging capability of the converter. Moreover, a datasheet was prepared and given to people who were there on the demonstration day. The addition of the fan along with the unpredicted MOSFET parameters caused a difference between the expected efficiency and the measured efficiency which is the only project specification the converter could not meet. Overall, we learned so many practical power electronics knowledge, implemented hardware and we believe that we have successfully completed the project.

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[7] https://cdn.ozdisan.com/ETicaret_Dosya/488135_6340503.pdf

[8] https://cdn.ozdisan.com/ETicaret_Dosya/342170_703953.pdf