# Component Selection

According to the waveforms, shown in the Simulation part, we have decided on the important components. The core selection was justified in the Magnetic Design part; thus, there will not be any information about the magnetic core in this section.

* **MOSFET:** IRFU3710ZPbF [3]

As shown in the Simulation section, the MOSFET has a peak voltage level of around 70V, due to ringing, which means the MOSFET should endure a voltage stress much higher than the input voltage. Moreover, this value is changing according to the designed snubber which is not finalized in this project for the time being. To account for all of this, a relatively high safety margin must be considered while choosing a MOSFET. IRFU3710ZPbF can bear 100V and 39A while having an 18mΩ which is quite good for our design; thus, we have chosen this MOSFET.

* **IC:** UC3843B [4]

UC3843B is a current-mode PWM controller. It has a low start-up current (< 0.5 mA), which is advantageous for the flyback converter. It can operate up to 500kHz and can provide up to a full-duty cycle. Moreover, it is selected since its usage in isolated power converters is highly known and a high number of sources can be found on its driving circuitry.

* **Diode:** DSA30C100PB [5]

While the design includes 4 diodes, three Schottky and one Zener, the most important ones are the one at the secondary winding side and the one at the snubber. The snubber diode has a peak voltage of 70V, just like the MOSFET. However, it has a lower forward current than the MOSFET with a 7A peak. The chosen diode can withstand 100V and it has an IF rating of 15A. The voltage drop in the conduction is 0.73V which is one of the lowest values we could find; thus, we have chosen this diode since efficiency is one of the main concerns in this project. Also, since both diodes have similar waveforms, we will be using this for both of the diodes.

* **Optocoupler:** PC817X [6]

We have chosen a single channel optocoupler since we need only one channel and cost can increase with the increasing number of channels. Moreover, we have chosen this optocoupler since it is easy to find and economically feasible.

* **Output Capacitor:** PKLH-016V471MG125 [7]

We have chosen this one as the output capacitor. It is an Aluminum Electrolytic Capacitor with a voltage rating of 16V. While only one of them is 470µF, we will parallel four of them to reduce ESR while having the wanted capacitance rating at the output side.

Aside from the components mentioned above, various resistors and capacitors will be used.

# Test Results

When we implemented the circuit we simulated, we saw that under full load at 20V input condition, the MOSFET can heat up to 110℃ under ten seconds. As a precaution, we have added a cooling fan to the circuit. Moreover, to drive the fan and supply the controller, we have used a 15V out buck converter that can easily operate at 40V input voltage. After implementing the fan, we observed that despite cooling via a fan, the MOSFET still heats up to 100℃ after some run time. To solve the heating of the MOSFET, we have added a second MOSFET in parallel to the first one. While paralleling MOSFETs is not considered as a good practice, by paralleling we have successfully reduced the current in a MOSFET to half of its original value and the MOSFET heats stabilized around 50-60℃. After finalizing the circuit, we have moved to conduct the tests. In Figure **…** finalized converter picture is given.

A close up of a machine

Description automatically generated

Figure 1. Finalized and implemented design

The converter displays different characteristics at different input voltage and loading conditions; thus, a comprehensive analysis is needed. The first analysis we made was to compare output voltage, input power, temperatures, line regulation and efficiency for different loading conditions. In **Table X,** you can see the converter data gathered from the initial test.

Table 1. Gathered power, voltage and temperature data of the converter

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Pout(W) | Vin(V) | Vref(V) | Vout(V) | Pin(W) | Tmax (°C) | TMOSFET (°C) | Regulation | Efficiency (%) |
| 0 | 30 | 12.5 | 12.5 | 3.6 | 30 | 26 | 0% | 0 |
| 6 | 20 | 12.5 | 12.46 | 12.5 | 32 | 26 | 0.32% | 48 |
| 6 | 30 | 12.5 | 12.48 | 13.1 | 35 | 28 | 0.16% | 45.8 |
| 6 | 40 | 12.5 | 12.5 | 13.5 | 32 | 27 | 0% | 44.4 |
| 30 | 20 | 12.5 | 12.4 | 46.2 | 40 | 33 | 0.8% | 64.9 |
| 30 | 30 | 12.5 | 12.4 | 47.2 | 50 | 35 | 0.8% | 63.6 |
| 30 | 40 | 12.5 | 12.5 | 49.5 | 52 | 37 | 0% | 60.6 |
| 45 | 20 | 12.5 | 12.3 | 77 | 67 | 55 | 1.6% | 58.4 |
| 45 | 30 | 12.5 | 12.4 | 69.5 | 60.3 | 45 | 0.8% | 64.7 |
| 45 | 40 | 12.5 | 12.4 | 75.5 | 57 | 40 | 0.8% | 59.6 |
| 60 | 20 | 12.5 | 12.2 | 99 | 95 | 70 | 2.4% | 60.6 |
| 60 | 30 | 12.5 | 12.2 | 95.1 | 67.2 | 57 | 2.4% | 63.1 |
| 60 | 40 | 12.5 | 12.2 | 92.3 | 67 | 55 | 2.4% | 65 |

As can be seen from the above table, the optimum operating condition of the converter is at the rated load while the input is 40V. Moreover, we can see that the voltage regulation of the converter is inside the specified region for all the operating conditions. While the peak efficiency was reached at rated load, line regulation is better at low output power conditions. Due to forced cooling, there is not any heat problem, as can be understood from the given temperature data.

From the given table, the following graphs that show the behavior of the converter can be deduced.

A graph of a line voltage

Description automatically generated

Figure 2. Line regulation at various output power

A graph with lines and numbers

Description automatically generated

Figure 3. Output regulation

A graph of a voltage

Description automatically generated

Figure 4. Input power to output power

A graph of a voltage

Description automatically generated

Figure 5. Maximum temperature inside the converter according to output power

A graph of a voltage

Description automatically generated

Figure 6. Maximum temperature of MOSFETs' according to output power

A graph of a power line

Description automatically generated with medium confidence

Figure 7. Efficiency according to output power

In **Figure 1**, the output voltage at different input voltages for various output powers is given. **Figure 2** shows the output voltage to output power correlation for different input voltages. **Figure 3** shows the linear behavior of the system and the input-output power relationship. The remaining figures give information about the component temperatures and efficiency. As can be observed, with the fan added, the component temperatures are kept at suitable levels. Moreover, it is obvious that after a certain point, 30W output power, the efficiency of the converter converges to approximately 66%.

While in the simulations the efficiency of the converter is around 80%, in reality, we have observed an efficiency of 66%. We have identified two main reasons for this efficiency discrepancy between the simulation and the hardware implementation. The first reason is the RDS(ON) difference. While in the datasheet of the IRFU3710ZPbF the RDS(ON) is given as 23mΩ, after some investigation, we believe that IRFU3710ZPbF has a much higher RDS(ON) value than the one given in the datasheet. The fact that the MOSFET heats up drastically without a parallel MOSFET and a fan supports the claim. Since it has a much higher resistance, the power drop on the MOSFET becomes higher than the simulated power drop since the current magnitude is similar in both the simulation and the tests. In the simulation, the power dissipated on the MOSFET is calculated as 2W; however, when we calculated the power dissipation on the MOSFET of the implemented circuit using oscilloscope waveforms, we have seen that it was approximately 7.6W. The second reason is the addition of the fan. As mentioned above, to keep the heat at manageable levels, we have added a cooling fan. The fan draws 3W in steady-state operation, which reduces the efficiency where 60W is the rated power. In summary, the addition of a fan which is nonexistent in the simulation and the difference between the given RDS(ON) and real RDS(ON) values are the reasons for the reduced efficiency.

For a more comprehensive analysis, we have observed and recorded the waveforms.

No load waveform:

A screen with a graph on it

Description automatically generated

Figure 8. Waveform at no load

10% loading waveforms:

A close up of a device

Description automatically generated

Figure 9. Ten percent loading at 20V input voltage waveforms

A close up of a device

Description automatically generated

Figure 10. Ten percent loading at 40V input voltage waveform

50% loading waveforms:

A close up of a device

Description automatically generated

Figure 11. Half-rated loading at 20V input voltage waveform

A screen with a blue and red line

Description automatically generated

Figure 12. Half-rated loading at 40V input voltage waveform

Rated loading waveforms:

A white electronic device with buttons and a screen

Description automatically generated

Figure 13. Rated loading at 20V input voltage waveform

A white electronic device with buttons and a screen

Description automatically generated

Figure 14. Rated loading at 30V input voltage waveform

A white electronic device with buttons and a screen

Description automatically generated

Figure 15. Rated loading at 40V input voltage waveforms

In Figures **8- 11**, it is seen that the converter can hold the voltage while supplying a below-rated output current. Moreover, it can be seen that output voltage decreases slightly as loading increases. The existence of spikes due to switching can be seen especially in CH2 waveforms; however, the spikes were not large enough to jeopardize the operation.

The full loading at 20V input is considered to be the most unsafe operation condition due to the highest current value; nevertheless, in Figure **12**, it is seen that the converter can bear the current without a clear difference in the waveforms, which shows the capability of the converter.

After confirming and gathering data on the steady-state operation, the transient behaviors were investigated.

A white electronic device with buttons and a screen

Description automatically generated

Figure 16. Full load start at 20V

A white electronic device with buttons and a screen

Description automatically generated

Figure 17. Full load start at 40V

In the above figures, the capability of full load start is shown. Despite drawing a larger current in the start-up than the steady state, the converter can tolerate the current and stabilize itself. However, a soft start is always preferred.

A close up of a device

Description automatically generated

Figure 18. Load turn-on transient waveform

A close up of a monitor

Description automatically generated

Figure 19. Load turn-off transient waveform

By observing Figures **17** and **18**, one can see that the settling time of the system is approximately 200µs. The load turn-on response is quite good since there is a very small steady-state error and the rise time is 170µs. On the other hand, the turn-off transient is not so preferable. During the turn-off response, there is a ringing that can reach up to a 5V ripple. If the component rating were tighter, the ringing could be an issue; however, the components in our design were selected with a safety margin. Thus, despite the ringing, the converter can safely bear the turn off transient.