# 1. Description

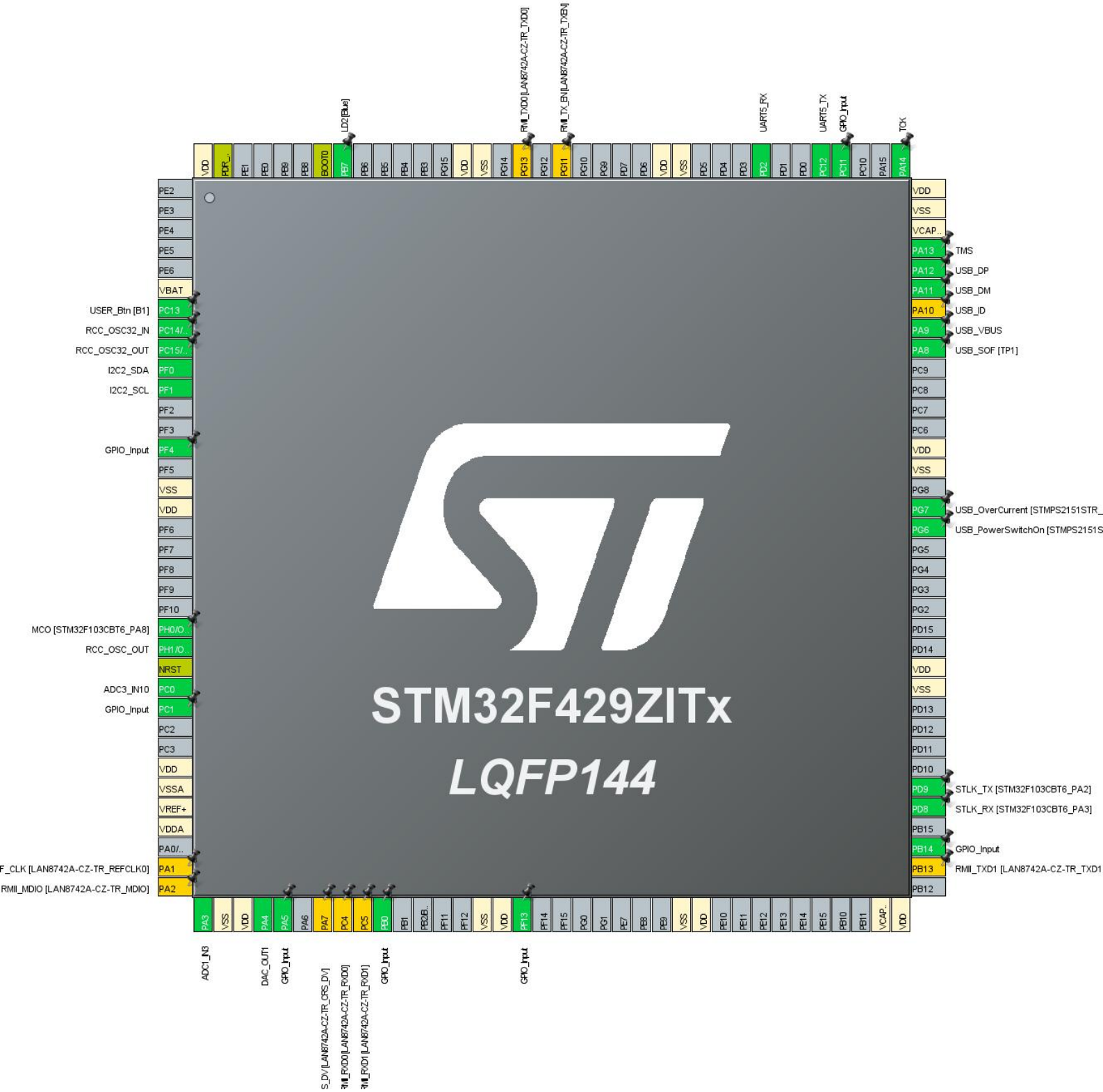
## 1.1. Project

| | |
|---|---|
| Project Name | DAC_LOAD_DRIVER_4 |
| Board Name | NUCLEO-F429ZI |
| Generated with: | STM32CubeMX 5.6.0 |
| Date | 02/15/2021 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F4 |
| MCU Line | STM32F429/439 |
| MCU name | STM32F429ZITx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

## 2. Pinout Configuration



# 3. Pins Configuration

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 6 | VBAT | Power | | |
| 7 | PC13 | I/O | GPIO_EXTI13 | USER_Btn [B1] |
| 8 | PC14/OSC32_IN | I/O | RCC_OSC32_IN | |
| 9 | PC15/OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 10 | PF0 | I/O | I2C2_SDA | |
| 11 | PF1 | I/O | I2C2_SCL | |
| 14 | PF4 * | I/O | GPIO_Input | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 23 | PH0/OSC_IN | I/O | RCC_OSC_IN | MCO [STM32F103CBT6_PA8] |
| 24 | PH1/OSC_OUT | I/O | RCC_OSC_OUT | |
| 25 | NRST | Reset | | |
| 26 | PC0 | I/O | ADC3_IN10 | |
| 27 | PC1 * | I/O | GPIO_Input | |
| 30 | VDD | Power | | |
| 31 | VSSA | Power | | |
| 32 | VREF+ | Power | | |
| 33 | VDDA | Power | | |
| 35 | PA1 ** | I/O | ETH_REF_CLK | RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0] |
| 36 | PA2 ** | I/O | ETH_MDIO | RMII_MDIO [LAN8742A-CZ-TR_MDIO] |
| 37 | PA3 | I/O | ADC1_IN3 | |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 40 | PA4 | I/O | DAC_OUT1 | |
| 41 | PA5 * | I/O | GPIO_Input | |
| 43 | PA7 ** | I/O | ETH_CRS_DV | RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV] |
| 44 | PC4 ** | I/O | ETH_RXD0 | RMII_RXD0 [LAN8742A-CZ-TR_RXD0] |
| 45 | PC5 ** | I/O | ETH_RXD1 | RMII_RXD1 [LAN8742A-CZ-TR_RXD1] |
| 46 | PB0 * | I/O | GPIO_Input | |
| 51 | VSS | Power | | |

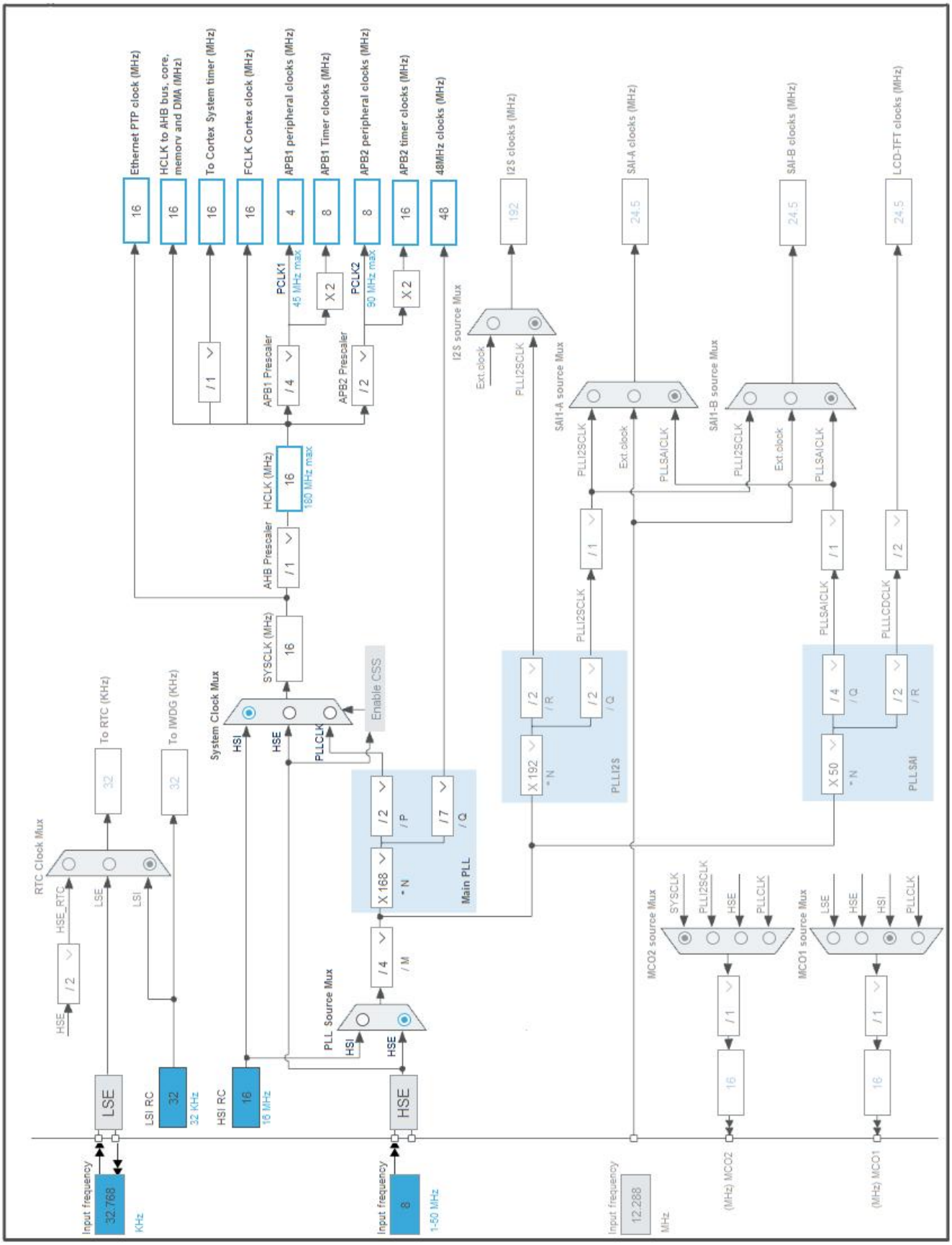
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 52 | VDD | Power | | |
| 53 | PF13 * | I/O | GPIO_Input | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 71 | VCAP_1 | Power | | |
| 72 | VDD | Power | | |
| 74 | PB13 ** | I/O | ETH_TXD1 | RMII_TXD1 [LAN8742A-CZ-TR_TXD1] |
| 75 | PB14 * | I/O | GPIO_Input | |
| 77 | PD8 | I/O | USART3_TX | STLK_RX [STM32F103CBT6_PA3] |
| 78 | PD9 | I/O | USART3_RX | STLK_TX [STM32F103CBT6_PA2] |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 91 | PG6 * | I/O | GPIO_Output | USB_PowerSwitchOn [STMPS2151STR_EN] |
| 92 | PG7 * | I/O | GPIO_Input | USB_OverCurrent [STMPS2151STR_FAULT] |
| 94 | VSS | Power | | |
| 95 | VDD | Power | | |
| 100 | PA8 | I/O | USB_OTG_FS_SOF | USB_SOF [TP1] |
| 101 | PA9 | I/O | USB_OTG_FS_VBUS | USB_VBUS |
| 102 | PA10 ** | I/O | USB_OTG_FS_ID | USB_ID |
| 103 | PA11 | I/O | USB_OTG_FS_DM | USB_DM |
| 104 | PA12 | I/O | USB_OTG_FS_DP | USB_DP |
| 105 | PA13 | I/O | SYS_JTMS-SWDIO | TMS |
| 106 | VCAP_2 | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |
| 109 | PA14 | I/O | SYS_JTCK-SWCLK | TCK |
| 112 | PC11 * | I/O | GPIO_Input | |
| 113 | PC12 | I/O | UART5_TX | |
| 116 | PD2 | I/O | UART5_RX | |
| 120 | VSS | Power | | |
| 121 | VDD | Power | | |
| 126 | PG11 ** | I/O | ETH_TX_EN | RMII_TX_EN [LAN8742A-CZ-TR_TXEN] |
| 128 | PG13 ** | I/O | ETH_TXD0 | RMII_TXD0 [LAN8742A-CZ-TR_TXD0] |
| 130 | VSS | Power | | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 131 | VDD | Power | | |
| 137 | PB7 * | I/O | GPIO_Output | LD2 [Blue] |
| 138 | BOOT0 | Boot | | |
| 143 | PDR_ON | Reset | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



# 5. Software Project

## 5.1. Project Settings

| Name | Value |
|---|---|
| Project Name | DAC_LOAD_DRIVER_4 |
| Project Folder | C:\Users\erdem\STM32CubeIDE\DENEME123\DAC_LOAD_DRIVER_4 |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.25.2 |

## 5.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |

# 6. Power Consumption Calculator report

6.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F4 |
| Line | STM32F429/439 |
| MCU | STM32F429ZITx |
| Datasheet | 024030_Rev9 |

6.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |

6.3. Battery Selection

| | |
|---|---|
| Battery | Li-SOCL2(A3400) |
| Capacity | 3400.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 100.0 mA |
| Max Pulse Current | 200.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

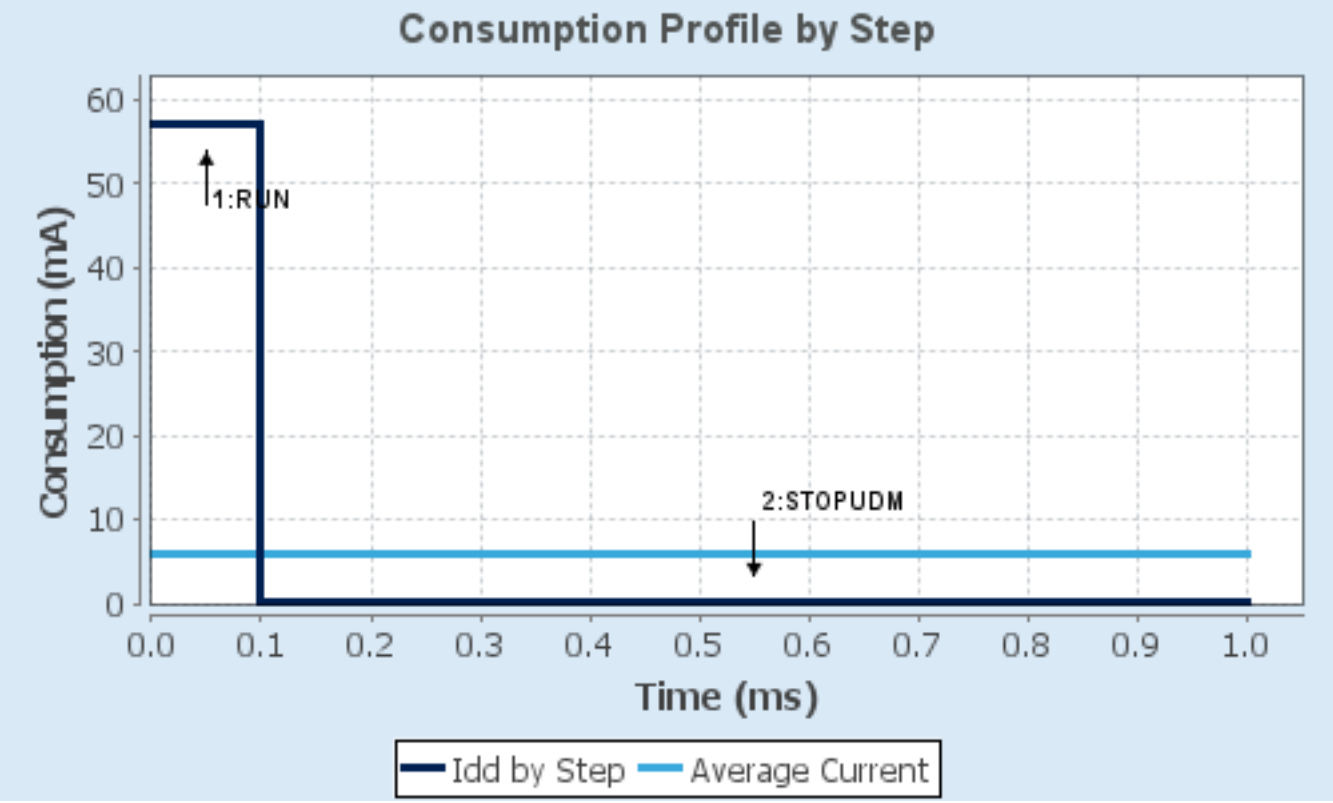
6.4. Sequence

| ***Step*** | Step1 | Step2 |
|---|---|---|
| ***Mode*** | RUN | STOP_UDM (Under Drive) |
| ***Vdd*** | 3.3 | 3.3 |
| ***Voltage Source*** | Battery | Battery |
| ***Range*** | Scale1-High | No Scale |
| ***Fetch Type*** | FLASH | n/a |
| ***CPU Frequency*** | 180 MHz | 0 Hz |
| ***Clock Configuration*** | HSE PLL | Regulator_LP Flash-PwrDwn |
| ***Clock Source Frequency*** | 4 MHz | 0 Hz |
| ***Peripherals*** | | |
| ***Additional Cons.*** | 0 mA | 0 mA |
| ***Average Current*** | 57 mA | 100 µA |
| ***Duration*** | 0.1 ms | 0.9 ms |
| ***DMIPS*** | 225.0 | 0.0 |
| ***Ta Max*** | 97.48 | 104.99 |
| ***Category*** | In DS Table | In DS Table |

## 6.5. RESULTS

| Sequence Time | 1 ms | Average Current | 5.79 mA |
|---|---|---|---|
| Battery Life | 24 days, 10 hours | Average DMIPS | 225.0 DMIPS |

## 6.6. Chart


Consumption Profile by Step
Consumption (mA)
60
50
40
30
20
10
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

# 7. IPs and Middleware Configuration

## 7.1. ADC1

**mode: IN3**

### 7.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 6 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 3 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 7.2. ADC3

**mode: IN10**

### 7.2.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | **PCLK2 divided by 6 *** |
| Resolution | 12 bits (15 ADC Clock cycles) |

| | |
|---|---|
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 10 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## *7.3. DAC*

**mode: OUT1 Configuration**

### 7.3.1. Parameter Settings:

**DAC Out1 Settings:**

| | |
|---|---|
| Output Buffer | Enable |
| Trigger | None |

## *7.4. GPIO*

## *7.5. I2C2*

**I2C: I2C**

### 7.5.1. Parameter Settings:

**Master Features:**

| | |
|---|---|
| I2C Speed Mode | **Fast Mode *** |
| I2C Clock Speed (Hz) | 400000 |
| Fast Mode Duty Cycle | Duty cycle Tlow/Thigh = 2 |

**Timing configuration:**

| | |
|---|---|
| Coefficient of Digital Filter | 0 |
| Analog Filter | Enabled |

**Slave Features:**

| | |
|---|---|
| Clock No Stretch Mode | Disabled |
| Primary Address Length selection | 7-bit |
| Dual Address Acknowledged | Disabled |
| Primary slave address | 0 |
| General Call address detection | Disabled |

## 7.6. RCC

**High Speed Clock (HSE): BYPASS Clock Source**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

### 7.6.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Instruction Cache | Enabled |
| Prefetch Buffer | Enabled |
| Data Cache | Enabled |
| Flash Latency(WS) | 0 WS (1 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Regulator Voltage Scale | Power Regulator Voltage Scale 3 |
| Power Over Drive | Disabled |

## 7.7. SYS

**Debug: Serial Wire**

**Timebase Source: SysTick**

## 7.8. UART5

### Mode: Asynchronous

### 7.8.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *7.9. USART3*

### Mode: Asynchronous

### 7.9.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

## *7.10. USB_OTG_FS*

### Mode: Device_Only

### mode: Activate_SOF

### mode: Activate_VBUS

### 7.10.1. Parameter Settings:

| | |
|---|---|
| Speed | Device Full Speed 12MBit/s |
| Low power | Disabled |
| Link Power Management | Disabled |
| VBUS sensing | Enabled |
| Signal start of frame | Enabled |

*** User modified value**

# 8. System Configuration

## 8.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC1 | PA3 | ADC1_IN3 | Analog mode | No pull-up and no pull-down | n/a | |
| ADC3 | PC0 | ADC3_IN10 | Analog mode | No pull-up and no pull-down | n/a | |
| DAC | PA4 | DAC_OUT1 | Analog mode | No pull-up and no pull-down | n/a | |
| I2C2 | PF0 | I2C2_SDA | Alternate Function Open Drain | Pull-up | **Very High *** | |
| | PF1 | I2C2_SCL | Alternate Function Open Drain | Pull-up | **Very High *** | |
| RCC | PC14/OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15/OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| | PH0/OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | MCO [STM32F103CBT6_PA8] |
| | PH1/OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | TMS |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | TCK |
| UART5 | PC12 | UART5_TX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| | PD2 | UART5_RX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| USART3 | PD8 | USART3_TX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | STLK_RX [STM32F103CBT6_PA3] |
| | PD9 | USART3_RX | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | STLK_TX [STM32F103CBT6_PA2] |
| USB_OTG_FS | PA8 | USB_OTG_FS_SOF | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_SOF [TP1] |
| | PA9 | USB_OTG_FS_VBUS | Input mode | No pull-up and no pull-down | **n/a** | USB_VBUS |
| | PA11 | USB_OTG_FS_DM | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_DM |
| | PA12 | USB_OTG_FS_DP | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_DP |
| | | | | | | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| Single Mapped Signals | PA1 | ETH_REF_CLK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_REF_CLK [LAN8742A-CZ-TR_REFCLK0] |
| | PA2 | ETH_MDIO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_MDIO [LAN8742A-CZ-TR_MDIO] |
| | PA7 | ETH_CRS_DV | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_CRS_DV [LAN8742A-CZ-TR_CRS_DV] |
| | PC4 | ETH_RXD0 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_RXD0 [LAN8742A-CZ-TR_RXD0] |
| | PC5 | ETH_RXD1 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_RXD1 [LAN8742A-CZ-TR_RXD1] |
| | PB13 | ETH_TXD1 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_TXD1 [LAN8742A-CZ-TR_TXD1] |
| | PA10 | USB_OTG_FS_ID | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | USB_ID |
| | PG11 | ETH_TX_EN | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_TX_EN [LAN8742A-CZ-TR_TXEN] |
| | PG13 | ETH_TXD0 | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | RMII_TXD0 [LAN8742A-CZ-TR_TXD0] |
| GPIO | PC13 | GPIO_EXTI13 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | USER_Btn [B1] |
| | PF4 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PC1 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PA5 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PB0 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PF13 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PB14 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PG6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | USB_PowerSwitchOn [STMPS2151STR_EN] |
| | PG7 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | USB_OverCurrent [STMPS2151STR_FAULT] |
| | PC11 | GPIO_Input | Input mode | **Pull-down *** | n/a | |
| | PB7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | LD2 [Blue] |

## *8.2. DMA configuration*

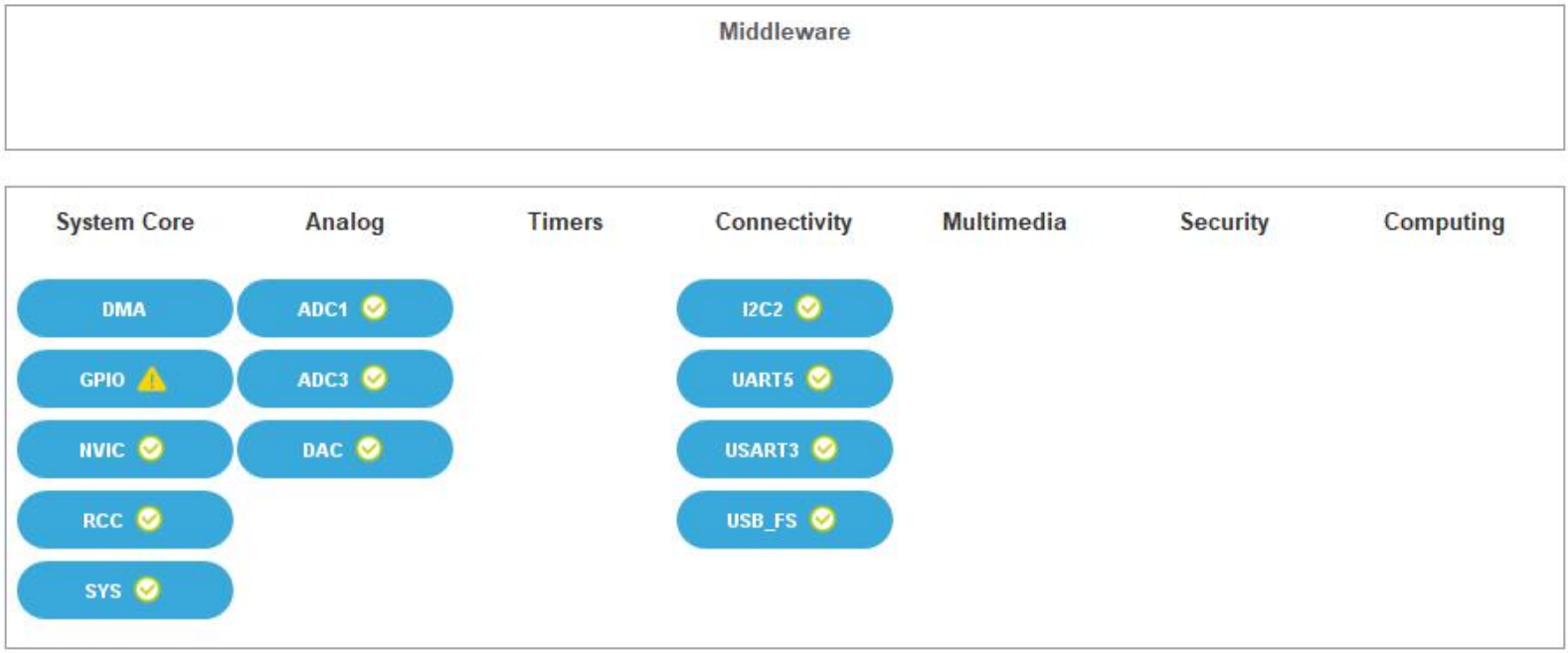
nothing configured in DMA service

## 8.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| I2C2 event interrupt | unused | | |
| I2C2 error interrupt | unused | | |
| USART3 global interrupt | unused | | |
| EXTI line[15:10] interrupts | unused | | |
| UART5 global interrupt | unused | | |
| TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts | unused | | |
| USB On The Go FS global interrupt | unused | | |
| FPU global interrupt | unused | | |

*** User modified value**

# 9. Predefined Views - Category view : Current



# 10. Software Pack Report