



VNH5019A-E

Automotive fully integrated H-bridge motor driver

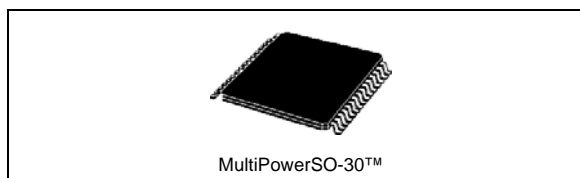
Features

| Type | $R_{DS(on)}$ | I_{out} | V_{CCmax} |
|------------|--------------------------------|-----------|-------------|
| VNH5019A-E | 18 m Ω typ (per leg) | 30 A | 41 V |

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Output current: 30 A
- 3 V CMOS compatible inputs
- Undervoltage and overvoltage shutdown
- High-side and low-side thermal shutdown
- Cross-conduction protection
- Current limitation
- Very low standby power consumption
- PWM operation up to 20 khz
- Protection against:
 - Loss of ground and loss of V_{CC}
- Current sense output proportional to motor current
- Charge pump output for reverse polarity protection
- Output protected against short to ground and short to V_{CC}

Description

The VNH5019A-E is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side drivers and two low-side switches. The high-side driver switch is designed using STMicroelectronics' well known and proven proprietary VIPower® M0 technology that allows to efficiently integrate on the same die a true



Power MOSFET with an intelligent signal/protection circuit.

The three dice are assembled in MultiPowerSO-30 package on electrically isolated lead-frames. This package, specifically designed for the harsh automotive environment offers improved thermal performance thanks to exposed die pads. The input signals IN_A and IN_B can directly interface to the microcontroller to select the motor direction and the brake condition.

The $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The CS pin allows to monitor the motor current by delivering a current proportional to its value when CS_DIS pin is driven low or left open. The PWM, up to 20 KHz, lets us to control the speed of the motor in all possible conditions. In all cases, a low-level state on the PWM pin turns-off both the LS_A and LS_B switches. When PWM rises to a high-level, LS_A or LS_B turn-on again depending on the input pin state.

Output current limitation and thermal shutdown protects the concerned high-side in short to ground condition.

The short to battery condition is revealed by the overload detector or by thermal shutdown that latches off the relevant low-side.

Active V_{CC} pin voltage clamp protects the device against low energy spikes in all configurations for the motor.

CP pin provides the necessary gate drive for an external n-channel PowerMOS used for reverse polarity protection.

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1 Block diagram and pin description

Figure 1. Block diagram

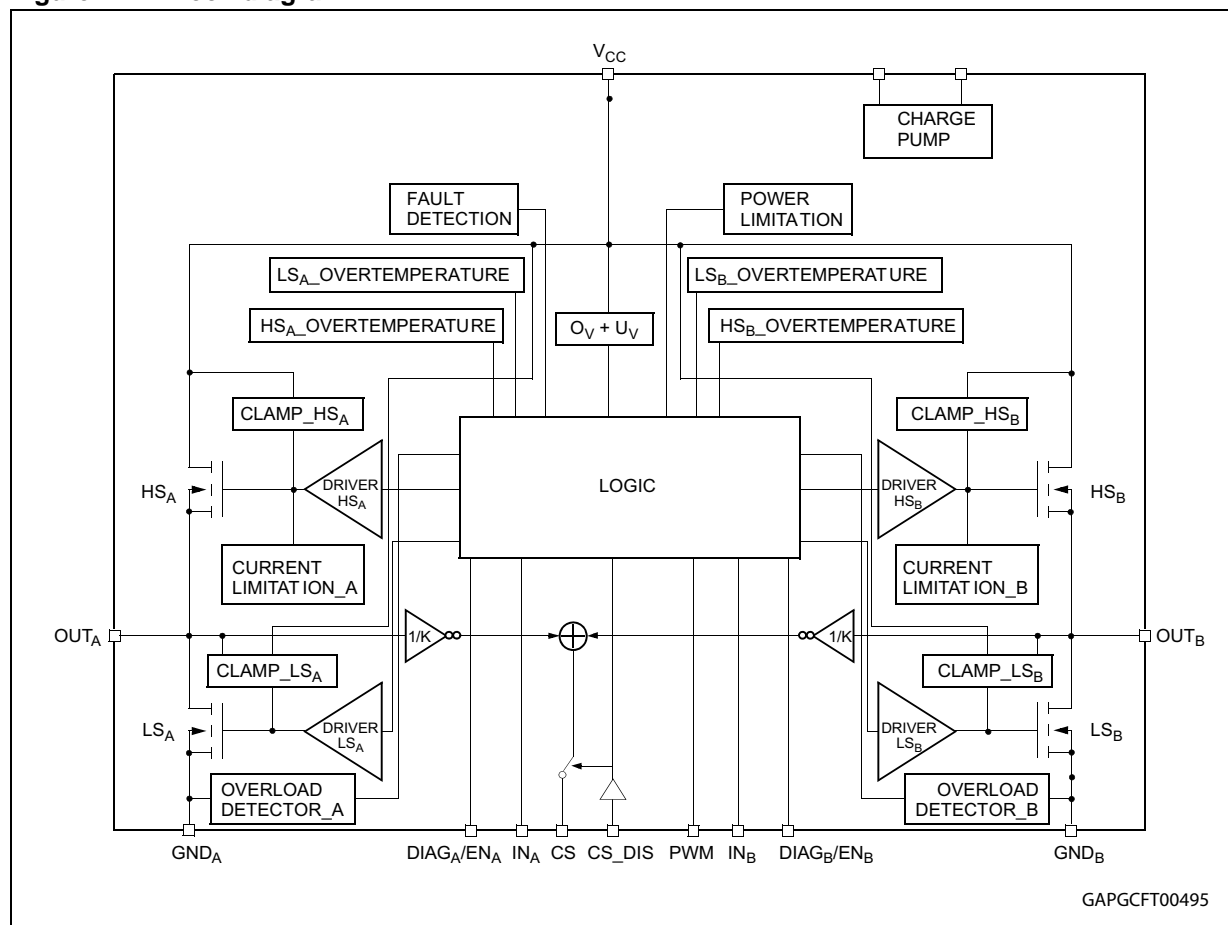


Figure 2. Configuration diagram (top view)

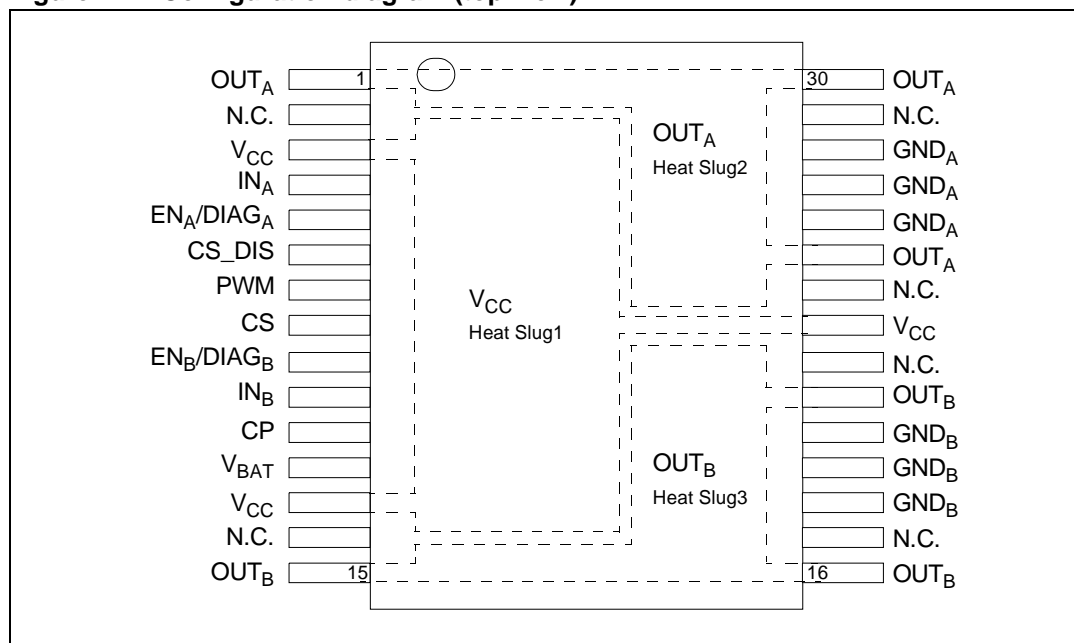


Table 1. Suggested connections for unused and not connected pins

| Connection / pin | Current sense | N.C. | OUTx | INPUTx, PWM DIAGx/ENx CS_DIS |
|------------------|-----------------------|------|-------------|------------------------------------|
| Floating | Not allowed | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 10 kΩ resistor |

Table 2. Pin definitions and functions

| Pin | Symbol | Function |
|-----------------------|------------------------------------|---|
| 1, 25, 30 | OUT _A , Heat Slug2 | Source of high-side switch A / drain of low-side switch A, power connection to the motor |
| 2,14,17, 22, 24,29 | N.C. | Not connected |
| 3, 13, 23 | V _{CC} , Heat Slug1 | Drain of high-side switches and connection to the drain of the external PowerMOS used for the reverse battery protection |
| 12 | V _{BAT} | Battery connection and connection to the source of the external PowerMOS used for the reverse battery protection |
| 5 | EN _A /DIAG _A | Status of high-side and low-side switches A; open drain output. This pin must be connected to an external pull-up resistor. When externally pulled low, it disables half-bridge A. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), this pin is pulled low by the device (see Table 13: Truth table in fault conditions (detected on OUT_A)) |

Table 2. Pin definitions and functions (continued)

| Pin | Symbol | Function |
|------------|------------------------------------|---|
| 6 | CS_DIS | Active high CMOS compatible pin to disable the current sense pin |
| 4 | IN _A | Clockwise input. CMOS compatible |
| 7 | PWM | PWM input. CMOS compatible. |
| 8 | CS | Output of current sense. This output delivers a current proportional to the motor current, if CS_DIS is low or left open. The information can be read back as an analog voltage across an external resistor. |
| 9 | EN _B /DIAG _B | Status of high-side and low-side switches B; Open drain output. This pin must be connected to an external pull up resistor. When externally pulled low, it disables half-bridge B. In case of fault detection (thermal shutdown of a high-side FET or excessive ON-state voltage drop across a low-side FET), this pin is pulled low by the device (see Table 13: Truth table in fault conditions (detected on OUTA)). |
| 10 | IN _B | Counter clockwise input. CMOS compatible |
| 11 | CP | Connection to the gate of the external MOS used for the reverse battery protection |
| 15, 16, 21 | OUT _B , Heat Slug3 | Source of high-side switch B / drain of low-side switch B, power connection to the motor |
| 26, 27, 28 | GND _A | Source of low-side switch A and power ground ⁽¹⁾ |
| 18, 19, 20 | GND _B | Source of low-side switch B and power ground ⁽¹⁾ |

1. GNDA and GNDB must be externally connected together

Table 3. Block descriptions⁽¹⁾

| Name | Description |
|---|---|
| Logic control | Allows the turn-on and the turn-off of the high-side and the low-side switches according to the Table 12 . |
| Overtoltage + undervoltage | Shut down the device outside the range [4.5 V to 24 V] for the battery voltage. |
| High-side, low-side and clamp voltage | Protect the high-side and the low-side switches from the high-voltage on the battery line in all configuration for the motor. |
| High-side and low-side driver | Drive the gate of the concerned switch to allow a proper R _{DS(on)} for the leg of the bridge. |
| Linear current limiter | Limits the motor current, by reducing the high-side switch gate-source voltage when short-circuit to ground occurs. |
| High-side and low-side overtemperature protection | In case of short-circuit with the increase of the junction's temperature, it shuts down the concerned driver to prevent its degradation and to protect the die. |
| Low-side overload detector | Detects when low-side current exceeds shutdown current and latches off the concerned low-side. |

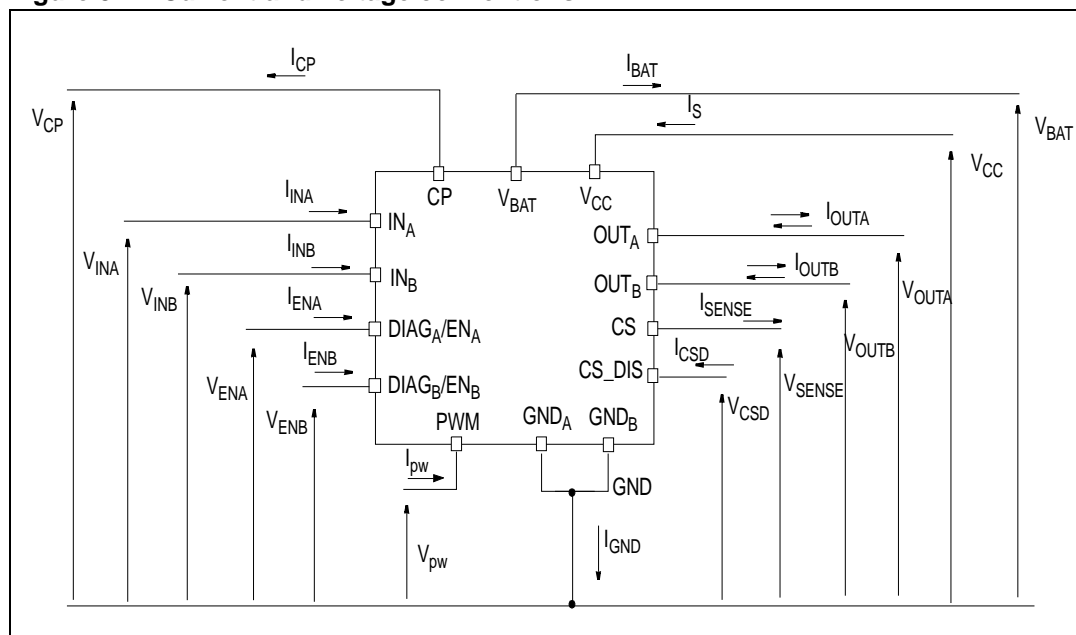
Table 3. Block descriptions⁽¹⁾ (continued)

| Name | Description |
|------------------|---|
| Charge pump | Provides the voltage necessary to drive the gate of the external PowerMOS used for the reverse polarity protection |
| Fault detection | Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by pulling down the concerned ENx/DIAGx pin. |
| Power limitation | Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition. |

1. See [Figure 1](#)

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 4. Absolute maximum rating

| Symbol | Parameter | Value | Unit |
|---------------|--|--------|------|
| V_{BAT} | Maximum battery voltage ⁽¹⁾ | -16 | V |
| | | +41 | V |
| V_{CC} | Maximum bridge supply voltage | + 41 | V |
| I_{max} | Maximum output current (continuous) | 30 | A |
| I_R | Reverse output current (continuous) | -30 | A |
| I_{IN} | Input current (IN_A and IN_B pins) | +/- 10 | mA |
| I_{EN} | Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins) | +/- 10 | mA |
| I_{pw} | PWM input current | +/- 10 | mA |
| I_{CP} | CP output current | +/- 10 | mA |
| I_{CS_DIS} | CS_DIS input current | +/- 10 | mA |

Table 4. Absolute maximum rating (continued)

| Symbol | Parameter | Value | Unit |
|-----------|--|----------------------------|--------|
| V_{CS} | Current sense maximum voltage | $V_{CC} - 41$ $+V_{CC}$ | V V |
| V_{ESD} | Electrostatic discharge (human body model: $R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$) | 2 | kV |
| T_c | Case operating temperature | -40 to 150 | °C |
| T_{STG} | Storage temperature | -55 to 150 | °C |

1. This applies with the n-channel MOSFET used for the reverse battery protection. Otherwise V_{BAT} has to be shorted to V_{CC} .

2.2 Thermal data

Table 5. Thermal data

| Symbol | Parameter | Max. value | Unit |
|----------------|--------------------------------------|-------------------------------|------|
| $R_{thj-case}$ | Thermal resistance junction-case HSD | 1.7 | °C/W |
| | Thermal resistance junction-case LSD | 3.2 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | See Figure 18 | °C/W |

2.3 Electrical characteristics

Values specified in this section are for $8\text{ V} < V_{CC} < 21\text{ V}$, $-40\text{ °C} < T_j < 150\text{ °C}$, unless otherwise specified.

Table 6. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|--|---|------|------|----------|--------------------------------|
| V_{CC} | Operating bridge supply voltage | | 5.5 | | 24 | V |
| I_S | Supply current | OFF-state with all fault cleared and $EN_x = 0\text{ V}$ (standby): $IN_A = IN_B = PWM = 0$; $T_j = 25\text{ °C}$; $V_{CC} = 13\text{ V}$ $IN_A = IN_B = PWM = 0$ | | 10 | 15 60 | μA μA |
| | | OFF-state (no standby): $IN_A = IN_B = PWM = 0$; $EN_x = 5\text{ V}$ | | | 6 | mA |
| | | ON-state: IN_A or $IN_B = 5\text{ V}$, no PWM IN_A or $IN_B = 5\text{ V}$, $PWM = 20\text{ kHz}$ | | 4 | 8 8 | mA mA |
| | | | | | | |
| R_{ONHS} | Static high-side resistance | $I_{OUT} = 15\text{ A}$; $T_j = 25\text{ °C}$ | | 12.0 | | m Ω |
| | | $I_{OUT} = 15\text{ A}$; $T_j = -40\text{ °C}$ to 150 °C | | | 26.5 | |
| R_{ONLS} | Static low-side resistance | $I_{OUT} = 15\text{ A}$; $T_j = 25\text{ °C}$ | | 6.0 | | m Ω |
| | | $I_{OUT} = 15\text{ A}$; $T_j = -40\text{ °C}$ to 150 °C | | | 11.5 | |
| V_f | High-side free-wheeling diode forward voltage | $I_f = 15\text{ A}$, $T_j = 150\text{ °C}$ | | 0.6 | 0.8 | V |
| $I_{L(off)}$ | High-side OFF-state output current (per channel) | $T_j = 25\text{ °C}$; $V_{OUTX} = EN_x = 0\text{ V}$; $V_{CC} = 13\text{ V}$ | | | 3 | μA |
| | | $T_j = 125\text{ °C}$; $V_{OUTX} = EN_x = 0\text{ V}$; $V_{CC} = 13\text{ V}$ | | | 5 | |

Table 7. Logic inputs (IN_A , IN_B , EN_A , EN_B , PWM , CS_DIS)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--------------------------|--|------|------|------|---------------|
| V_{IL} | Low-level input voltage | Normal operation ($DIAG_X/EN_x$ pin acts as an input pin) | | | 0.9 | V |
| V_{IH} | High-level input voltage | Normal operation ($DIAG_X/EN_x$ pin acts as an input pin) | 2.1 | | | V |
| I_{INL} | Low-level input current | $V_{IN} = 0.9\text{ V}$ | 1 | | | μA |
| I_{INH} | High-level input current | $V_{IN} = 2.1\text{ V}$ | | | 10 | μA |
| V_{IHYST} | Input hysteresis voltage | Normal operation ($DIAG_X/EN_x$ pin acts as an input pin) | 0.15 | | | V |

Table 7. Logic inputs (IN_A, IN_B, EN_A, EN_B, PWM, CS_DIS) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------|--|------|------|------|------|
| V _{ICL} | Input clamp voltage | I _{IN} = 1 mA | 5.5 | 6.3 | 7.5 | V |
| | | I _{IN} = -1 mA | -1.0 | -0.7 | -0.3 | |
| V _{DIAG} | Enable low-level output voltage | Fault operation (DIAG _X /EN _X pin acts as an output pin); I _{EN} = 1 mA | | | 0.4 | V |

Table 8. Switching (V_{CC} = 13 V, R_{LOAD} = 0.87 Ω, T_j = 25 °C)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---------------------|---|--|-----|-----|------|------|
| f | PWM frequency | | 0 | | 20 | kHz |
| t _{d(on)} | HSD rise time | Input rise time < 1 μs (see Figure 9) | | | 250 | μs |
| t _{d(off)} | HSD fall time | Input rise time < 1 μs (see Figure 9) | | | 250 | μs |
| t _r | LSD rise time | (see Figure 8) | | 1 | 2 | μs |
| t _f | LSD fall time | (see Figure 8) | | 1 | 2 | μs |
| t _{DEL} | Delay time during change of operating mode | (see Figure 7) | 200 | 400 | 1600 | μs |
| t _{rr} | High-side free wheeling diode reverse recovery time | (see Figure 10) | | 110 | | ns |
| I _{RM} | Dynamic cross-conduction current | I _{OUT} = 15 A (see Figure 10) | | 2 | | A |

Table 9. Protection and diagnostic

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-----------------------------------|--|-------------------------|-----|-----|-----|------|
| V _{USD} | V _{CC} undervoltage shutdown | | | 4.5 | 5.5 | V |
| V _{USDhyst} | V _{CC} undervoltage shutdown hysteresis | | | 0.5 | | V |
| V _{OV} | V _{CC} overvoltage shutdown | | 24 | 27 | 30 | V |
| I _{LIM_H} | High-side current limitation | | 30 | 50 | 70 | A |
| I _{SD_LS} | Low-side shutdown current | | 70 | 115 | 160 | A |
| V _{CLPHS} ⁽¹⁾ | High-side clamp voltage (V _{CC} to OUT _A = 0 or OUT _B = 0) | I _{OUT} = 15 A | 43 | 48 | 54 | V |
| V _{CLPLS} ⁽¹⁾ | Low-side clamp voltage (OUT _A = V _{CC} or OUT _B = V _{CC} to GND) | I _{OUT} = 15 A | 27 | 30 | 33 | V |
| T _{TSD} ⁽²⁾ | Thermal shutdown temperature | V _{IN} = 2.1 V | 150 | 175 | 200 | °C |

Table 9. Protection and diagnostic (continued)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|------------------|---------------------------------------|-----------------------|-----|-----|-----|------|
| T_{TSD_LS} | Low-side thermal shutdown temperature | $V_{IN} = 0\text{ V}$ | 150 | 175 | 200 | °C |
| $T_{TR}^{(3)}$ | Thermal reset temperature | | 135 | | | °C |
| $T_{HYST}^{(3)}$ | Thermal hysteresis | | 7 | 15 | | °C |

1. The device is able to pass the ESD and ISO pulse requirements as specified in the [Table 15](#).
2. T_{TSD} is the minimum threshold temperature between HS and LS
3. Valid for both HSD and LSD

Table 10. Current sense ($8\text{ V} < V_{CC} < 21\text{ V}$)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|---------------|---|---|------|------|-------|---------------|
| K_0 | I_{OUT}/I_{SENSE} | $I_{OUT} = 3\text{ A}$, $V_{SENSE} = 0.5\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | 4670 | 7110 | 10110 | |
| dK_0/K_0 | Analog current sense ratio drift | $I_{OUT} = 3\text{ A}$; $V_{SENSE} = 0.5\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | -19 | | 19 | % |
| K_1 | I_{OUT}/I_{SENSE} | $I_{OUT} = 8\text{ A}$, $V_{SENSE} = 1.3\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | 6060 | 7030 | 8330 | |
| dK_1/K_1 | Analog current sense ratio drift | $I_{OUT} = 8\text{ A}$; $V_{SENSE} = 1.3\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | -14 | | 14 | % |
| K_2 | I_{OUT}/I_{SENSE} | $I_{OUT} = 15\text{ A}$, $V_{SENSE} = 2.4\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | 6070 | 6990 | 7810 | |
| dK_2/K_2 | Analog current sense ratio drift | $I_{OUT} = 15\text{ A}$; $V_{SENSE} = 2.4\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | -12 | | 12 | % |
| K_3 | I_{OUT}/I_{SENSE} | $I_{OUT} = 25\text{ A}$, $V_{SENSE} = 4\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | 6000 | 6940 | 7650 | |
| dK_3/K_3 | Analog current sense ratio drift | $I_{OUT} = 25\text{ A}$; $V_{SENSE} = 4\text{ V}$, $T_j = -40\text{ °C to }150\text{ °C}$ | -12 | | 12 | % |
| V_{SENSE} | Max analog sense output voltage | $I_{OUT} = 15\text{ A}$, $R_{SENSE} = 1.1\text{ k}\Omega$ | 5 | | | V |
| I_{SENSE0} | Analog sense leakage current | $I_{OUT} = 0\text{ A}$, $V_{SENSE} = 0\text{ V}$, $V_{CSD} = 5\text{ V}$, $V_{IN} = 0\text{ V}$, $T_j = -40\text{ to }150\text{ °C}$ | 0 | | 5 | μA |
| | | $I_{OUT} = 0\text{ A}$, $V_{SENSE} = 0\text{ V}$, $V_{CSD} = 0\text{ V}$, $V_{IN} = 5\text{ V}$, $T_j = -40\text{ to }150\text{ °C}$ | 0 | | 100 | |
| $t_{DSENSEH}$ | Delay response time from falling edge of CS_DIS pin | $V_{IN} = 5\text{ V}$, $V_{SENSE} < 4\text{ V}$, $I_{OUT} = 8\text{ A}$, $I_{SENSE} = 90\%$ of $I_{SENSEmax}$ (see fig Figure 13) | | | 50 | μs |
| $t_{DSENSEL}$ | Delay response time from rising edge of CS_DIS pin | $V_{IN} = 5\text{ V}$, $V_{SENSE} < 4\text{ V}$, $I_{OUT} = 8\text{ A}$, $I_{SENSE} = 10\%$ of $I_{SENSEmax}$ (see fig Figure 13) | | | 20 | μs |

Table 11. Charge pump

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|-----------|-----------------------------|--|--------------|------|---------------|------|
| V_{CP} | Charge pump output voltage | $EN_X = 5\text{ V}$ | $V_{CC} + 5$ | | $V_{CC} + 10$ | V |
| | | $EN_X = 5\text{ V}, V_{CC} = 4.5\text{ V}$ | | 10.5 | | |
| I_{BAT} | Charge pump standby current | $EN_A = EN_B = 0\text{ V}$ | | 200 | | nA |

2.4 Waveforms and truth table

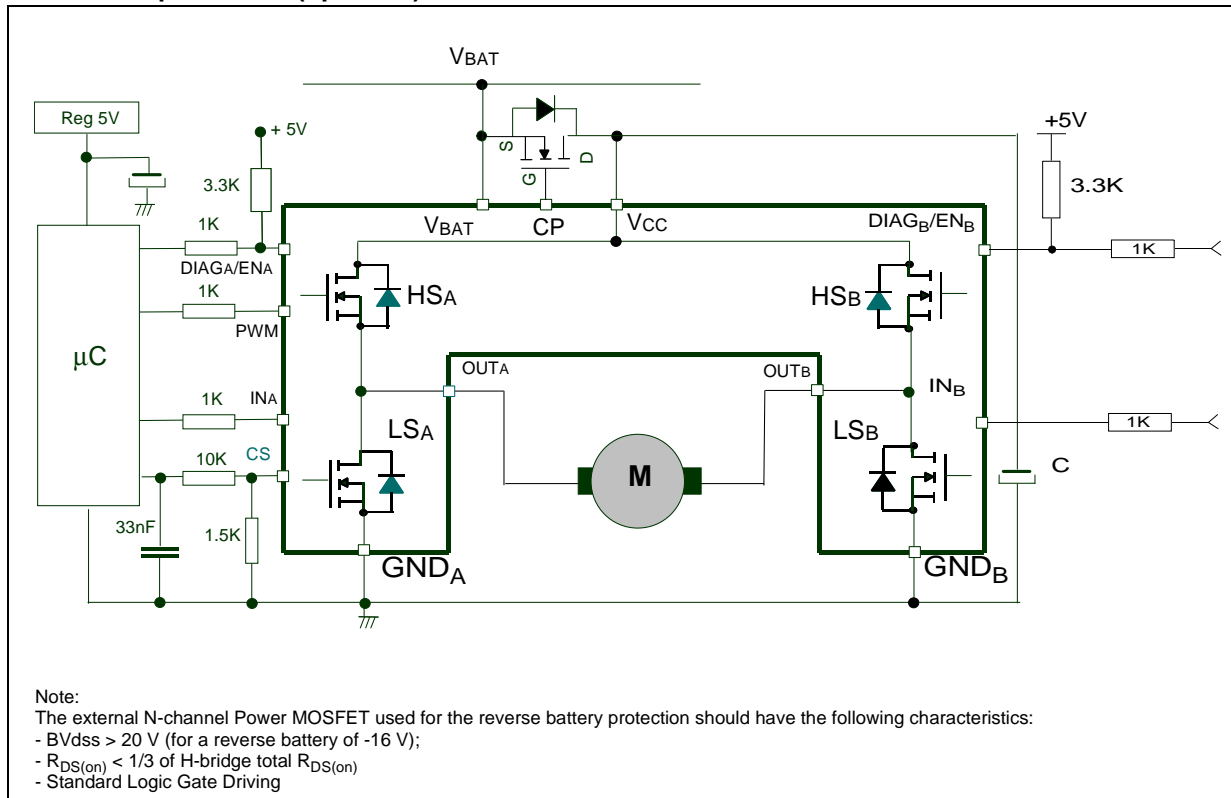
In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled-high

PWM pin usage: in all cases, a “0” on the PWM pin turns-off both LS_A and LS_B switches. When PWM rises back to “1”, LS_A or LS_B turn-on again depending on the input pin state.

Table 12. Truth table in normal operating conditions

| IN_A | IN_B | $DIAG_A/EN_A$ | $DIAG_B/EN_B$ | OUT_A | OUT_B | CS ($V_{CSD} = 0\text{ V}$) | Operating mode |
|--------|--------|---------------|---------------|---------|---------|-------------------------------|------------------------|
| 1 | 1 | 1 | 1 | H | H | High imp. | Brake to V_{CC} |
| 1 | 0 | 1 | 1 | H | L | $I_{SENSE} = I_{OUT}/K$ | Clockwise (CW) |
| 0 | 1 | 1 | 1 | L | H | $I_{SENSE} = I_{OUT}/K$ | Counterclockwise (CCW) |
| 0 | 0 | 1 | 1 | L | L | High imp. | Brake to GND |


Figure 4. Typical application circuit for DC to 20 kHz PWM operation with reverse battery protection (option A)




Note:

The value of the blocking capacitor (C) depends on the application conditions and defines voltage and current ripple onto supply line at PWM operation. Stored energy of the motor inductance may flyback into the blocking capacitor, if the bridge driver goes into 3-state. This causes a hazardous overvoltage if the capacitor is not big enough. As basic orientation, 500 μ F per 10 A load current is recommended.

| IN _A | IN _B | DIAG _A /EN _A | DIAG _B /EN _B | OUT _A | OUT _B | CS (V _{CSD} =0V) |
|-----------------|-----------------|------------------------------------|------------------------------------|------------------|------------------|---------------------------|
| 1 | 1 | 0 | 1 | OPEN | H | High impedance |
| | 0 | | | | L | |
| 0 | 1 | | | | H | I _{OUTB} /K |
| | 0 | | | | L | High impedance |
| X | X | | 0 | | OPEN | |



Fault Information



Protection Action

The fault conditions are:

- overtemperature on one or both high-sides (for example, if a short to ground occurs as it could be the case described in line 1 and 2 in the [Table 14](#));
- Short to battery condition on the output (saturation detection on the low-side Power MOSFET).

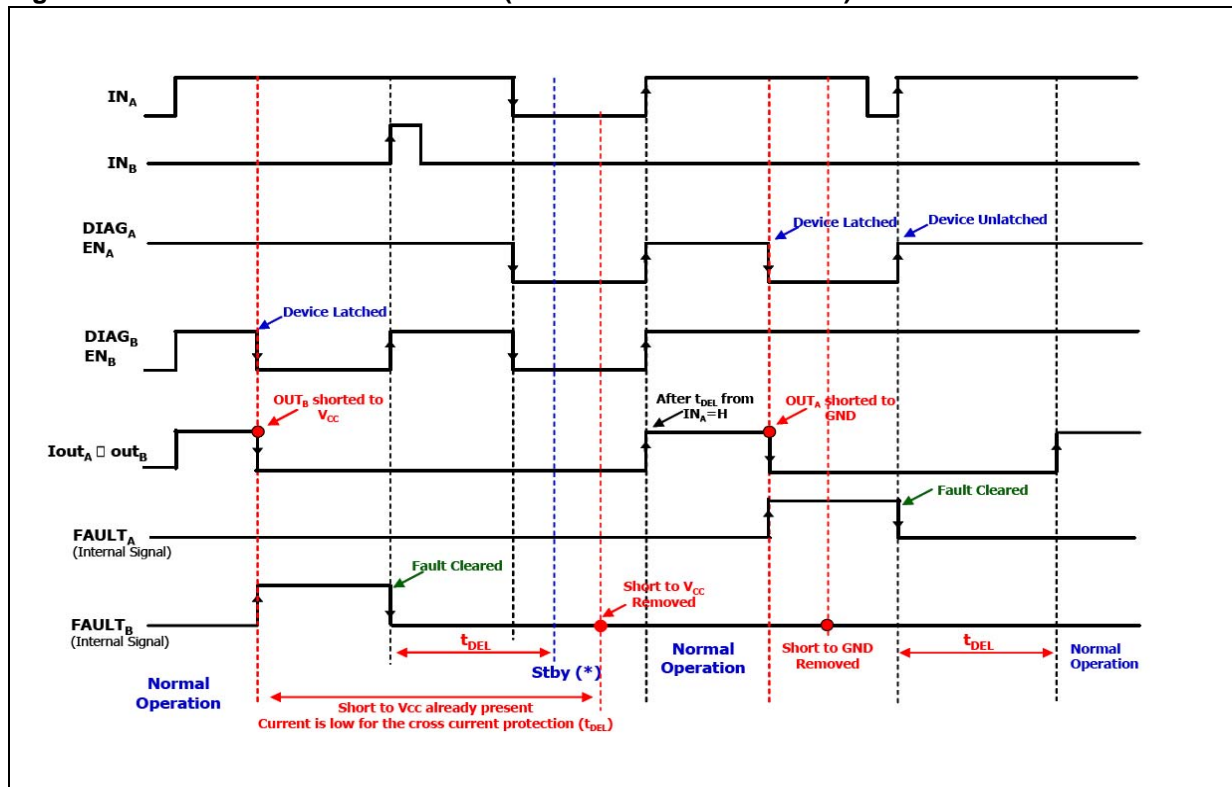
Possible origins of fault conditions may be:

- OUT_A is shorted to ground. It follows that, high-side A is in overtemperature state.
- OUT_A is shorted to V_{CC} . It follow that, low-side Power MOSFET is in saturation state.

When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A , IN_B , $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn-on the respective output (OUT_X) again, the input signal must rise from low-level to high-level.

Figure 6. Behavior in fault condition (how a fault can be cleared)



Note: In case of the fault condition is not removed, the procedure for unlatching and sending the device in Stby mode is:

- Clear the fault in the device (toggle: IN_A if $EN_A=0$ or IN_B if $EN_B=0$)
- Pull low all inputs, PWM and Diag/EN pins within t_{DEL} .

If the Diag/En pins are already low, PWM=0, the fault can be cleared simply toggling the input. The device enters in stby mode as soon as the fault is cleared.

Table 14. Electrical transient requirements (part 1)

| ISO T/R 7637/1 Test Pulse | Test level | | | | |
|---------------------------------|------------|---------|---------|---------|--------------------------|
| | I | II | III | IV | Delay and impedance |
| 1 | -25 V | -50 V | -75 V | -100 V | 2 ms, 10 Ω |
| 2 | +25 V | +50 V | +75 V | +100 V | 0.2 ms, 10 Ω |
| 3a | -25 V | -50 V | -100 V | -150 V | 0.1 μ s, 50 Ω |
| 3b | +25 V | +50 V | +75 V | +100 V | 0.1 μ s, 50 Ω |
| 4 | -4 V | -5 V | -6 V | -7 V | 100 ms, 0.01 Ω |
| 5 | +26.5 V | +46.5 V | +66.5 V | +86.5 V | 400 ms, 2 Ω |

Table 15. Electrical transient requirements (part 2)

| ISO T/R 7637/1 Test Pulse | Test levels | | | |
|---------------------------------|-------------|----|-----|----|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

Table 16. Electrical transient requirements (part 3)

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

2.5 Reverse battery protection

Against reverse battery condition the charge pump feature allows to use an external N-channel MOSFET connected as shown in the typical application circuit (see [Figure 4](#)).

As alternative option, a N-channel MOSFET connected to GND pin can be used (see typical application circuit in figure [Figure 5](#)).

With this configuration we recommend to short V_{BAT} pin to V_{CC} .

The device sustains no more than -30 A in reverse battery conditions because of the two body diodes of the Power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH5019A-E is pulled-down to the V_{CC} line (approximately -1.5 V). Series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through microcontroller I/Os, series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

Figure 7. Definition of the delay times measurement

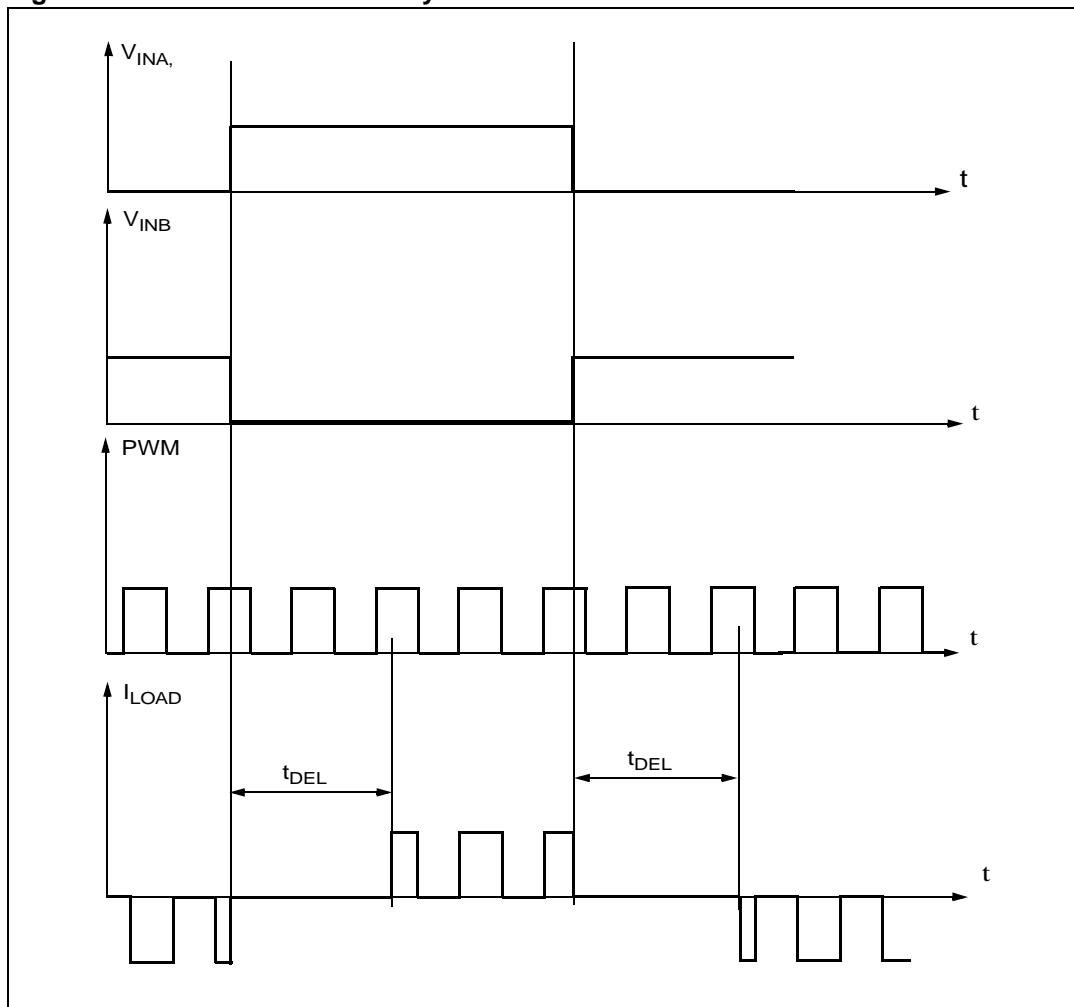


Figure 8. Definition of the low-side switching times

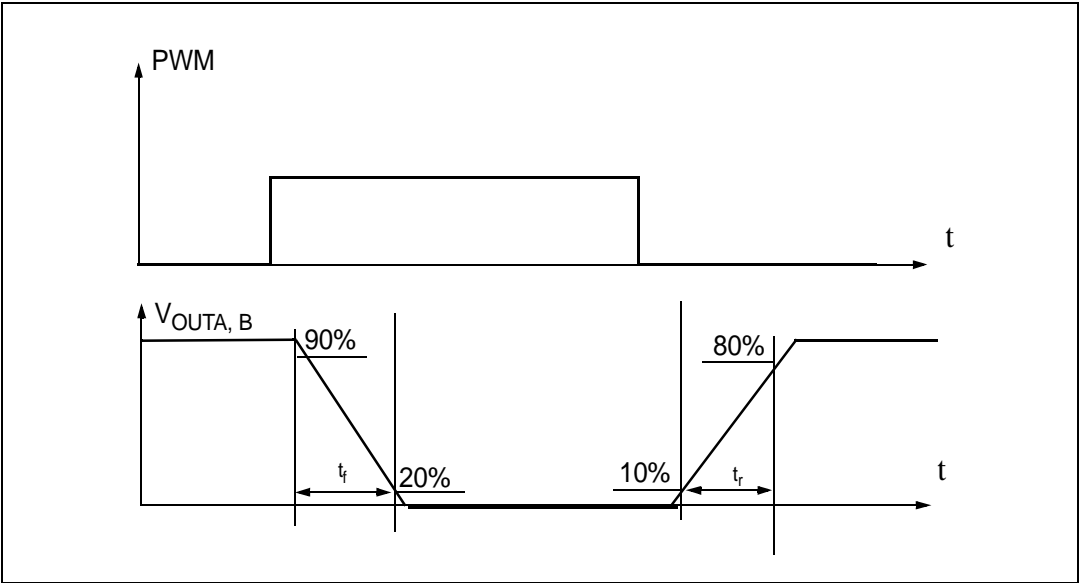


Figure 9. Definition of the high-side switching times

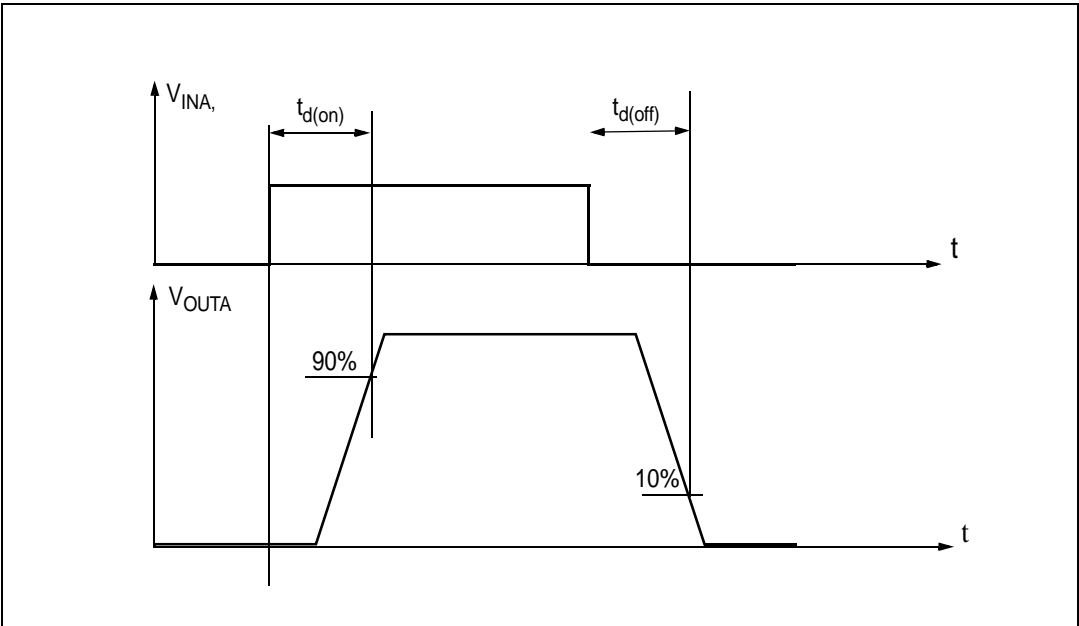


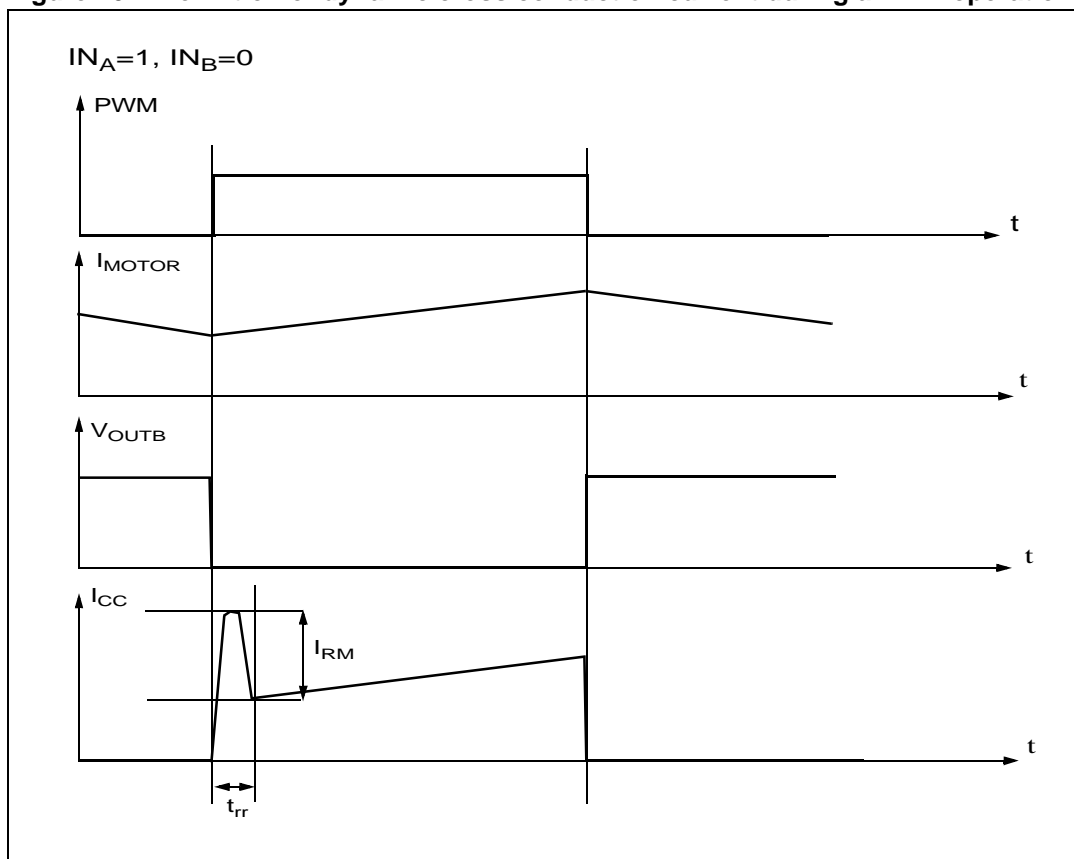
Figure 10. Definition of dynamic cross conduction current during a PWM operation

Figure 11. Waveforms in full bridge operation (part 1)

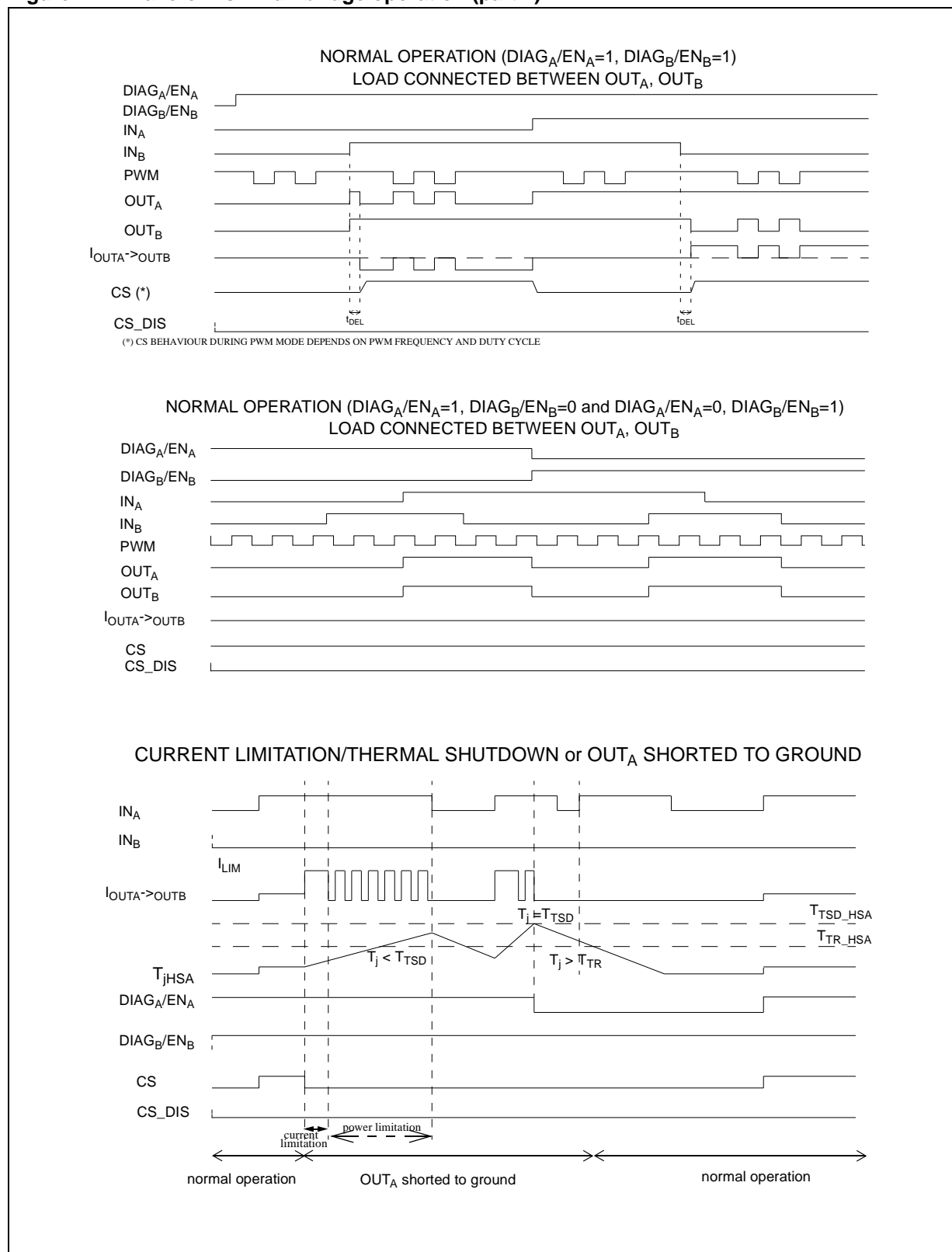


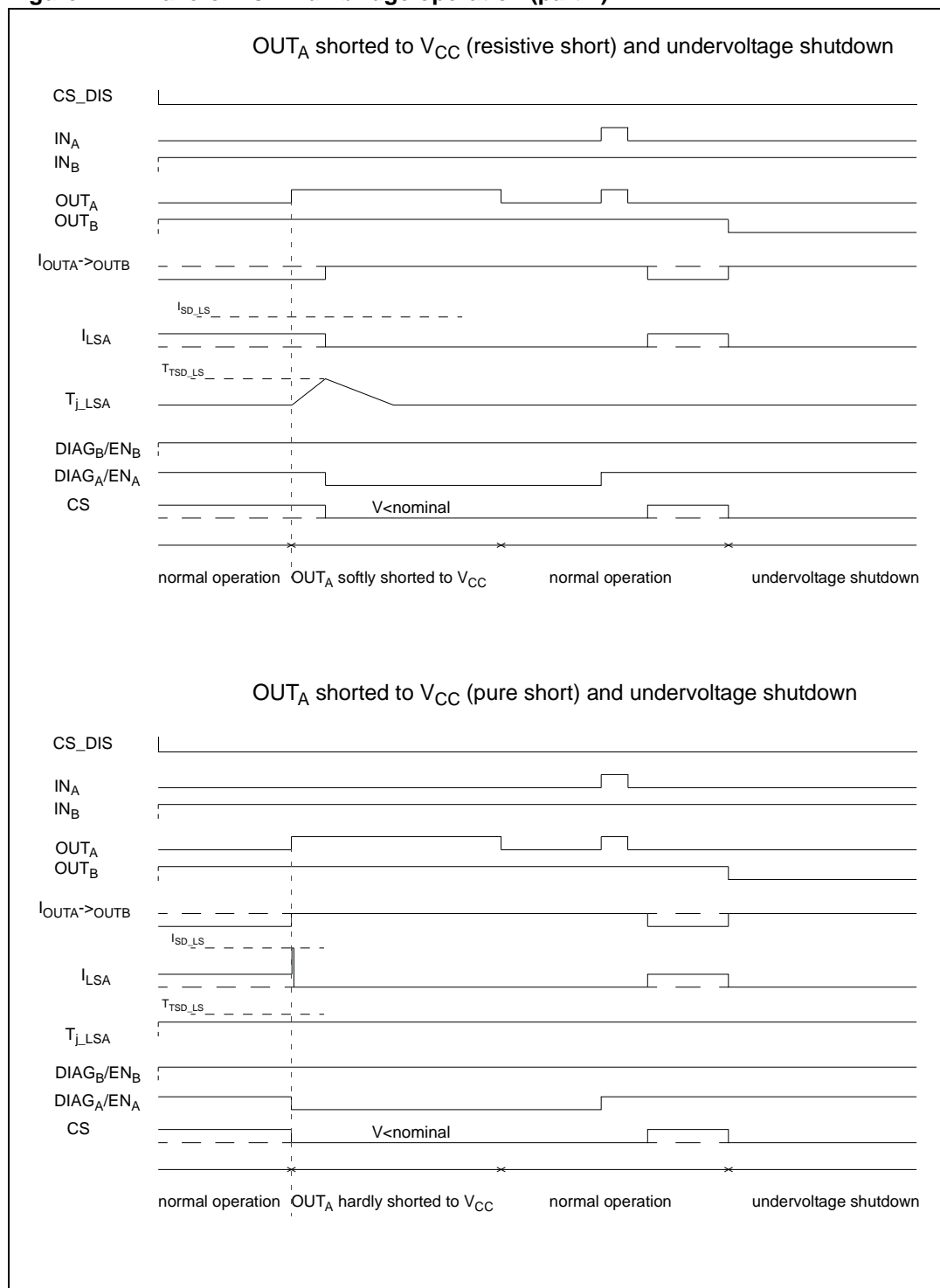
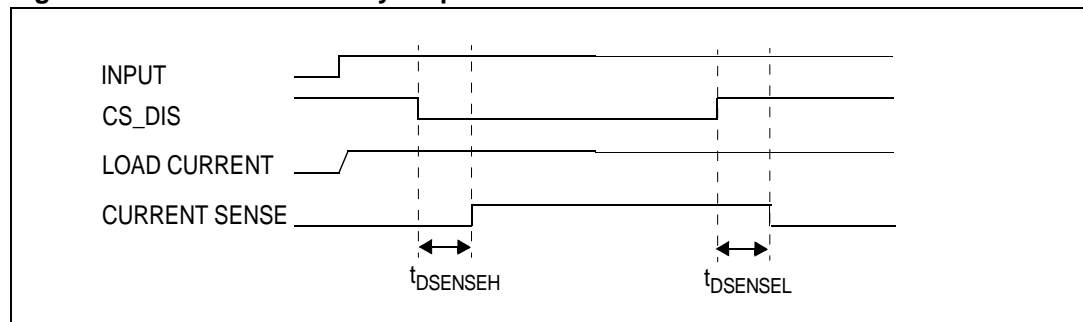
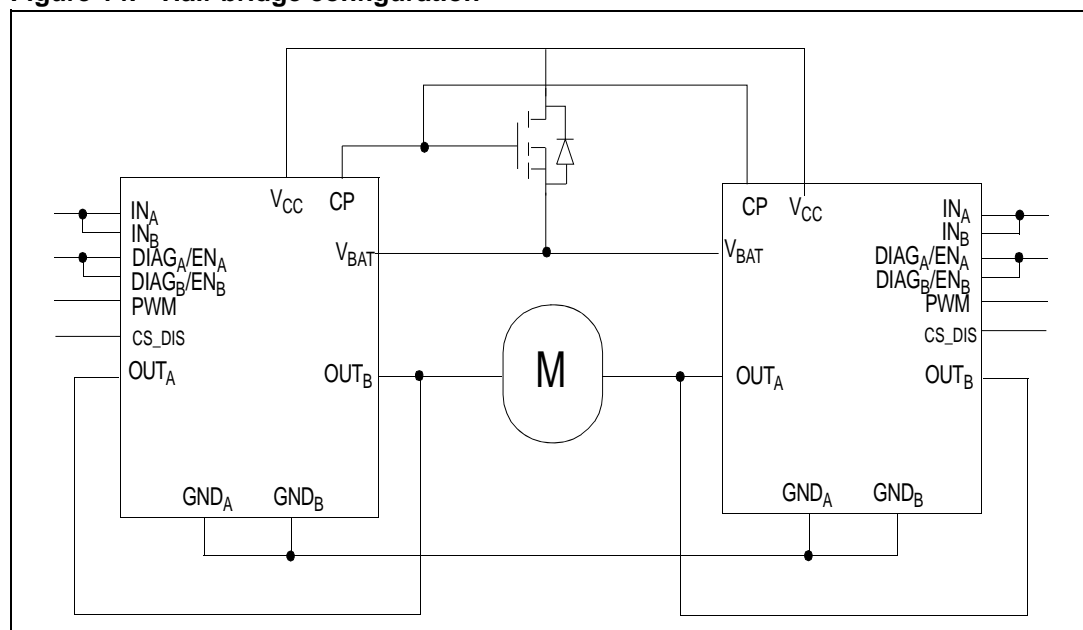
Figure 12. Waveforms in full bridge operation (part 2)


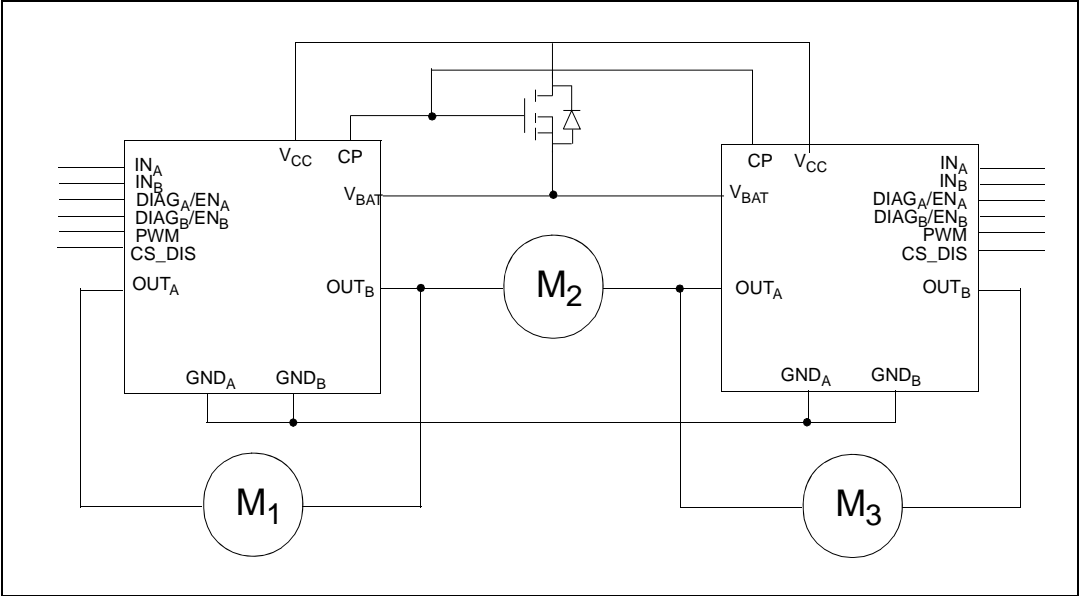
Figure 13. Definition of delay response time of sense current

The VNH5019A-E can be used as a high power half-bridge driver achieving an on- resistance per leg of 9.5 mΩ. The figure below shows the suggested configuration:

Figure 14. Half-bridge configuration

The VNH5019A-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. DIAG_x/EN_x pins allow to put unused half-bridges in high-impedance. The figure below shows the suggested configuration:

Figure 15. Multi-motors configuration



3 Package and PCB thermal data

3.1 MultiPowerSO-30 thermal data

Figure 16. MultiPowerSO-30™ PC board

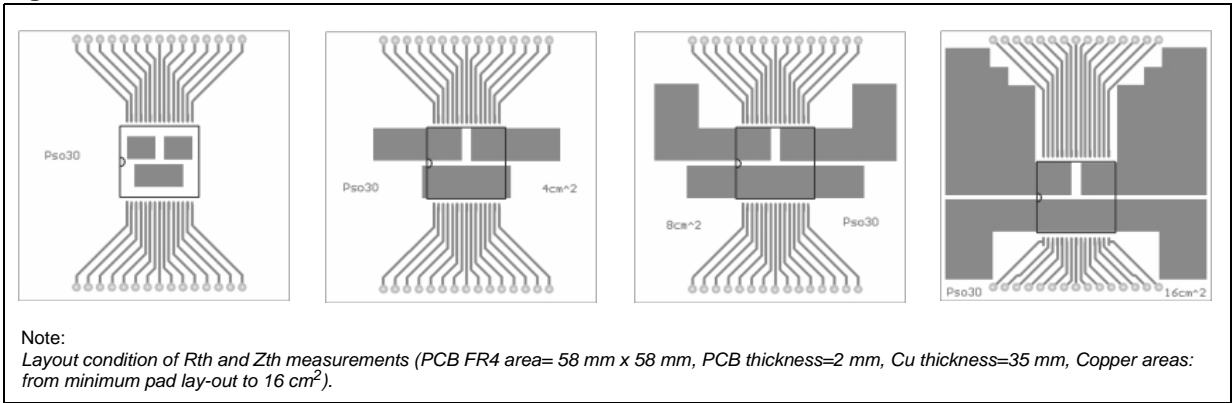


Figure 17. Chipset configuration

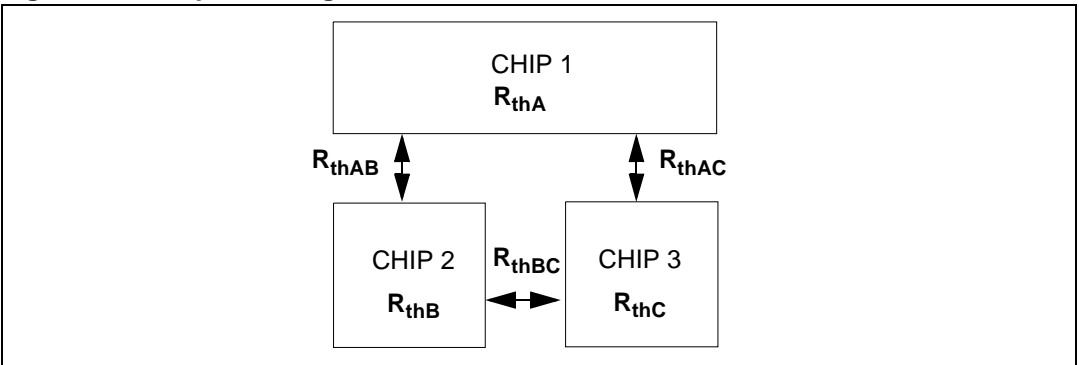
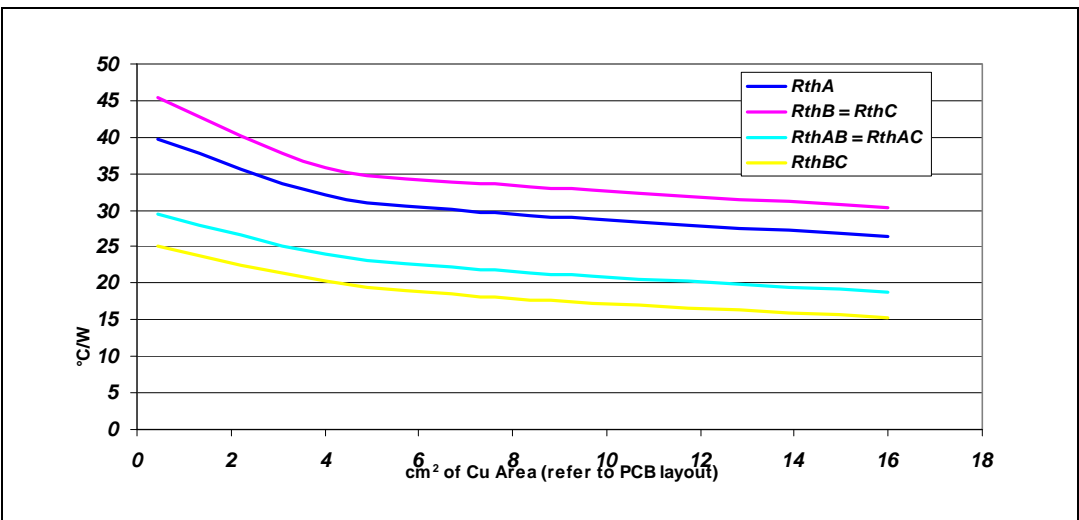


Figure 18. Auto and mutual $R_{thj-amb}$ vs PCB copper area in open box free air condition



3.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 17. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

| Chip 1 | Chip 2 | Chip 3 | Tjchip1 | Tjchip2 | Tjchip3 |
|--------|--------|--------|---|--|--|
| ON | OFF | ON | $P_{dchip1} \cdot R_{thA} + P_{dchip3} \cdot R_{thAC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + P_{dchip3} \cdot R_{thC} + T_{amb}$ |
| ON | ON | OFF | $P_{dchip1} \cdot R_{thA} + P_{dchip2} \cdot R_{thAB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + P_{dchip2} \cdot R_{thBC} + T_{amb}$ |
| ON | OFF | OFF | $P_{dchip1} \cdot R_{thA} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + T_{amb}$ | $P_{dchip1} \cdot R_{thAC} + T_{amb}$ |
| ON | ON | ON | $P_{dchip1} \cdot R_{thA} + (P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_{amb}$ | $P_{dchip2} \cdot R_{thB} + P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_{amb}$ | $P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_{amb}$ |

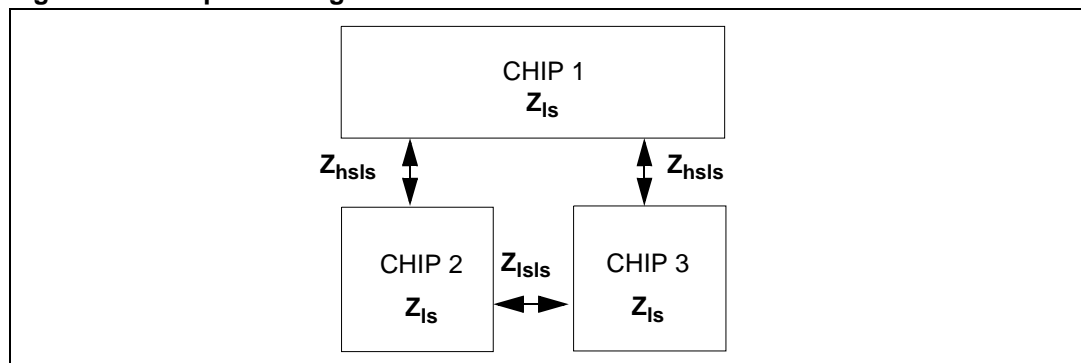
3.1.2 Thermal calculation in transient mode

$$T_{hs} = P_{dhs} \cdot Z_{hs} + Z_{hsIs} \cdot (P_{dIsA} + P_{dIsB}) + T_{amb}$$

$$T_{IsA} = P_{dIsA} \cdot Z_{Is} + P_{dhs} \cdot Z_{hsIs} + P_{dIsB} \cdot Z_{hsIs} + T_{amb}$$

$$T_{IsB} = P_{dIsB} \cdot Z_{Is} + P_{dhs} \cdot Z_{hsIs} + P_{dIsA} \cdot Z_{hsIs} + T_{amb}$$

Figure 19. Chipset configuration



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Figure 20. MultiPowerSO-30 HSD thermal impedance junction ambient single pulse

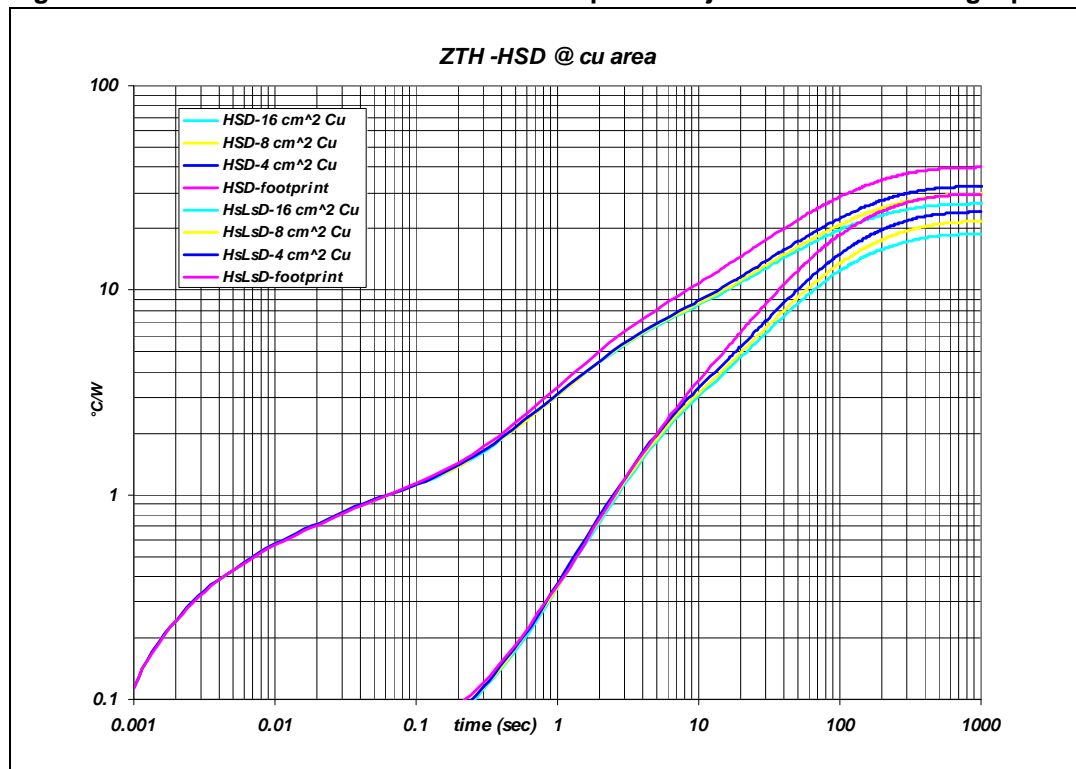


Figure 21. MultiPowerSO-30 LSD thermal impedance junction ambient single pulse

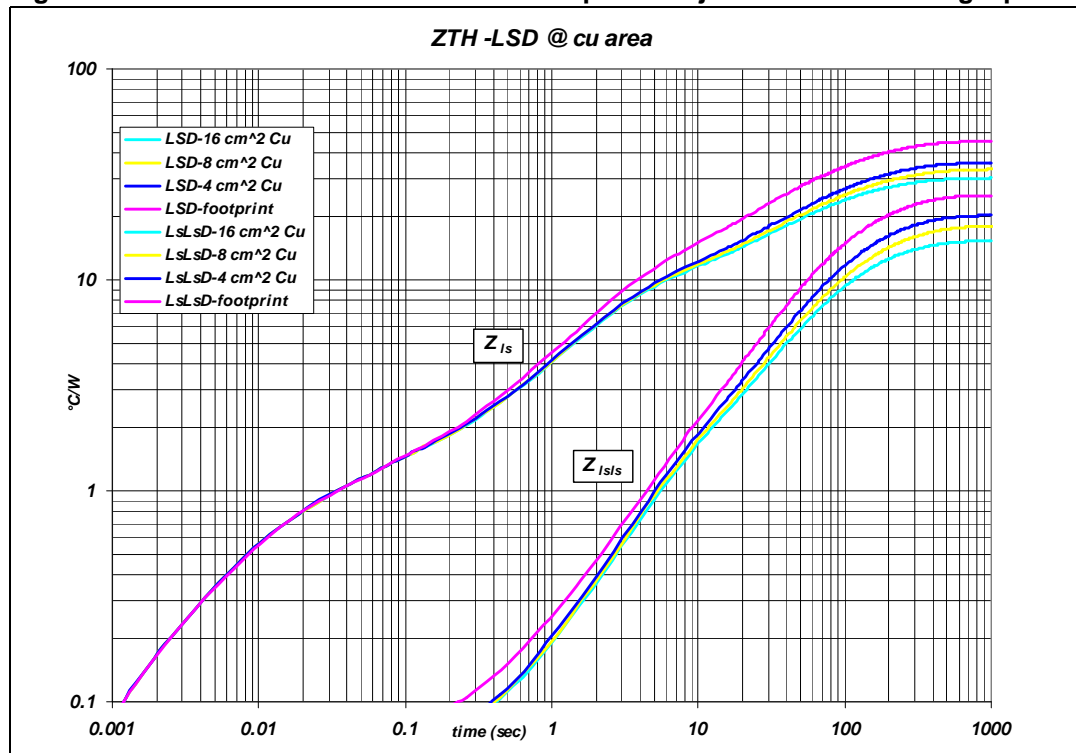
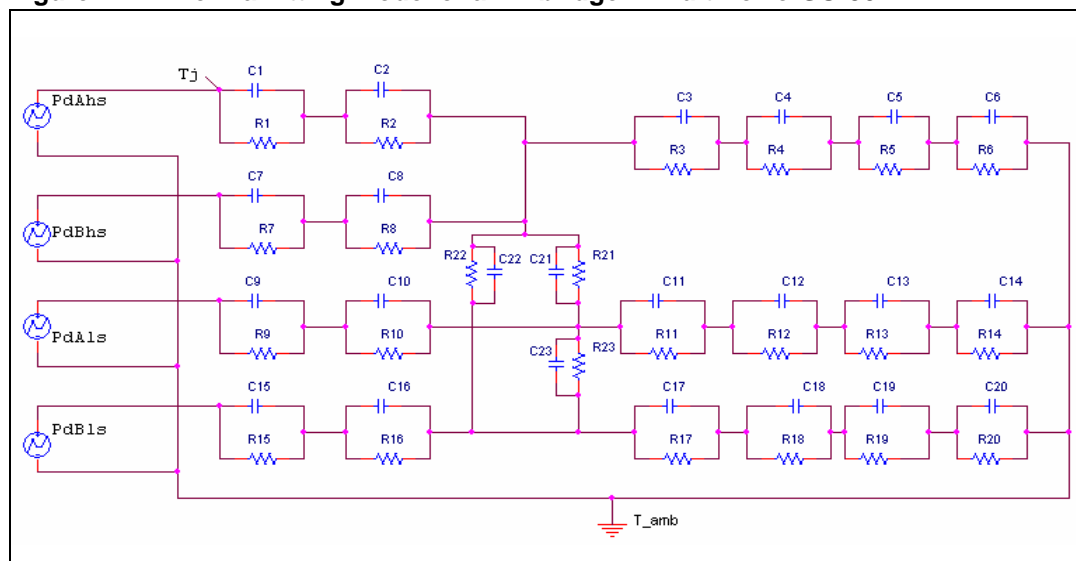


Figure 22. Thermal fitting model of an H-bridge in MultiPowerSO-30**Table 18. Thermal parameters⁽¹⁾**

| Area/island (cm ²) | Footprint | 4 | 8 | 16 |
|--------------------------------|-----------|-------|-------|-------|
| R1 = R7 (°C/W) | 0.1 | | | |
| R2 = R8 (°C/W) | 0.3 | | | |
| R3 = R10 = R16 (°C/W) | 0.5 | | | |
| R4 (°C/W) | 6 | | | |
| R5 (°C/W) | 30 | 24 | 24 | 24 |
| R6 (°C/W) | 56 | 52 | 42 | 32 |
| R9 = R15 (°C/W) | 0.05 | | | |
| R11 = R17 (°C/W) | 0.7 | | | |
| R12 = R18 (°C/W) | 10 | | | |
| R13 = R19 (°C/W) | 36 | 26 | 26 | 26 |
| R14 = R20 (°C/W) | 56 | 42 | 36 | 28 |
| R21 = R22 (°C/W) | 35 | 25 | 25 | 25 |
| R23 (°C/W) | 160 | 150 | 150 | 150 |
| C1 = C7 = C9 = C15 (W.s/°C) | 0.005 | | | |
| C2 = C8 (W.s/°C) | 0.01 | | | |
| C3 (W.s/°C) | 0.03 | | | |
| C4 (W.s/°C) | 0.4 | | | |
| C5 (W.s/°C) | 1.5 | 2 | 2 | 2 |
| C6 (W.s/°C) | 3 | 4 | 5 | 6 |
| C10 = C16 (W.s/°C) | 0.015 | | | |
| C11 = C17 (W.s/°C) | 0.05 | | | |
| C12 = C18 (W.s/°C) | 0.3 | | | |
| C13 = C19 (W.s/°C) | 1.2 | 2 | 2 | 2 |
| C14 = C20 (W.s/°C) | 2.5 | 3 | 4 | 5 |
| C21 = C22 = C23 (W.s/°C) | 0.01 | 0.008 | 0.008 | 0.008 |

1. The blank space means that the value is the same as the previous one.

4 Package and packing information

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 MultiPowerSO-30 mechanical data

Figure 23. MultiPowerSO-30 package dimensions

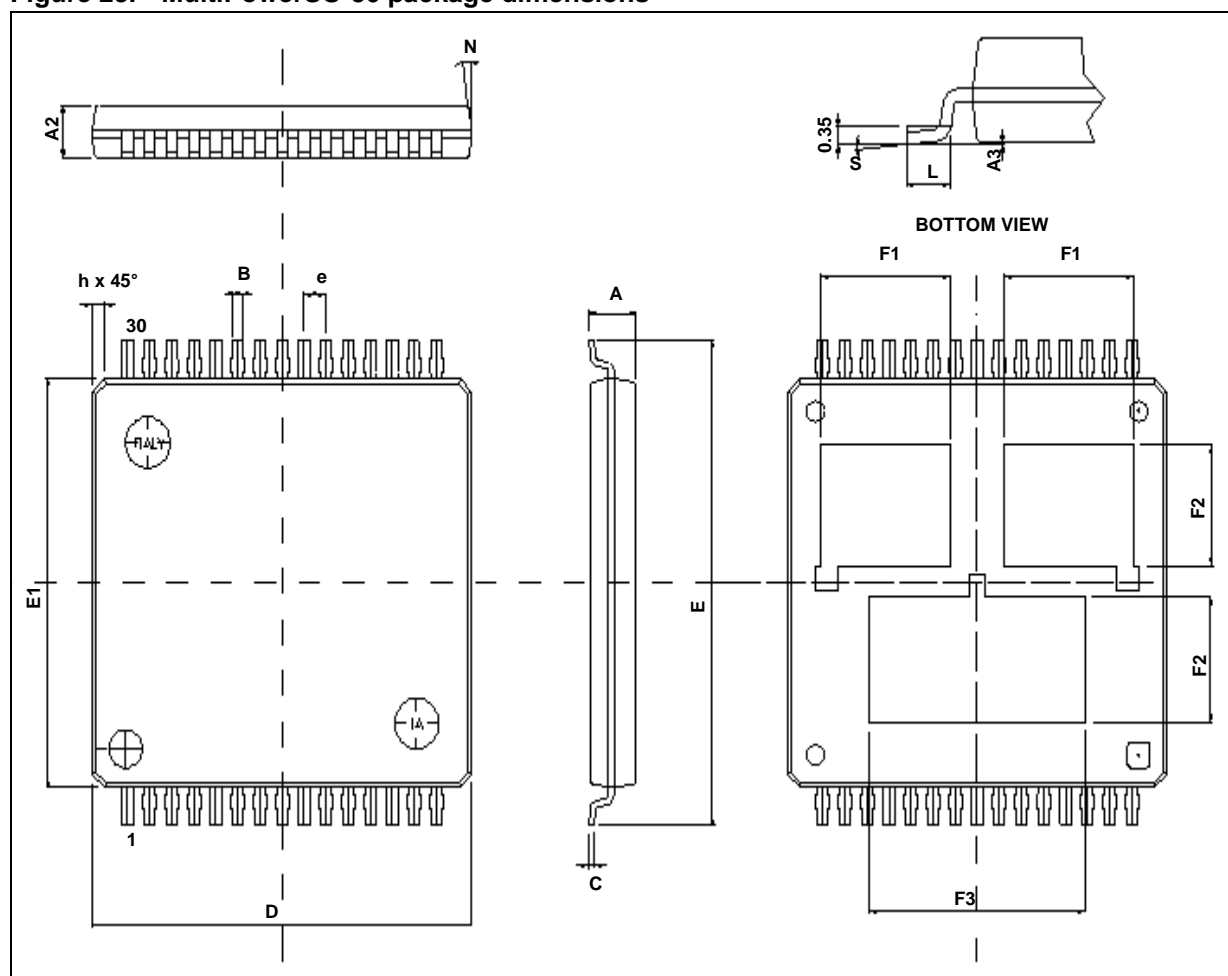
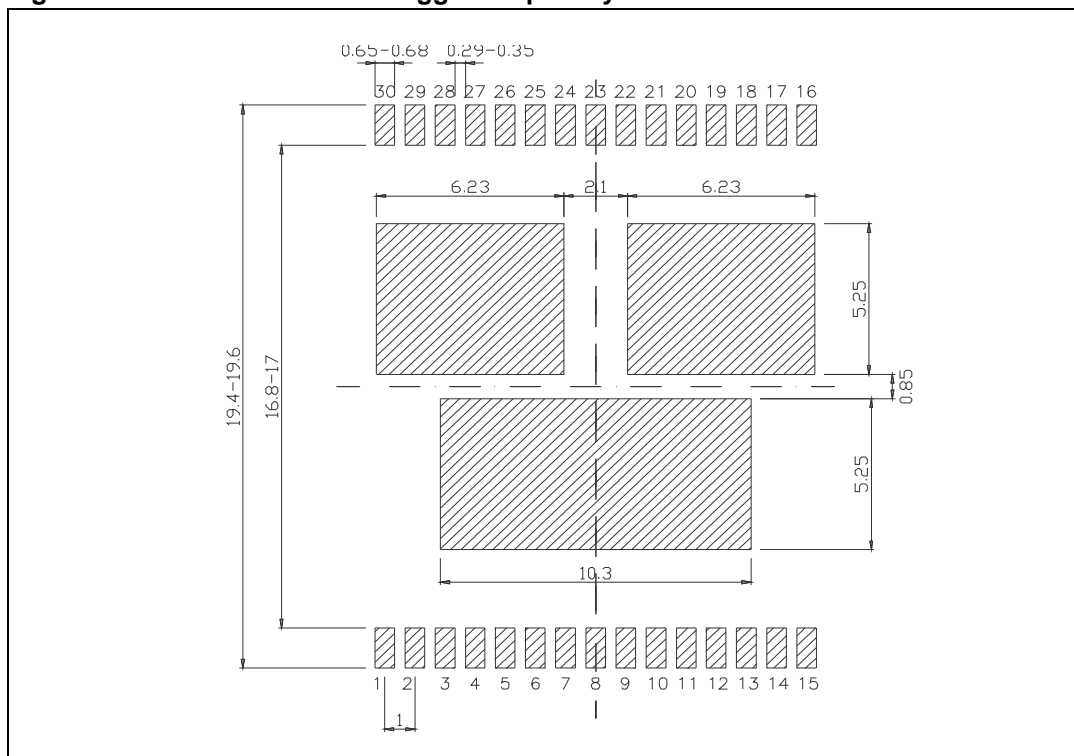


Table 19. MultiPowerSO-30 mechanical data

| Symbol | Data book mm | | |
|--------|--------------|------|-------|
| | Min. | Typ. | Max. |
| A | | | 2.35 |
| A2 | 1.85 | | 2.25 |
| A3 | 0 | | 0.1 |
| B | 0.42 | | 0.58 |
| C | 0.23 | | 0.32 |
| D | 17.1 | 17.2 | 17.3 |
| E | 18.85 | | 19.15 |
| E1 | 15.9 | 16 | 16.1 |
| e | | 1 | |
| F1 | 5.55 | | 6.05 |
| F2 | 4.6 | | 5.1 |
| F3 | 9.6 | | 10.1 |
| L | 0.8 | | 1.15 |
| N | | | 10° |
| S | 0° | | 7° |

4.3 MultiPowerSO-30 suggested land pattern

Figure 24. MultiPowerSO-30 suggested pad layout



4.4 MultiPowerSO-30 packing information

The devices can be packed in tube or tape and reel shipments (see [Table 20: Device summary](#) for packaging quantities).

Figure 25. MultiPowerSO-30 tube shipment (no suffix)

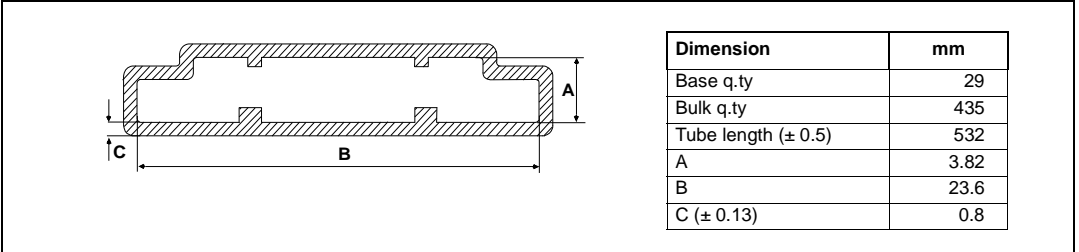
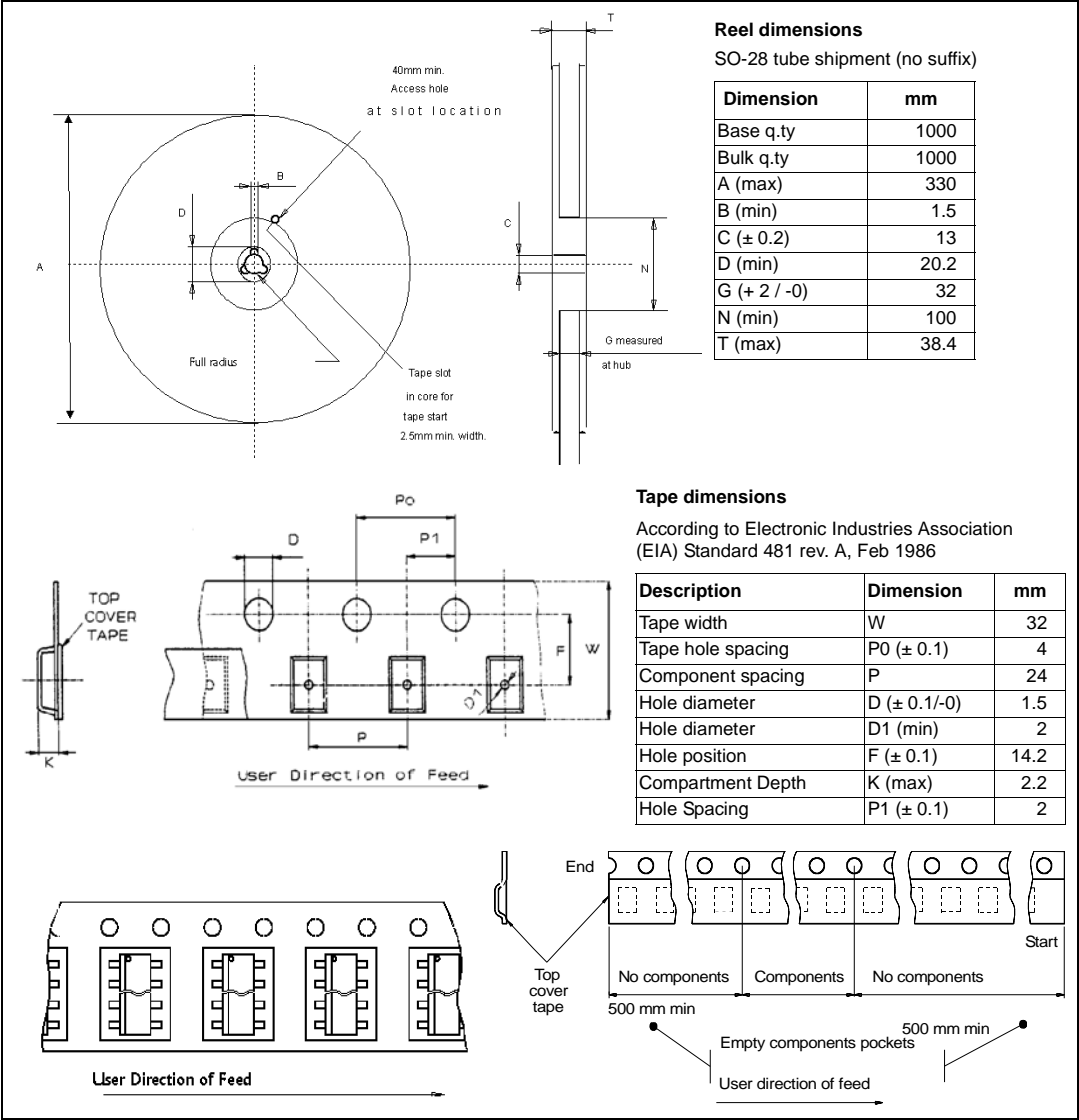


Figure 26. MultiPowerSO-30 tape and reel shipment (suffix “TR”)



5 Order codes

Table 20. Device summary

| Package | Order codes | |
|-----------------|-------------|---------------|
| | Tube | Tape and reel |
| MultiPowerSO-30 | VNH5019A-E | VNH5019TR-E |

6 Revision history

Table 21. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 22-Jan-2008 | 1 | Initial release. |
| 04-Nov-2009 | 2 | <p>Uploaded corporate template by using V3 version</p> <p>Added Table 5: Thermal data</p> <p>Section 2.1: Absolute maximum ratings</p> <ul style="list-style-type: none"> – Added text <p>Table 6: Power section</p> <ul style="list-style-type: none"> – I_S: added max value for $I_{N_A} = I_{N_B} = PWM = 0$; $T_j = 25\text{ }^{\circ}\text{C}$; $V_{CC}=13\text{ V}$ in Test conditions, deleted $I_{N_A} = I_{N_B} = PWM = 0$ – V_f: changed Test conditions, changed typ/max value – I_{RM}: deleted and copied in Table 8: Switching ($V_{CC} = 13\text{ V}$, $R_{LOAD} = 0.87\text{ W}$, $T_j = 25\text{ }^{\circ}\text{C}$) whole row <p>Table 8: Switching ($V_{CC} = 13\text{ V}$, $R_{LOAD} = 0.87\text{ W}$, $T_j = 25\text{ }^{\circ}\text{C}$)</p> <ul style="list-style-type: none"> – t_{DEL}: changed min/typ/max value – Copied I_{RM} row by Table 6: Power section <p>Updated Table 10: Current sense ($8\text{ V} < V_{CC} < 21\text{ V}$)</p> <p>Table 11: Charge pump</p> <ul style="list-style-type: none"> – V_{CP}: changed min/max value for $EN_X = 5\text{ V}$, changed typ value for $EN_X = 5\text{ V}$, $V_{CC} = 4.5\text{ V}$ <p>Updated Figure 11: Waveforms in full bridge operation (part 1)</p> <p>Updated Figure 12: Waveforms in full bridge operation (part 2)</p> <p>Added Chapter 4</p> |
| 16-Dec-2009 | 3 | <p>Updated following tables:</p> <ul style="list-style-type: none"> – Table 6: Power section – Table 9: Protection and diagnostic – Table 10: Current sense ($8\text{ V} < V_{CC} < 21\text{ V}$) <p>Added Figure 6: Behavior in fault condition (how a fault can be cleared)</p> <p>Added Chapter 3: Package and PCB thermal data</p> |
| 06-Apr-2010 | 4 | <p>Updated Table 5: Thermal data.</p> <p>Table 6: Power section:</p> <ul style="list-style-type: none"> – I_S: updated test condition and max value <p>Updated table notes on Table 9: Protection and diagnostic.</p> <p>Table 10: Current sense ($8\text{ V} < V_{CC} < 21\text{ V}$):</p> <ul style="list-style-type: none"> – dK_0/k_0, dK_1/k_1, dK_3/k_3: updated minimum end maximum values. |
| 19-Apr-2010 | 5 | Updated Table 10: Current sense ($8\text{ V} < V_{CC} < 21\text{ V}$) . |
| 25-May-2010 | 6 | <p>Updated Features list.</p> <p>Updated Table 6: Power section.</p> |
| 02-Sep-2010 | 7 | Updated Table 5: Thermal data . |

Table 21. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 22-Dec-2011 | 8 | <p>Updated Figure 1: Block diagram</p> <p>Added Table 1: Suggested connections for unused and not connected pins</p> <p>Updated Table 3: Block descriptions</p> <p>Table 8: Switching ($V_{CC} = 13\text{ V}$, $R_{LOAD} = 0.87\text{ W}$, $T_j = 25\text{ °C}$):</p> <ul style="list-style-type: none"> – T_{TSD}, T_{TR}, T_{HYST}: added note – T_{TSD_LS}: added row <p>Updated Table 13: Truth table in fault conditions (detected on OUTA)</p> <p>Updated Figure 11: Waveforms in full bridge operation (part 1) and Figure 12: Waveforms in full bridge operation (part 2)</p> |
| 19-Sep-2013 | 9 | Updated Disclaimer. |

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