Middle East Technical University | Department of Computer Engineering

CENG 232

Logic Design

Spring 2020-2021

Lab 1

Due date: 14 April 2021, Wednesday, 23:55
No late submissions

1 Introduction

This laboratory aims to get you familiar with basic logic gates and combinational circuit design. You will simplify the circuit that is explained below and draw the circuit using the Logisim tool with the given gates.

2 IC Pool

In this LAB, you will use the following gates to build the circuit:

- 74LS04 (Inverter)
- 74LS08 (AND)
- 74LS32 (OR)

Note that you can use **only** the given gates. Usage of other gates is **NOT** allowed.

3 Lab Work

In this assignment, you are expected to perform the operations described in the following section.

3.1 Specifications

Suppose A and B are 2-bit binary **input** numbers and X, Y and Z are 1-bit binary **output** numbers. A and B are represented with A_1, A_0, B_1 and B_0 bits respectively where A_1 and B_1 are the most significant bits and A_0 and B_0 are the least significant bits of the relevant number. Your circuit will take A and B

as inputs and generate the outputs X,Y and Z with the following instructions:

$$\mathbf{X} = \begin{cases} 1 & A - B < -1 \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Y} = \begin{cases} 1 & \text{A/B is defined and an integer} \\ 0 & \text{otherwise} \end{cases}$$

$$\mathbf{Z} = \begin{cases} 1 & ((\text{A} \ll \text{B}) + (\text{B} \ll \text{A})) * ((\text{A} + 1) \gg \text{B}) + (\text{B} \gg \text{A}) >= 3 \\ 0 & \text{otherwise} \end{cases}$$

You have to use "input pins" and "output pins" for your inputs and outputs, respectively, from the Toolbar at the top of Logisim. Set their labels correctly using the following names:

Input pins: A1, A0, B1, B0.
Output pins: X, Y, Z.

Please, only set "label" property of the "pin" objects, do not add a "label" object onto the Logisim canvas.

Each pin corresponds to a digit in a 2-bit binary number. If it is set, then the value of the digit is 1 if reset, then the value of the digit is 0. Note that $\gg$ and $\ll$ are logical right and left shift operators respectively. For instance (4=0b100, 2=0b10) $4 \gg 1$ corresponds to shifting the bits of value 4 one step to right and results in 0b010. Similarly, $2 \ll 2$ operation shifts the bits of value 2 two steps to left, which yields 8=0b1000.

We highly recommend you simplify your circuitry as much as possible (via the techniques covered in the lectures) for ease of implementation. If the pandemic measure weren't in effect, you would be supposed to implement your design on breadboards, and the number of ICs that you'd purchase would be limited, hence it would be inevitable to simplify your circuits.

3.2 Input Output Examples

1. Suppose $A_1A_0 = 00$ and $B_1B_0 = 10$. In this case, A=0 and B=2 in decimal.
   $A - B = -2$
   Since $A - B < -1$, the output X is 1.

2. Suppose $A_1A_0 = 10$ and $B_1B_0 = 01$. In this case, A=2 and B=1 in decimal.
   $A - B = 1$
   Since $A - B < -1$ does not hold, the output X is 0.

3. Suppose $A_1A_0 = 01$ and $B_1B_0 = 01$. In this case, A=1 and B=1 in decimal.
   $A/B = 1$
   Since A/B is defined and an integer, the output Y is 1.

4. Suppose $A_1A_0 = 01$ and $B_1B_0 = 10$. In this case, A=1 and B=2 in decimal.
   $A/B = 0.5$
   Since A/B is not an integer, the output Y is 0.

5. Suppose $A_1A_0 = 01$ and $B_1B_0 = 10$. In this case, A=1 and B=2 in decimal.
   $A \ll B = 4$, $B \ll A = 4$, $(\text{A}+1) \gg \text{B} = 0$, $\text{B} \gg \text{A} = 1$
   $((\text{A} \ll \text{B}) + (\text{B} \ll \text{A})) * ((\text{A} + 1) \gg \text{B}) + (\text{B} \gg \text{A}) = 1$
   Since $((\text{A} \ll \text{B}) + (\text{B} \ll \text{A})) * ((\text{A} + 1) \gg \text{B}) + (\text{B} \gg \text{A}) >= 3$ does not hold, the output Z is 0.

6. Suppose $A_1A_0 = 01$ and $B_1B_0 = 01$. In this case, A=1 and B=1 in decimal.
   $A \ll B = 2$, $B \ll A = 2$, (A+1) $\gg$ B = 1, B $\gg$ A = 0
   $((\text{A} \ll \text{B}) + (\text{B} \ll \text{A})) * ((\text{A} + 1) \gg \text{B}) + (\text{B} \gg \text{A}) = 4$
   Since $((\text{A} \ll \text{B}) + (\text{B} \ll \text{A})) * ((\text{A} + 1) \gg \text{B}) + (\text{B} \gg \text{A}) >= 3$ holds, the output Z is 1.

4 Deliverables

1. Submit the circuit named `e1234567.circ` prepared in Logisim, until the specified deadline. Do not forget to replace `e1234567` with your 7-digit student ID. The evaluation of the submission will be a black-box test. **You should use CENG version of Logisim which is available on ODTUClass course page. Circuits designed with other Logisim versions, other tools or not named properly will not be graded!**

5 Cheating Policy

All the lab work should be **individual** and there is a policy of zero tolerance for cheating. See the course website for further information about cheating policy.

6 References

CENG Logism Version.