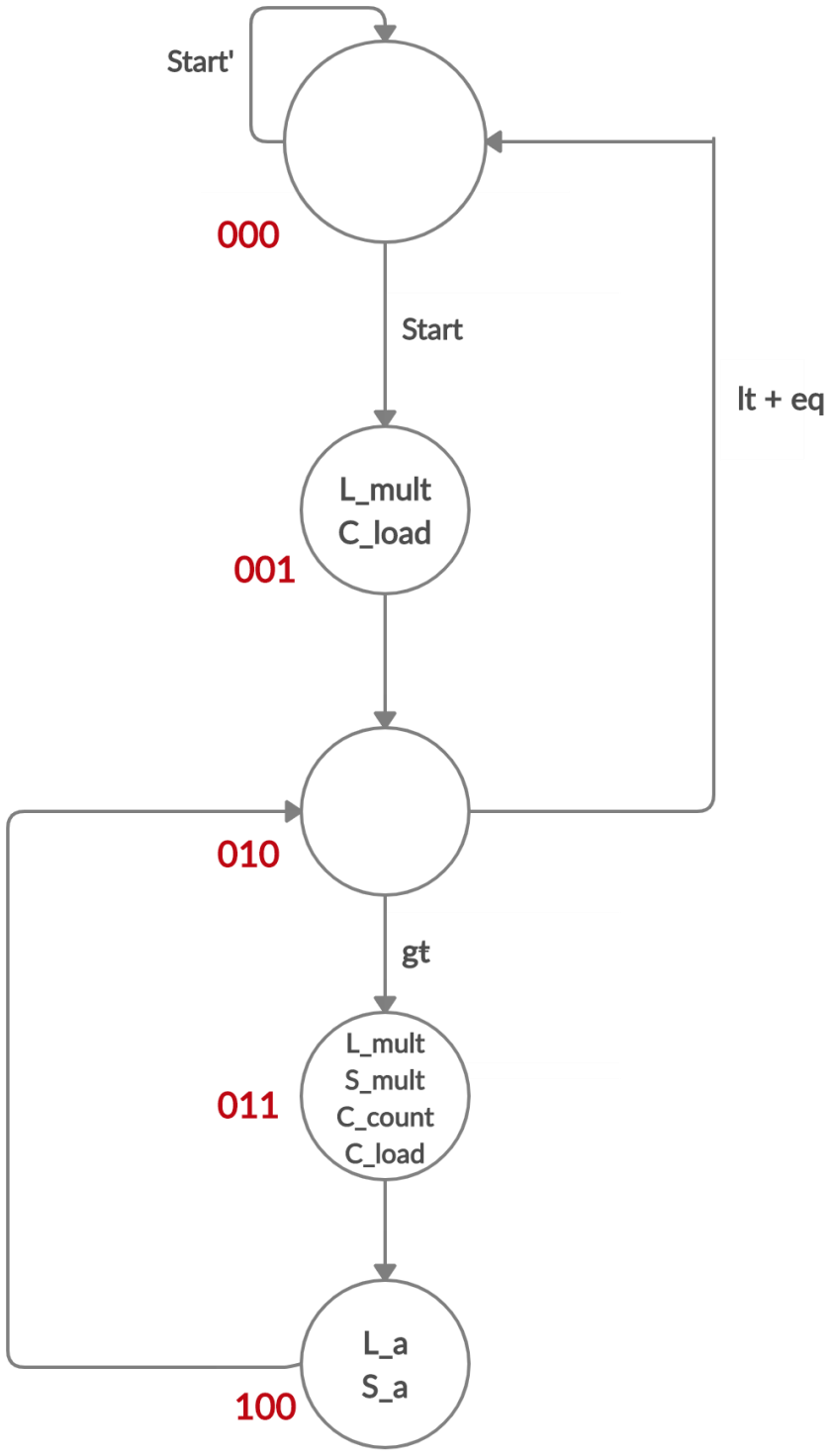
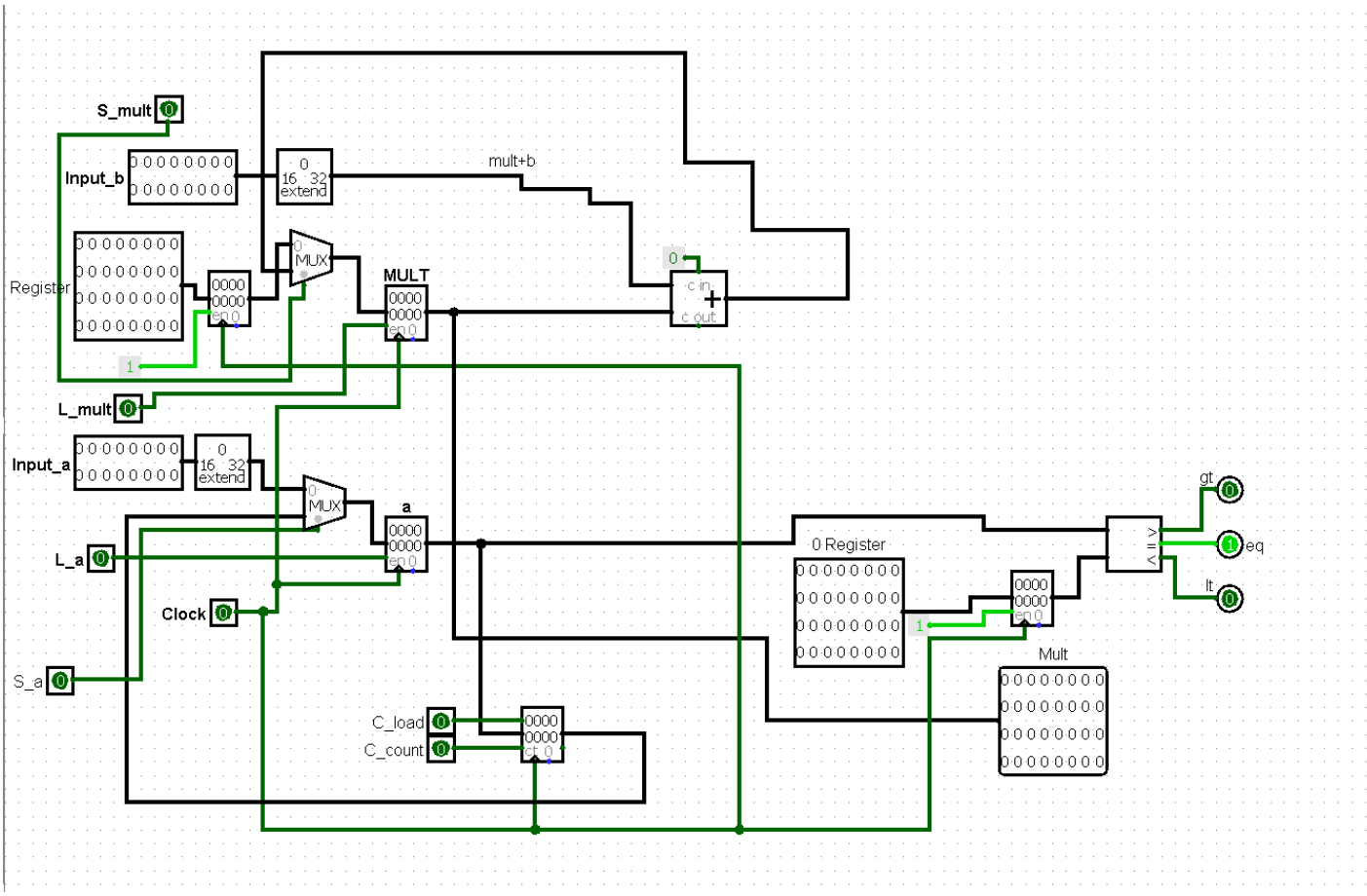
Report

State Diagram



Datapath


S_mult
Input_b
0
16 32
extend
mult+b
Register
MUX
MULT
0000
0000
en 0
0
c in
c out
1
L_mult
Input_a
a
L_a
Clock
S_a
C_load
C_count
0 Register
Mult
gt
eq
lt

Truth Tables

Inputs							Outputs		
S2	S1	S0	lt	gt	eq	Start	N2	N1	N0
0	0	0	-	-	-	0	0	0	0
0	0	0	-	-	-	1	0	0	1
0	0	1	-	-	-	-	0	1	0
0	1	0	1	0	0	-	0	0	0
0	1	0	0	1	0	-	0	1	1
0	1	0	0	0	1	-	0	0	0
0	1	1	-	-	-	-	1	0	0
1	0	0	-	-	-	-	0	1	0

Inputs			Outputs					
S2	S1	S0	L_mult	S_mult	L_a	C_load	S_a	C_count
0	0	0	0	0	1	0	0	0
0	0	1	1	0	0	1	0	0
0	1	0	0	0	0	0	0	0
0	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	0

Boolean Equations

N2 = S2’S1S0

N1 = S2’S1’S0 + S2’S1S0’Lt’gtEq’ +S2S1’S0’

N0 = S2’S1’S0’Start + S2’S1S0’Lt’gtEq’

L_mult = S2’S1’S0 + S2’S1S0 = S2’S0(S1’+S1) = S2’S0

S_mult = S2’S1S0

L_a = S2’S1’S0’ + S2S1’S0’

S_a = S2S1’S0’

C_count = S2’S1S0

C_load = S2’S1’S0 + S2’S1S0

Note: My circuit only works for positive A and B

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