GEBZE TECHNICAL UNIVERSITY
ELECTRONICS ENGINEERING
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ELM 237
ELECTRONICS LABORATORY 1

LAB 5 EXPERIMENT REPORT
MOSFET Measurement and Applications

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What is MOSFET?

A MOSFET is a four-terminal device having source(S), gate (G), drain (D) and body (B) terminals. In general, The body of the MOSFET is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor. MOSFET is generally considered as a transistor and employed in both the analog and digital circuits. This is the basic **introduction to MOSFET**. And the general structure of this device is as below :

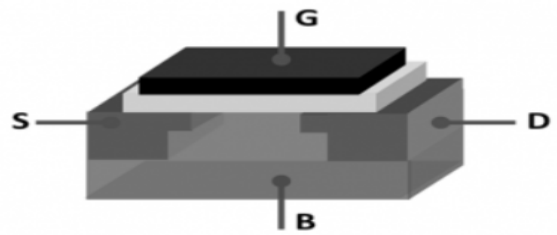
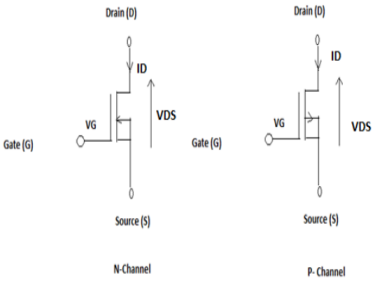


FIGURE 1: MOSFET

From the above **MOSFET structure**, the functionality of MOSFET depends on the electrical variations happening in the channel width along with the flow of carriers (either holes or electrons). The charge carriers enter into the channel through the source terminal and exit via the drain.
A MOSFET can function in two ways= Depletion Mode , Enhancement Mode.

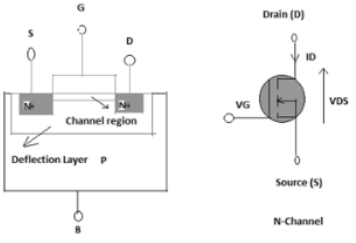


Depletion Mode

When there is no voltage across the gate terminal, the channel shows its maximum conductance. Whereas when the voltage across the gate terminal is either positive or negative, then the channel conductivity decreases.

Enhancement Mode

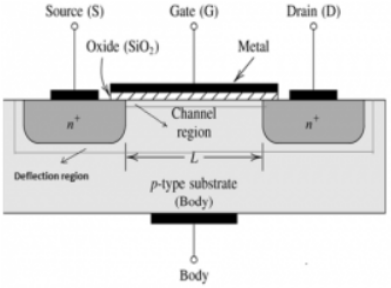
When there is no voltage across the gate terminal, then the device does not conduct. When there is the maximum voltage across the gate terminal, then the device shows enhanced conductivity.



Enhancement Mode

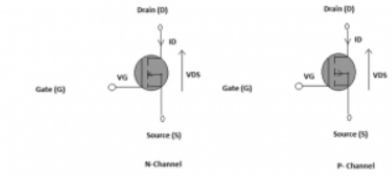
Working Principle of MOSFET

The main principle of the MOSFET device is to be able to control the voltage and current flow between the source and drain terminals. It works almost like a switch and the functionality of the device is based on the MOS capacitor. The MOS capacitor is the main part of MOSFET.



MOSFET Block Diagram

P-Channel MOSFET

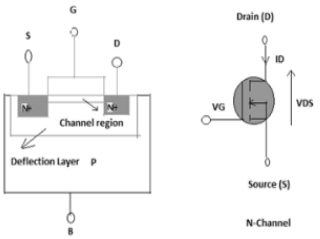


Depletion Mode P Channel

The P- channel MOSFET has a P- Channel region located in between the source and drain terminals. It is a four-terminal device having the terminals as gate, drain, source, and body. The drain and source are heavily doped p+ region and the body or substrate is of n-type. The flow of current is in the direction of positively charged holes.

N- Channel MOSFET

The N-Channel MOSFET has an N- channel region located in between the source and drain terminals. It is a four-terminal device having the terminals as gate, drain, source, body. In this type of Field Effect Transistor, the drain and source are heavily doped n+ region and the substrate or body are of P-type.



Enhancement Mode N Channel

MOSFET Regions of Operation

To the most general scenario, the operation of this device happens mainly in three regions and those are as follows: **Cut-off Region –** It is the region where the device will be in the OFF condition and there zero amount of current flow through it. Here, the device functions as a basic switch and is so employed as when they are necessary to operate as electrical switches. **Saturation Region –** In this region, the devices will have their drain to source current value as constant without considering the enhancement in the voltage across the drain to source. This happens only once when the voltage across the drain to source terminal increases more than the pinch-off voltage value. In this scenario, the device functions as a closed switch where a saturated level of current across the drain to source terminals flows. Due to this, the saturation region is selected when the devices are supposed to perform switching. **Linear/Ohmic Region –** It is the region where the current across the drain to source terminal enhances with the increment in the voltage across the drain to source path. When the MOSFET devices function in this linear region, they perform amplifier functionality.

1.1 Measuring Device Thresholds:

A new method for extracting the threshold voltage of MOSFETs is presented. The threshold voltage is the gate voltage at which the second difference of the logarithm of the drain current takes a minimum value. The threshold voltage characteristics are compared with ones measured with previous methods and it is shown that the proposed method overcomes previous problems.

1.1 Measuring Device Thresholds:

a) Selecting pin #1 as source terminal (a PMOS device), assemble the circuit shown in Figure 2. Ensure both substrate pins are connected. Use 10 V as supply. Measure the voltage from A to ground (V_A). Estimate V_{tp}.

Figure 1: Layout of 4007 MOS array.

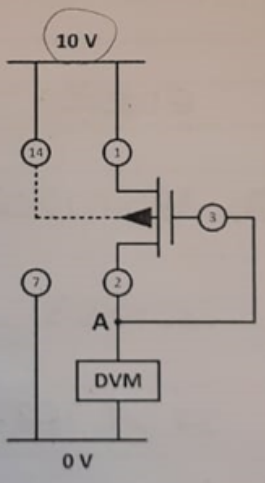
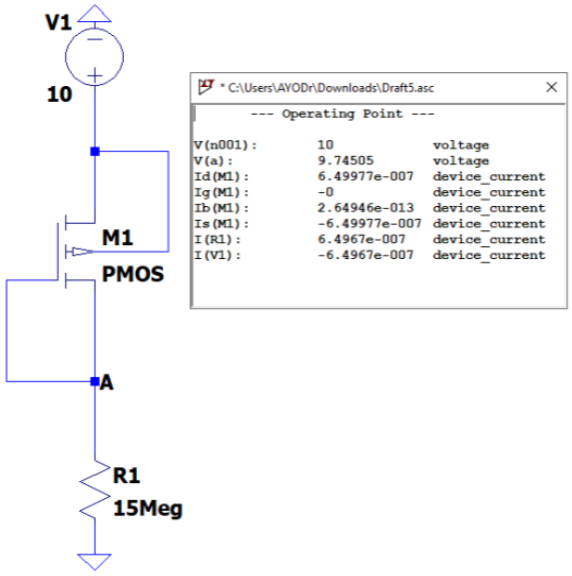


Figure 2: Setup to measure

b) Repeat the measurement with drain and source interchanged: Use pin #2 as source terminal.

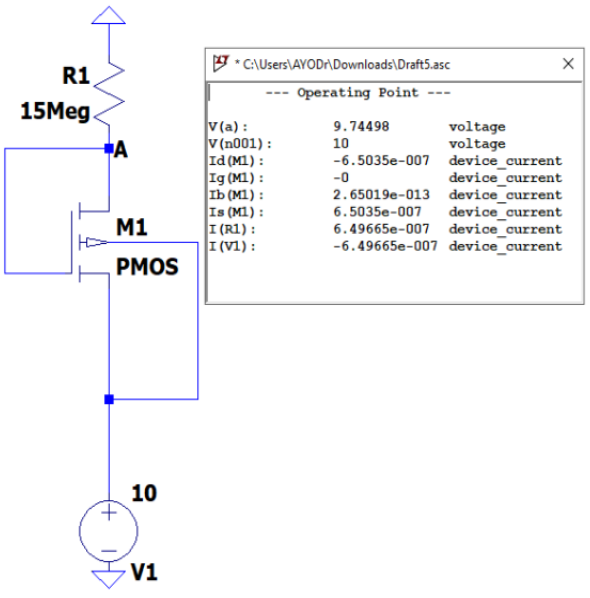
Table 1. DC voltage measurements and threshold voltage estimations of single transistor.

Pin # as Source	V_A	V_{tp}
#1 (a)	9.7	0.3
#2 (b)	9.7	0.3



After the necessary measurements were made, the following results were obtained. Even if the pin on which we measure and the gate, drain and source pins change, the results are the same. This result was obtained as a result of using the same mosfet. Minor differences may be caused by human error. We set up the circuits by always giving the seventh and fourteenth pins the lowest voltage and the highest voltage. We have obtained similar results even when the 2nd pin is taken as the source terminal. In other words, we have observed that nothing has changed in the measurement between the pins.We re-installed the same circuit over the LtSpice program to check if we got the right result. By replacing the DVM with 15meg, the high resistance in the voltmeter, which is actually there, is achieved. It has been observed that the results are close to each other.

By re-establishing the desired pin change circuit over the LtSpice program, we have observed that there is no change between the pins. Thus, it was certain that correct results were obtained both in the electronic environment and in the experimental environment.

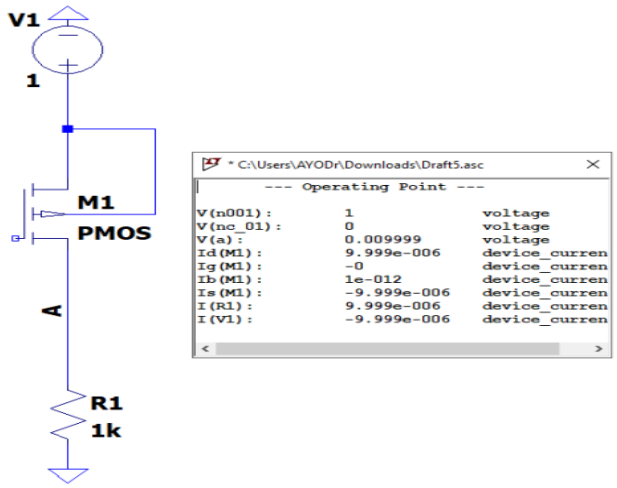


1.1c: We continued the circuit in figure two. By connecting a 1k resistor to A node, we disconnected the gate-drain and connected an adjustable voltage source to the gate. We increased the gate voltage by 0.2 volts, allowing it to be adjusted carefully and slowly. We made an ID calculation by noting the values we received. We determined the Vtp value with the ID value exceeding 10µA and noted the necessary values in the table.

c) Start with the configuration in Figure 2. Shunt node A to ground with a 1 kΩ resistor (note down its exact value). Break the gate-drain connection and connect the gate to an adjustable voltage source. Carefully and slowly adjust the gate voltage so that the V_{SG} is swept through the values given in the table below. Note V_A and calculate I_D. Estimate V_{tp} as the voltage allowing a $I_D > 10$ µA for this technology.

Table 2. DC voltage measurements, current calculations and threshold voltage estimations with different source-to-gate voltages.

V_{SG} (V)	0.0	0.2	0.4	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	V_{tp}
V_A	0.1 mV	0.20	0.15	3.3 mV	29.54 mV	120.80 mV	241.12 mV	0.402 V	0.67 V	0.80 V	1.04 V	1.33 V	1.62 V	0.8 V
I_D	0.1 µA	0.20 µA	0.15 µA	3.3 µA	29.54 µA	110.83 µA	241.12 µA	0.402 mA	0.67 mA	0.80 mA	1.04 mA	1.37 mA	1.62 mA	3µA

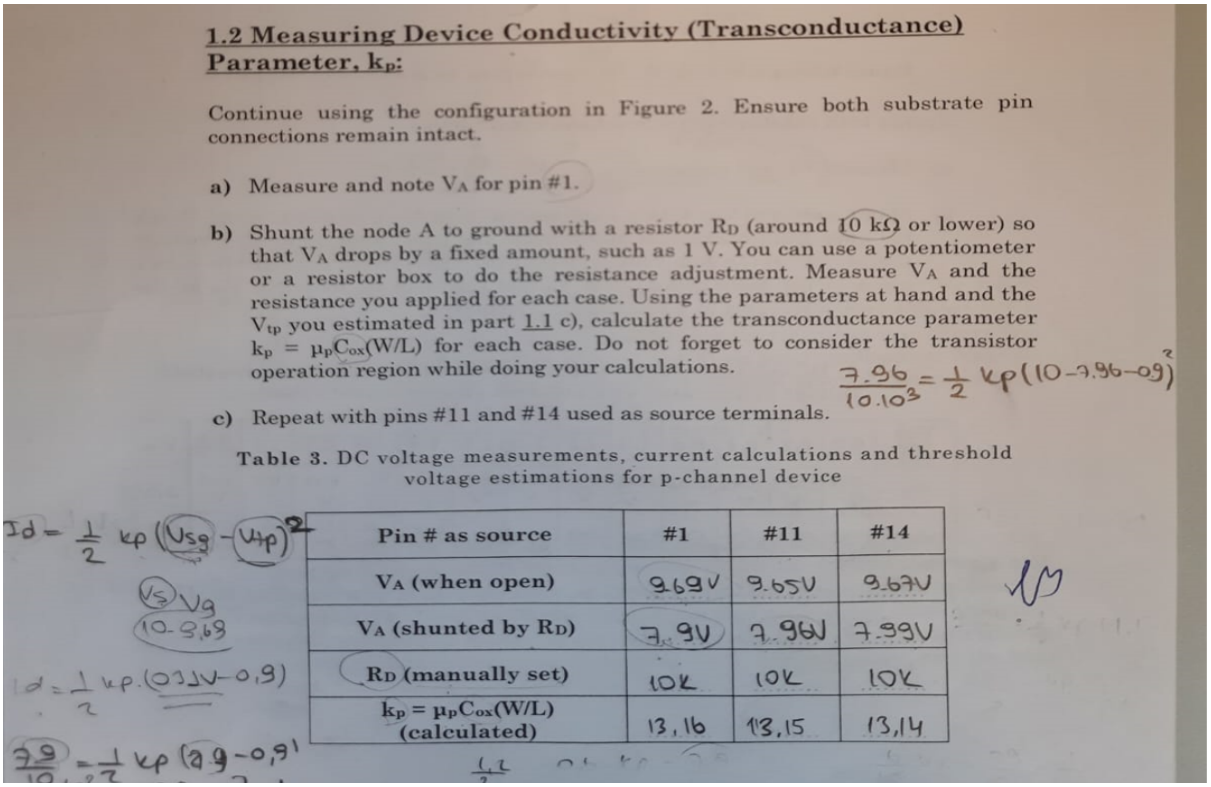


Whether the transistor is on or off is determined by the value of the voltage applied to the GATE pin. In N channel type mosfets, when the high voltage transistor applied to the GATE leg is opened, the transistor closes when the GATE is turned to minus state. When the GATE pin is connected to negative, no current flows through the transistor. As a higher voltage passes through the GATE, the transistor opens and current is allowed to flow. The opposite is true for the P type mosfet. As the voltage applied to the GATE leg approaches zero, the P-type MOSFET turns on.

We observed that the p-type mosfet current flows as the voltage value applied to the GATE gate decreases. Thus, a circuit measurement was made in accordance with the rules. Since the current passes through a 1k resistor, we obtained the voltage value we measured by dividing it by 1000. We noted the voltage at the limit value and the current value in the table.

We re-established the same circuit by disconnecting the necessary gate-drain connection in the LtSpice program. This time we set the GATE voltage value to 1 V as we wanted to show the desired 10µA value in the program. In the experimental environment, we obtained this value as 0.9V. These values, which are very close to each other, show that we did the experiment correctly. Errors arising from the experimental environment can be shown for the difference.

1.2 Measuring Device Conductivity (Transconductance) Parameter, kp:



1.2 Measuring Device Conductivity (Transconductance) Parameter, k_p:

Continue using the configuration in Figure 2. Ensure both substrate pin connections remain intact.

a) Measure and note V_A for pin #1.

b) Shunt the node A to ground with a resistor R_D (around 10 kΩ or lower) so that V_A drops by a fixed amount, such as 1 V. You can use a potentiometer or a resistor box to do the resistance adjustment. Measure V_A and the resistance you applied for each case. Using the parameters at hand and the V_{tp} you estimated in part 1.1 c), calculate the transconductance parameter $k_p = \mu_p C_{ox}(W/L)$ for each case. Do not forget to consider the transistor operation region while doing your calculations.

c) Repeat with pins #11 and #14 used as source terminals.

Table 3. DC voltage measurements, current calculations and threshold voltage estimations for p-channel device

Pin # as source	#1	#11	#14
V_A (when open)	9.69V	9.65V	9.67V
V_A (shunted by R_D)	7.9V	7.96V	7.99V
R_D (manually set)	10K	10K	10K
$k_p = \mu_p C_{ox}(W/L)$ (calculated)	13,16	13,15	13,14

$$I_d = \frac{K}{2}(V_{gs} - V_t)^2 \text{ where } K = \mu C_{ox}\frac{W}{L}$$

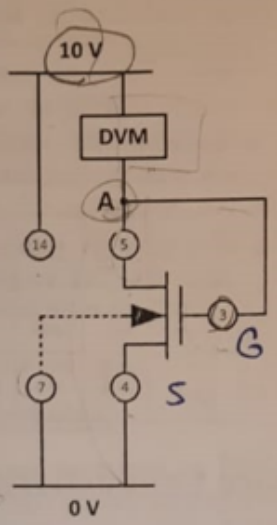
Kp is the transconductance of the MOSFET. This determines the drain current that flows for a given gate source voltage. We have reached the Kp parameter by using the formula on the left.

The circuit in figure two continued to be used. Va value measured for pin #1. A 10kΩ resistor is connected to reduce Va by 1V. Using the estimated Vtp value in section 1.1.c, the Kp value was calculated in accordance with the above formula. Calculations were made manually and added to the report. Afterwards, the same operations were repeated for pins #11 and #14. It was observed whether there was a difference between them. The point to be noted here was to note that pin #14 already has high voltage. Gate-drain-source resources are properly connected. As a result of the calculations, it was observed that the Kp values, which should be the same due to the fact that the same mosfet is used, are slightly different from each other. The Kp value is a MOSFET specific value. It is seen that the differences are due to measurement and calculation errors.

1.3 Measuring n Channel Device Parameters

1.3 Measuring n Channel Device Parameters:

Selecting pin #4 as source terminal (an NMOS device), assemble the circuit shown in Figure 3.



$V_{GS} \leq V_{tn}$

Figure 3: Setup to measure V_{tn}. Pin numbers given are in accordance with part a).

Ensure both substrate pin connections remain intact.

a) Measure V_A, and estimate V_{tn}. 10 − 9.37 =

b) Shunt node A to V_{DD} with a 1 kΩ resistor (note down its exact value). Break the gate-drain connection and connect the gate to an adjustable voltage source. Adjust the gate voltage so that the V_{GS} is swept through the values given in the table below. Note V_A and calculate I_D. Estimate V_{tn} as the voltage allowing a $I_D > 10$ µA for this technology.

Table 4. DC voltage measurements, current calculations and threshold voltage estimations with different gate-to-source voltages.

V_{GS} (V)	0.0	0.2	0.4	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	V_{tn}
V_A	10.052 V	10.052 V	10.052 V	10.052 V	10.051 V	10.051 V	10.036 V	9.994 V	9.93 V	9.82 V	9.77 V	9.60 V	9.43 V	1.5V
I_D	0	0	0	0	1 µA	1 µA	1.6 µA	58 µA	122 µA	238 µA	282 µA	452 µA	578 µA	30 µA

In a MOSFET, the drain leg is connected to the load, the Source leg is connected to the power source, the Gate leg is controlling the transistor. In N type mosfets, the high voltage applied to the GATE leg opens the transistor, while the low voltage applied makes the transistor closed. Considering this situation, the Vgs value was carefully changed thanks to the regulated voltage connected to the GATE leg, and the results were written in the report. The table is filled after the gate-drain is disconnected and the relevant resistor is connected. After the currents were calculated by considering the resistance value again, the Vtn value was selected in accordance with the 10µA criterion given in the condition and written in the report in a regular way.

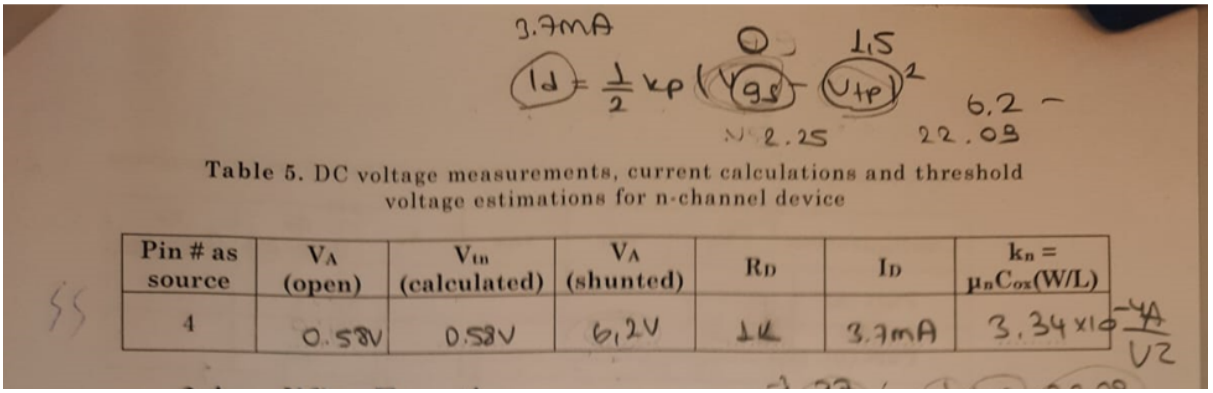


Table 5. DC voltage measurements, current calculations and threshold voltage estimations for n-channel device

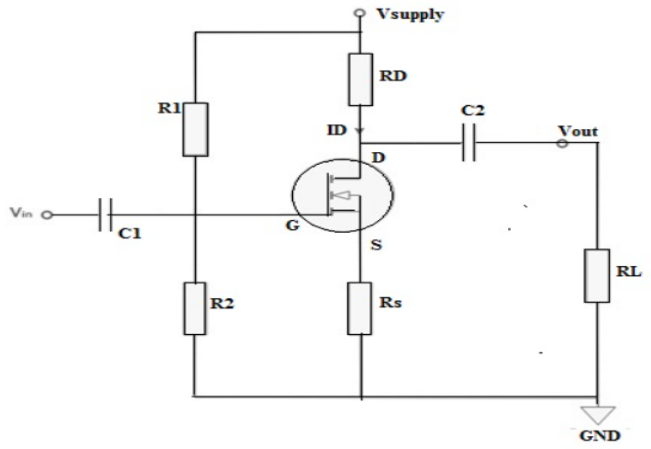
Pin # as source	V_A (open)	V_{tn} (calculated)	V_A (shunted)	R_D	I_D	$k_n = \mu_n C_{ox}(W/L)$
4	0.58V	0.58V	6.2V	1K	3.7mA	$3.34 \times 10^{-4} \frac{A}{V2}$

$$I_d = \frac{K}{2}(V_{gs} - V_t)^2 \text{ where } K = \mu C_{ox}\frac{W}{L}$$

The circuit in figure three has been returned. A 1 kΩ resistor is connected to node A. We measured the value of Va and the resistance we applied. We re-used the Kp formula we used earlier to calculate the Kp value.

2. Amplifier Function

In the MOSFET amplifier, a small change within gate voltage will generate a large change within drain current like in JFET. So, MOSFET will increase a weak signal's strength; consequently, it acts as an amplifier.



Biasing Circuit of MOSFET Amplifier

-MOSFET Amplifier Working

A complete MOSFET amplifier circuit can be designed by including a source, drain, load resistor & coupling capacities to the above circuit. The biasing circuit of the MOSFET amplifier is shown left.

Since we could not train the circuit given above during the experiment, we tried to get the results in electronic environment. We added the outputs we obtained to the report. We set up the circuit indicated in Figure 4.

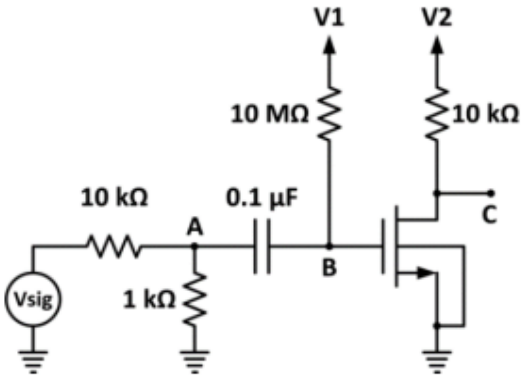
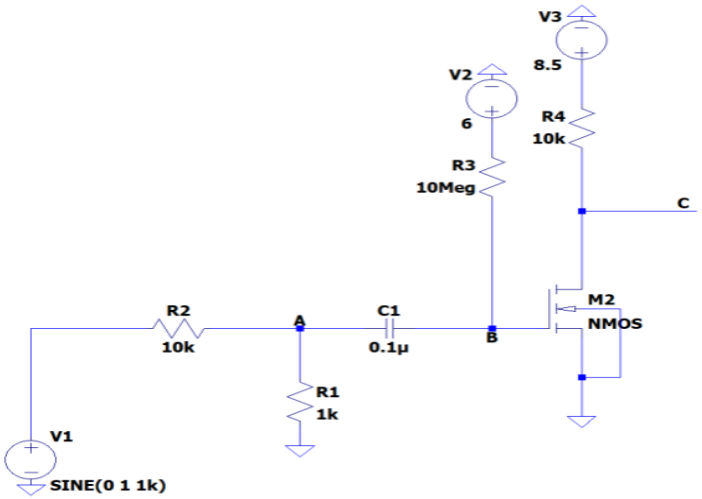
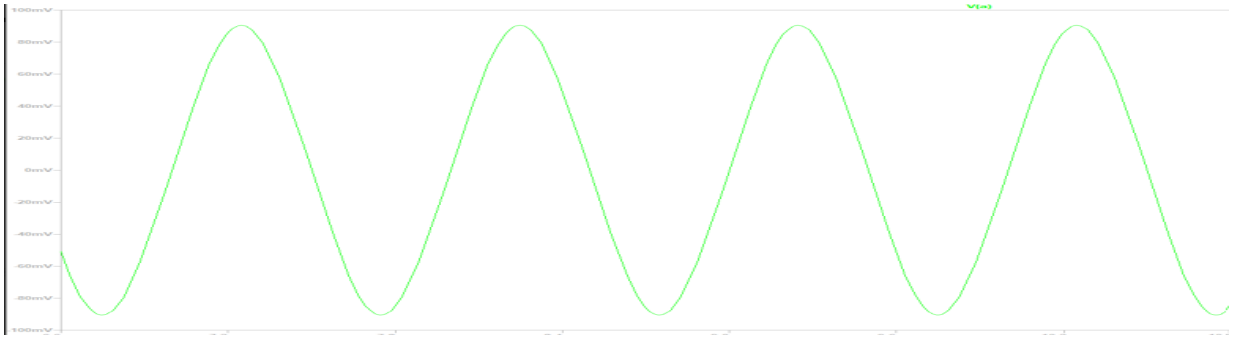


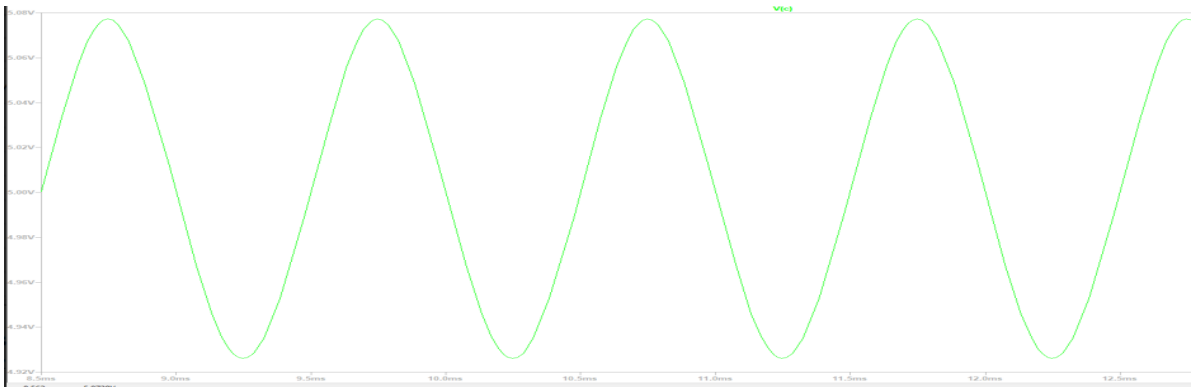
Figure 4: Simplistic amplifier topology.


V3
8.5
V2
6
R4
10k
R3
10Meg
C
M2
NMOS
R2
10k
A
C1
0.1µ
B
R1
1k
V1
SINE(0 1 1k)

Va:



Vc:



2.1 Transconductance :

Transconductance is the property of certain electronic components. Conductance is the reciprocal of resistance; transconductance is the ratio of. the current change at the output port to the voltage change at the input port. It is written as gm.

Similarly, in field effect transistors, and MOSFETs in particular, transconductance is the change in the drain current divided by the small change in the gate/source voltage with a constant drain/source voltage. Typical values of gm for a small-signal field effect transistor are 1 to 30 millisiemens.

Transconductance is a key test for validating the MOSFET performance in power electronics designs. It ensures that a MOSFET is functioning properly and helps engineers choose the best one when voltage gain is a key spec for their circuit designs. This, in turn allows companies to take power semiconductor devices to market faster while minimizing failures in the field.

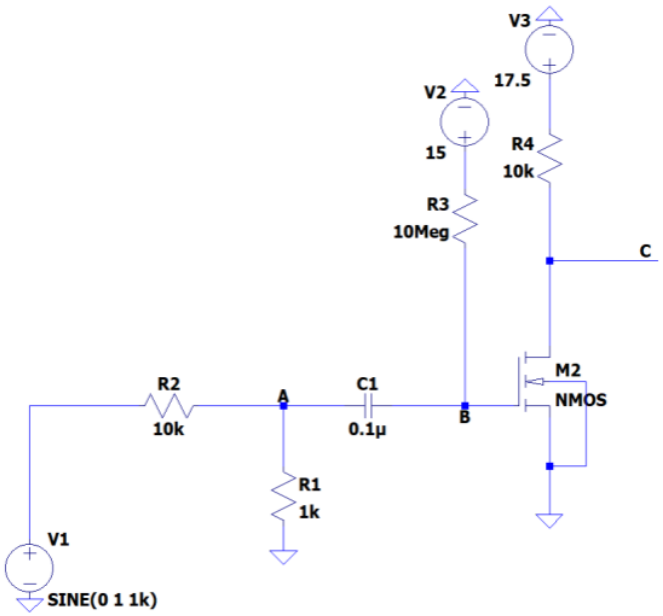
Transconductance is the ratio of drain current (ID) to gate-source voltage (VGS) when a constant drain-source voltage is applied. The current to voltage ratio is commonly referred to as gain. Transconductance is a critical parameter strictly connected with the threshold voltage (VTH) of MOSETs and both are related to the size of the gate channel. The formula for deriving the transconductance of a MOSFET from I-V measurements is:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

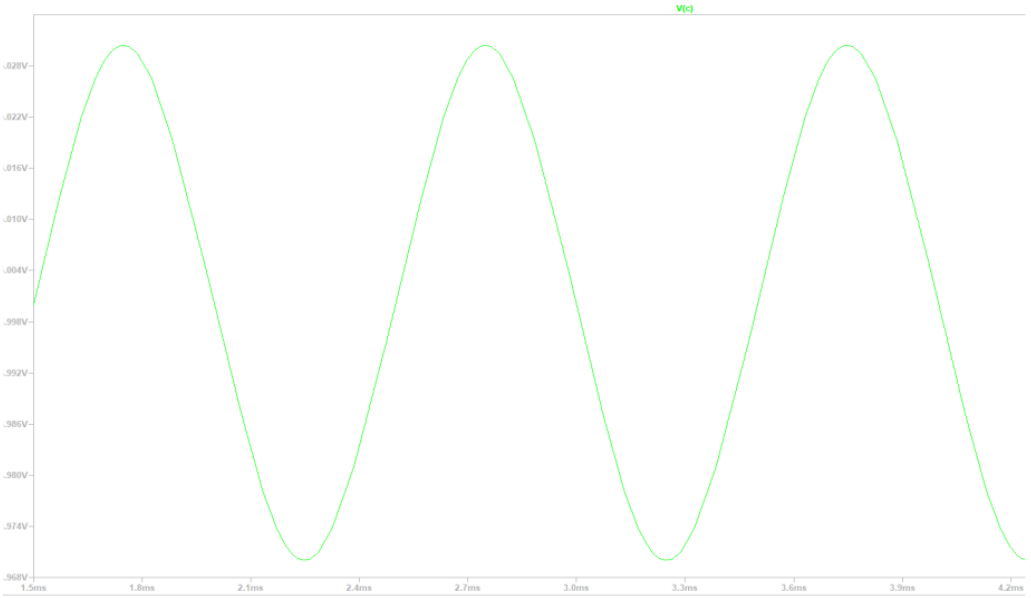
First Vsig = 0, then V2 = 6 V, and finally V1 is set to VC = 5 V. V1 was measured. The signal generator is tuned to provide 1 Vpp sine wave at 1 Khz. Checked the DC bias voltages to make sure the transistor is in saturation. Observed the small signal at nodes A and C through your oscilloscope.

2.1b First we set Vsig = 0, then V2 = 15 V, and finally we set V1 to be VC = 5 V. We measured V1. We have now set the signal generator to provide a 1 Vpp sine wave at 1 kHz. We checked the DC bias voltages to make sure the transistor was in saturation. We observed the small signal at nodes A and C through your oscilloscope. We paid attention to the small signal voltage gain Av = vc/va.

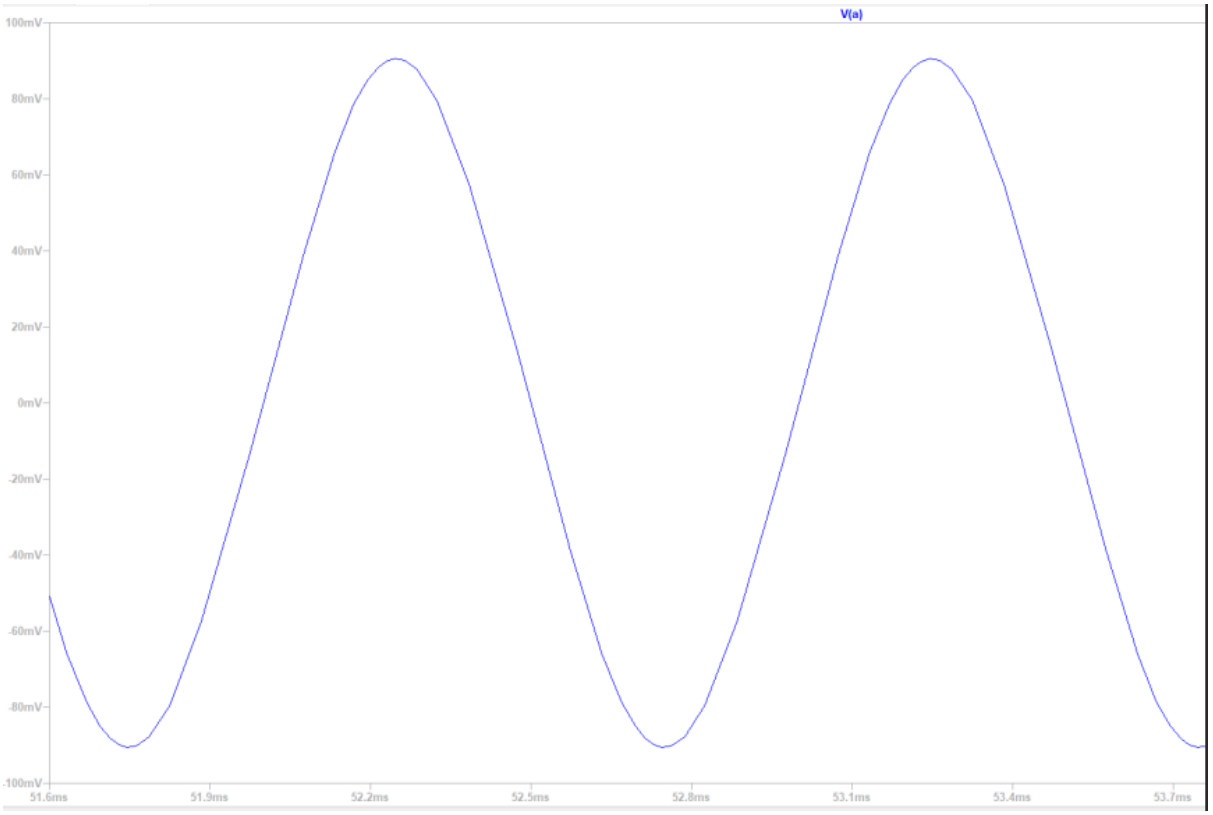
Since we could not get to this part during the experiment, we tried to set up the circuit in electronic environment. The obtained values and results are shown below.

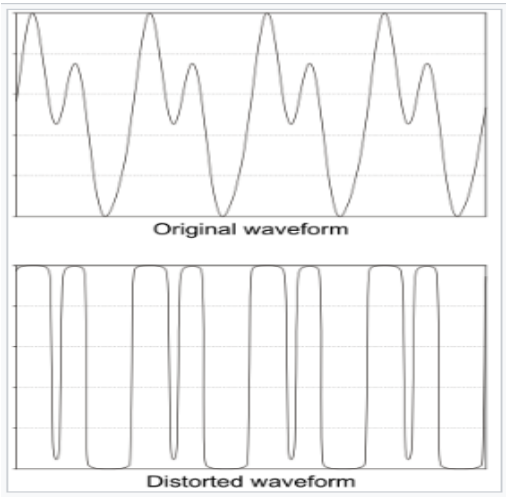


2.1 Vc



2.1 Va





A graph of a waveform and the distorted version of the same waveform

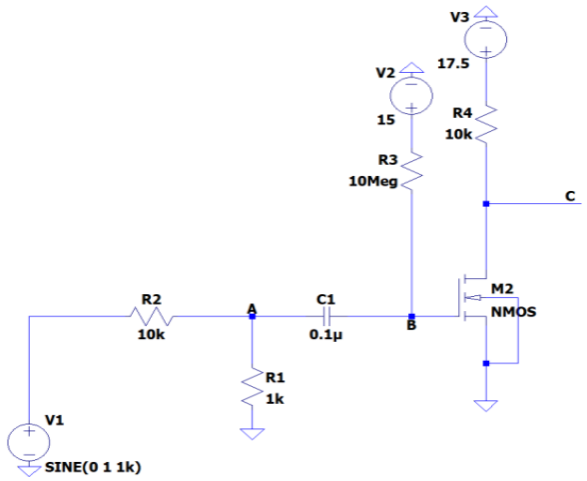
2.2 Signal Distortion

In signal processing, distortion is the alteration of the original shape (or other characteristic) of a signal. In communications and electronics it means the alteration of the waveform of an information-bearing signal, such as an audio signal representing sound or a video signal representing images, in an electronic device or communication channel.

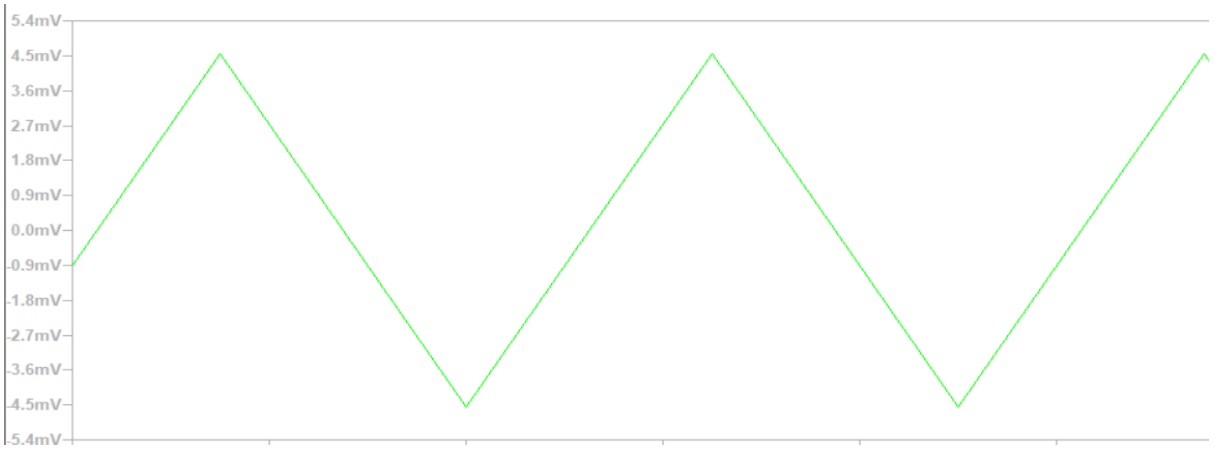
Distortion is usually unwanted, and so engineers strive to eliminate or minimize it. In some situations, however, distortion may be desirable.

In this part of the experiment, the same operations as 2.1.b are present, but triangular wave is sent.

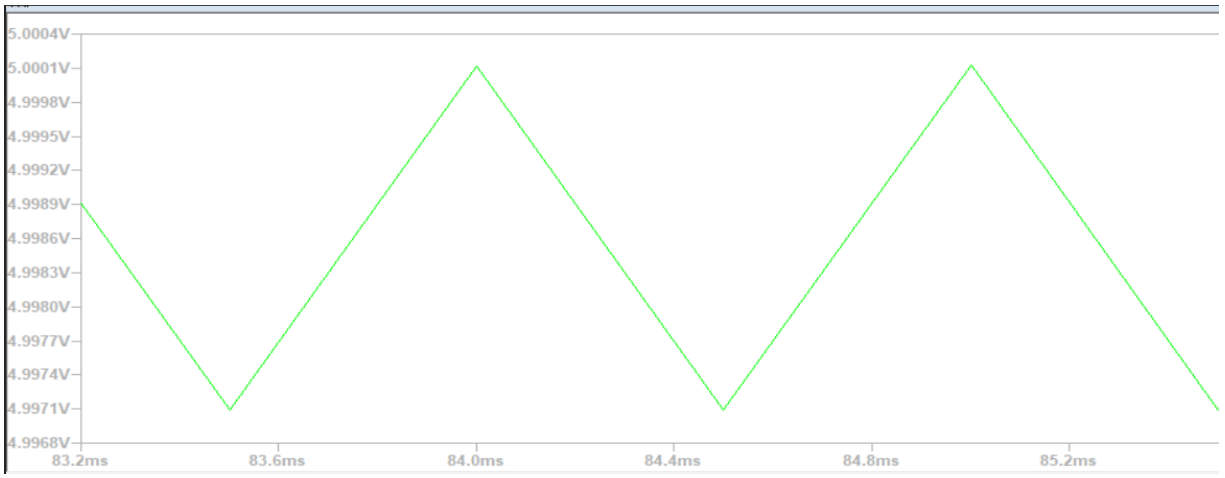
2.2.a Circuit:



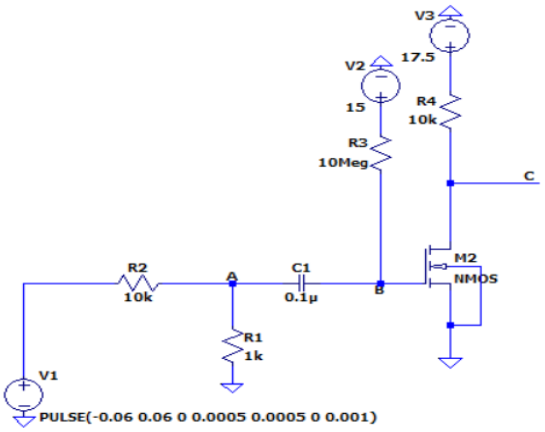
2.2.a Va

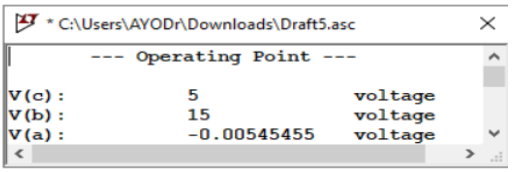


2.2.a Vc

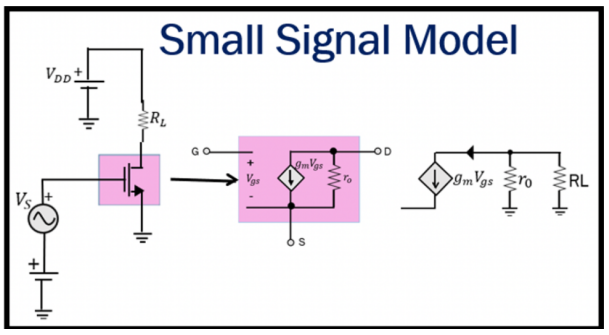


2.2.b We increased the input signal level until the Av value dropped 10%. We observed the small signal at nodes A and C on the oscilloscope and recorded the small signal voltage gain. In this case we have measured the DC voltage at node C. We specified all of these situations on the circuit as shown below and noted the results.



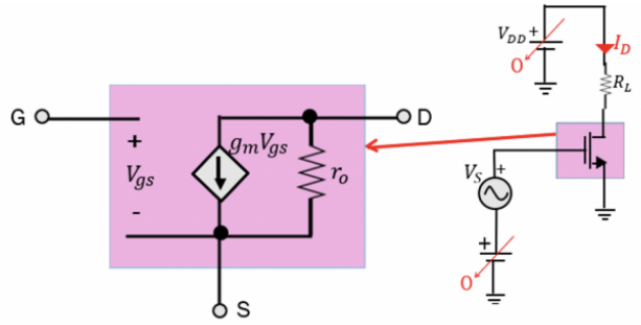


2.2.a Av = 1111.1
10% drop means gain should be 1000
If we take Vc as 5V peak
Va peak should be 5mV
Av value comes from here 1000
Dc Vc value came from 5V.



Small Signal in MOSFET

In this circuit, the Vgs is the input signal applied between gate and source terminal, and we know that the change in drain current is linearly proportional to Vgs. In this model, if you consider the effect of channel and modulation, then there will also be an output resistance (r0). If it is for a long length channel, then, as read in the Early Voltage section in the MOS transistor for a long length channel, the curve slope is almost constant in the saturation region, λ is very low, sometimes considered 0. Therefore, under the small-signal approximation, the MOS transistor can be replaced by the small-signal model.

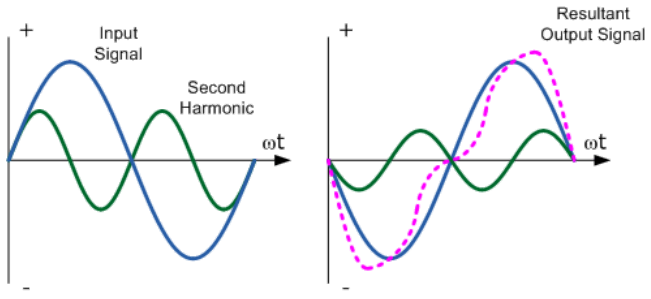


In the small-signal model, there is an output resistance r0 and the current source is gmVgs, so if we can find the Transconductance (gm), we can find the value of current in this circuit. Output resistance r0 is the fluctuation of drain-source voltage to current. For the long channel transistor, the VA (early voltage) is high, and as per the equation, r0 is directly proportional to length; therefore, r0 is high for the long channel transistor. Here, ID is the current bias.

- $r_0 = \frac{\partial V_{ds}}{\partial I_{ds}} = \frac{V_A}{I_D}$

AC analysis for the given circuit considering DC is 0 & VDD is grounded. VS in a small signal model is placed between gate and source terminal. When input signal VS is very low, the MOS transistor can be replaced by the small-signal model. The flow of current is clockwise and is gmVGS, and V0 is connected to load resistance RL. R0 and RL are in a parallel arrangement. Therefore, gain here will be gmVGS. (RL||r0) and this value is more than 1, and this shows that the output voltage will be amplified.

$$\text{Gain} = \frac{V_0}{V_S} = \text{gm}.(RL \| r_0) > 1$$



What is the nonlinear distortion?
Non linear distortion results from systems where the output signal is not exactly proportional to the input signal and harmonics or intermodulation products are generated. The impairment is introduced by the analogue part of transmission and switching systems and needs to be considered in the specification of the performance of the individual network components. However the levels of distortion encountered are such that it is rarely necessary to consider the distortion on an end to end basis.

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