GEBZE TECHNICAL UNIVERSITY

ELECTRONICS ENGINEERING

SPRING 2022

ELM237

ELECTRONICS LABORATORY I

LAB 4 EXPERIMENT REPORT

Bipolar Transistor Basics

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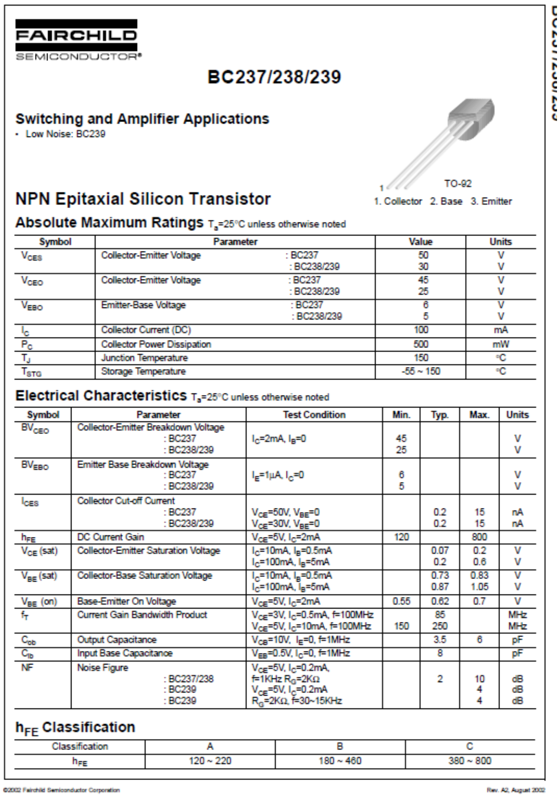

FAIRCHILD SEMICONDUCTOR®

BC237/238/239

Switching and Amplifier Applications
- Low Noise: BC239

TO-92
1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CES}	Collector-Emitter Voltage : BC237 : BC238/239	50 30	V V
V_{CEO}	Collector-Emitter Voltage : BC237 : BC238/239	45 25	V V
V_{EBO}	Emitter-Base Voltage : BC237 : BC238/239	6 5	V V
I_C	Collector Current (DC)	100	mA
P_C	Collector Power Dissipation	500	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage : BC237 : BC238/239	I_C=2mA, I_B=0	45 25			V V
BV_{EBO}	Emitter Base Breakdown Voltage : BC237 : BC238/239	I_E=1μA, I_C=0	6 5			V V
I_{CES}	Collector Cut-off Current : BC237 : BC238/239	V_{CE}=50V, V_{BE}=0 V_{CE}=30V, V_{BE}=0		0.2 0.2	15 15	nA nA
h_{FE}	DC Current Gain	V_{CE}=5V, I_C=2mA	120		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA I_C=100mA, I_B=5mA		0.07 0.2	0.2 0.6	V V
V_{BE} (sat)	Collector-Base Saturation Voltage	I_C=10mA, I_B=0.5mA I_C=100mA, I_B=5mA		0.73 0.87	0.83 1.05	V V
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=5V, I_C=2mA	0.55	0.62	0.7	V
f_T	Current Gain Bandwidth Product	V_{CE}=3V, I_C=0.5mA, f=100MHz V_{CE}=5V, I_C=10mA, f=100MHz	 150	85 250		MHz MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		3.5	6	pF
C_{ib}	Input Base Capacitance	V_{EB}=0.5V, I_C=0, f=1MHz		8		pF
NF	Noise Figure : BC237/238 : BC239 : BC239	V_{CE}=5V, I_C=0.2mA, f=1KHz R_G=2KΩ V_{CE}=5V, I_C=0.2mA R_G=2KΩ, f=30~15KHz		2	10 4 4	dB dB dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	120 ~ 220	180 ~ 460	380 ~ 800

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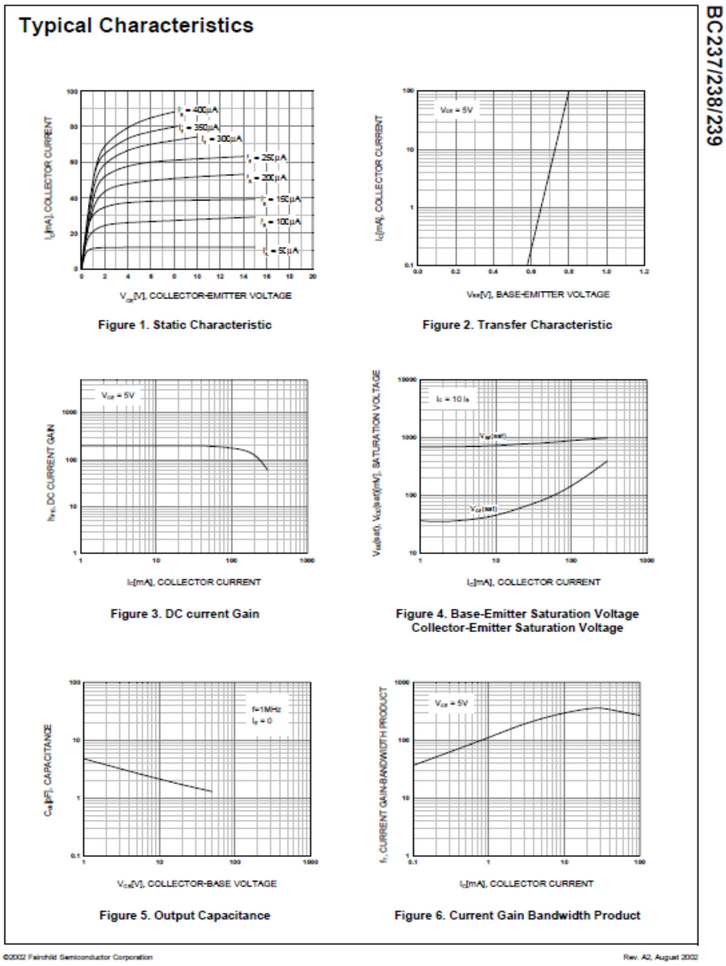
Picture 1

What is BJT?

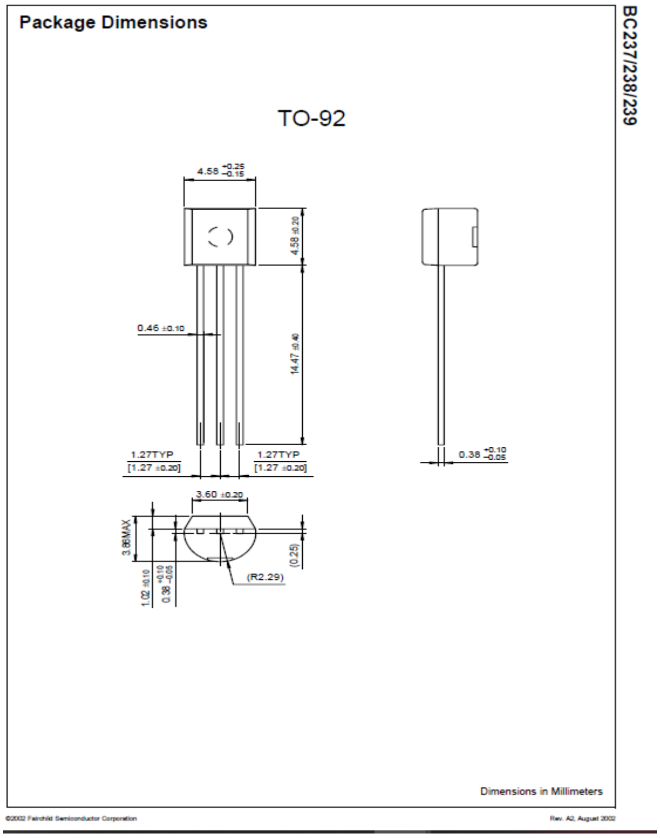
BJT which is short for Bipolar Junction Transistor is a semiconductor device that is constructed with 3 doped semiconductor regions. Base , collector and emitter seperated by 2 p-n junctions.

BJT's has 2 types PNP and NPN type of transistors. They are generally used to amplify the current.

They have 3 operation regions which are Active, Saturation and cut-off regions. In our experiment we have used a NPN BJT BC238. It's datasheet is available above from Picture 1 to 3.



Picture 2



Picture 3

1.Component Familiarization and Identification

1.1 Establishing Device Currents (npn):

Connect the circuit as shown in Figure 1, with the supplies *carefully* adjusted to ±10.00V. Note the exact values of resistors using your DVM and try to choose well-matched (with a 1% tolerance) resistors.

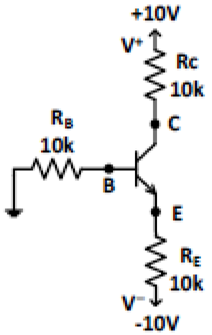
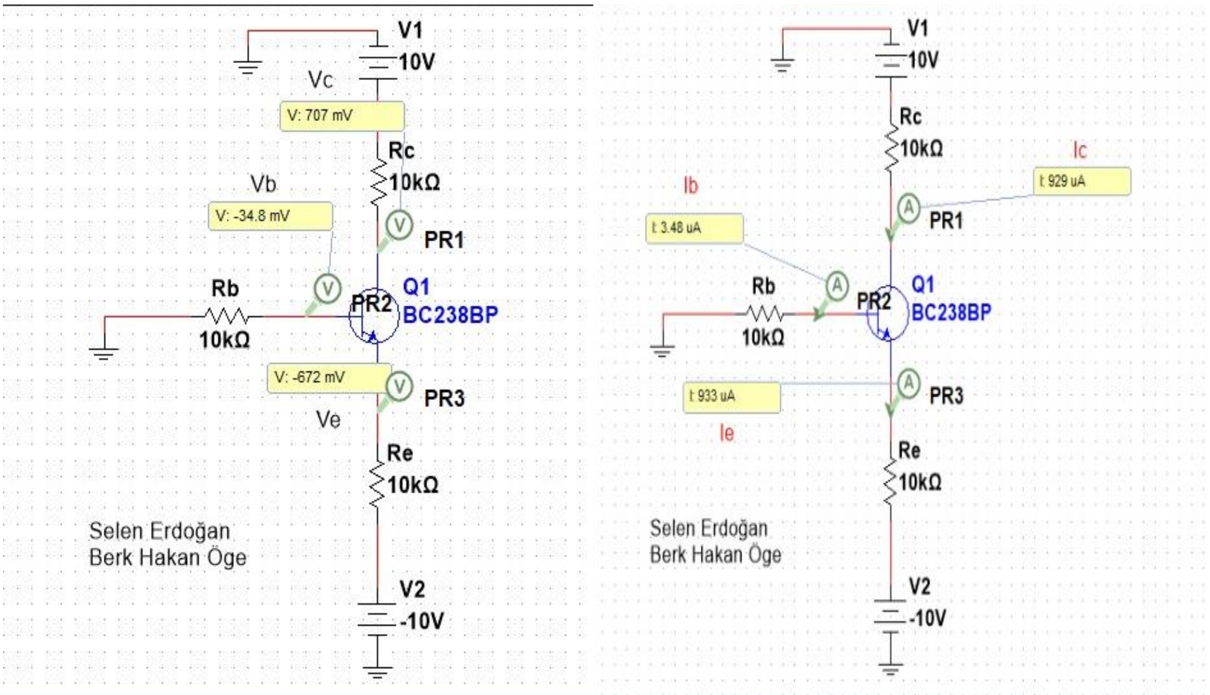


Figure 1. A flexible biasing circuit.

Measure the voltages at B, E, and C with respect to ground, using your DVM. Using these measurements, calculate V_{BE}, I_B, I_C, I_E, α, β. Fill Table 1.

V_B	V_C	V_E	V_{BE}	I_B	I_C	I_E	α	β
-36.33mV	0.617V	-0.686V	650mV	3.67 μA	0.952mA	0.954mA	0.996	259

Picture 4 result table 1 for figure 1



Picture 5 simulation results for voltage and current values in picture 4 table 1

Here in Picture 5 we can clearly see that the values we have measured inside the lab are similiar to the values we have found in simulations.

$$\text{Alpha}, (\alpha) = \frac{I_C}{I_E} \quad \text{and} \quad \text{Beta}, (\beta) = \frac{I_C}{I_B}$$

$$\therefore I_C = \alpha . I_E = \beta . I_B$$

$$\text{as: } \alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

Picture 6 formulas used to calculate current, β and α values

When we do the calculations according to both simulations and lab values we get the correct results for our current values.

1.2 Identifying the Controlling Junction and Junction Current:

a) Raise V^- to -5V, and measure the voltages at B, E, and C with respect to ground, using your DVM. Repeat the calculation steps in 1.1 and fill Table 2.

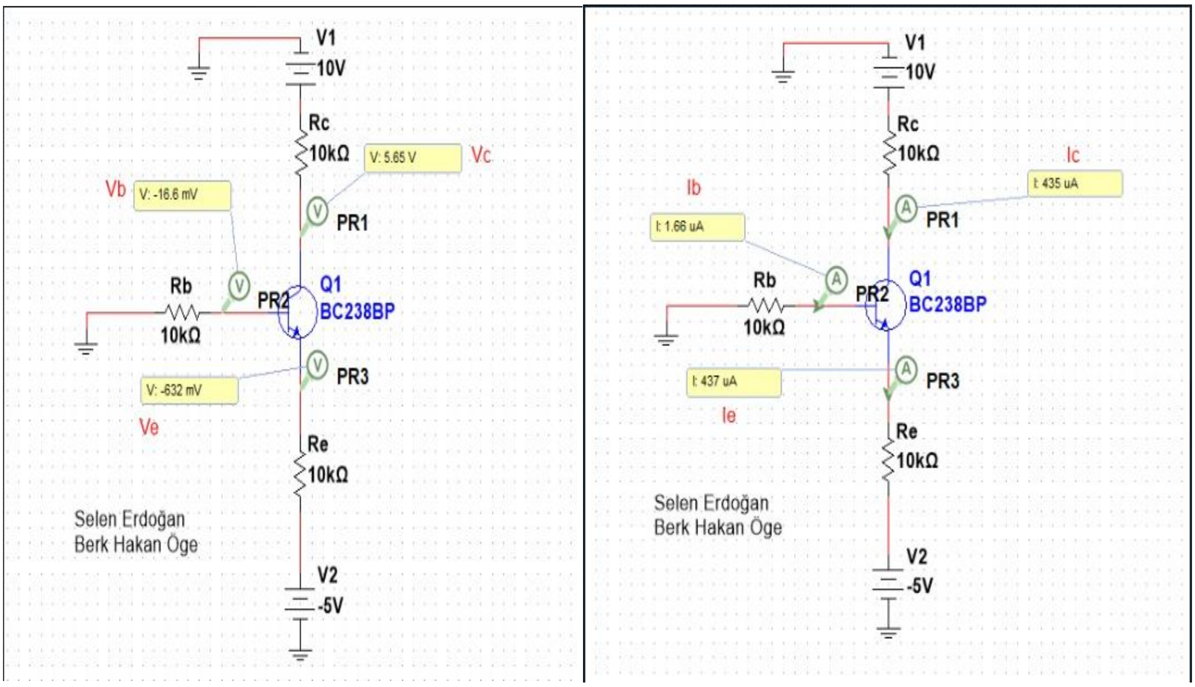
b) With V^- = -5V, lower V^+ to +5V, and repeat a).

In this step 1.2 we have first raised our -10V power supply to -5V and kept 10V supply stable. Measured the node voltage values and done the calculations according to given formulas in Picture 7

supply voltages.

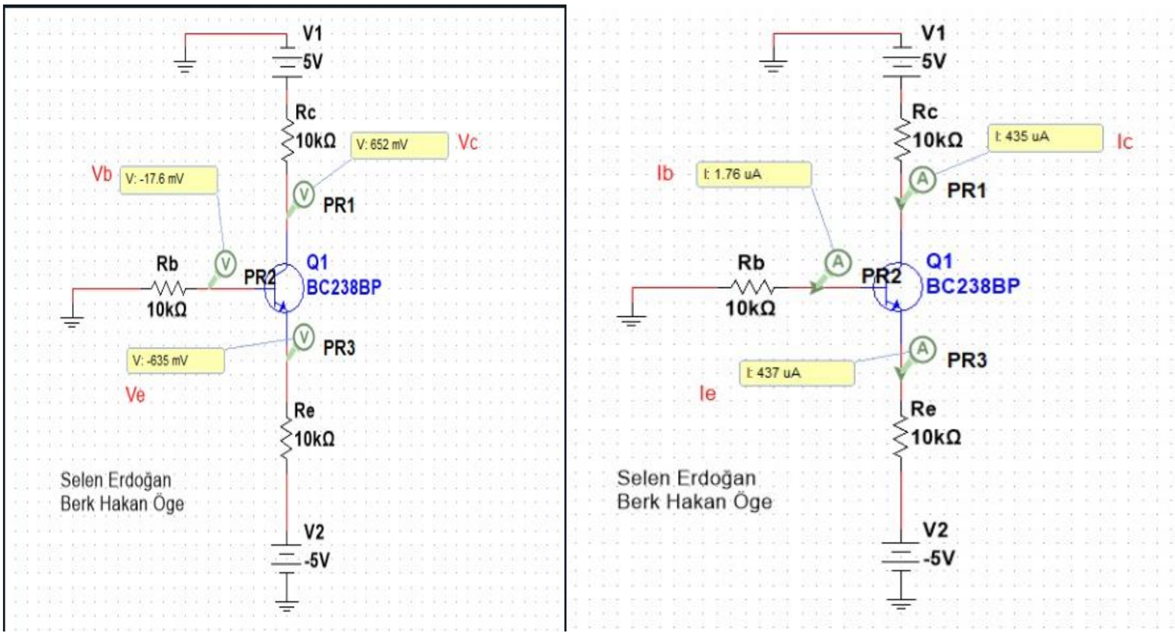
	V_B	V_C	V_E	V_{BE}	I_B	I_C	I_E	α	β
V^- = -5V V^+ = +10V	mV -16 17	V 5.668	V -0.582	mV 565,83	1.6μA	mA 0.435	mA 0.442	0,996	268.5
V^- = -5V V^+ = +5V	mV -30.5	V 0.705	V -0.653	622,5	3.1μA	mA 0.429	mA 0.435	0.992	137.94

Picture 7 table 2



Picture 8 Simulation Results of Voltage and Current Values in table 2.a

In the image above Picture 8 we can observe that our measurements during the lab session is almost the same as the values we have found with simulations. When we increase the V^- value the emitter voltage also increased accordingly and thus V_{BE} value decreased since it is $V_B - V_E$. When the supply voltage is twice its size from earlier the current flowing through the emitter is decreased almost half of its magnitude. And this causes all the current inside the system to decrease and this movement results in collector voltage increasing. Finally once again we used the Picture 6 formula sheet for the current values during the lab session and calculations seems to be on point.



Picture 9 Simulation Results of Voltage and Current Values in table 2.b

When we look at Picture 9 it is crystal clear that our system is back and balanced just like Picture 5 just the magnitude of our values are half the size since we adjusted them to be like that. During the 1.2 Identifying the controlling junction and junction part our BJT is in active mode cause the V_{BE} value is around 0.6-0.7 V and the current can flow through. Finally once again we used the Picture 6 formula sheet for the current values during the lab session and calculations seems to be on point.

2.Other, Less-Stable Biasing Schemes

2.1 Base-Current Bias:

Connect the circuit as shown in Figure 2. Note that this circuit is not a recommended bias design.

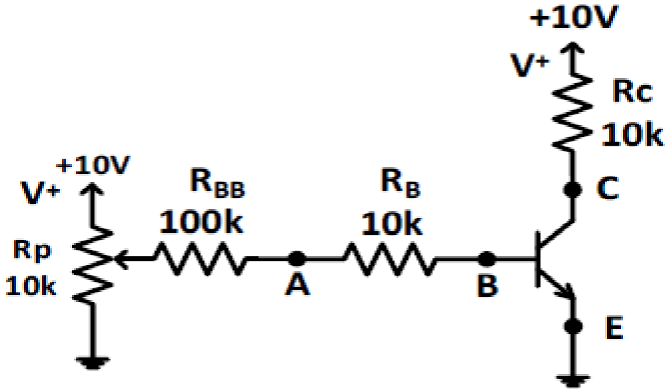


Figure 2. A bad base-current-biasing circuit.

a) Measure the voltage at node *C*, adjusting potentiometer R_P until V_C = +5V.

b) Measure the voltages at nodes *A* and *B* with your DVM.

c) While measuring V_C, heat the transistor. Note the new value of V_C.

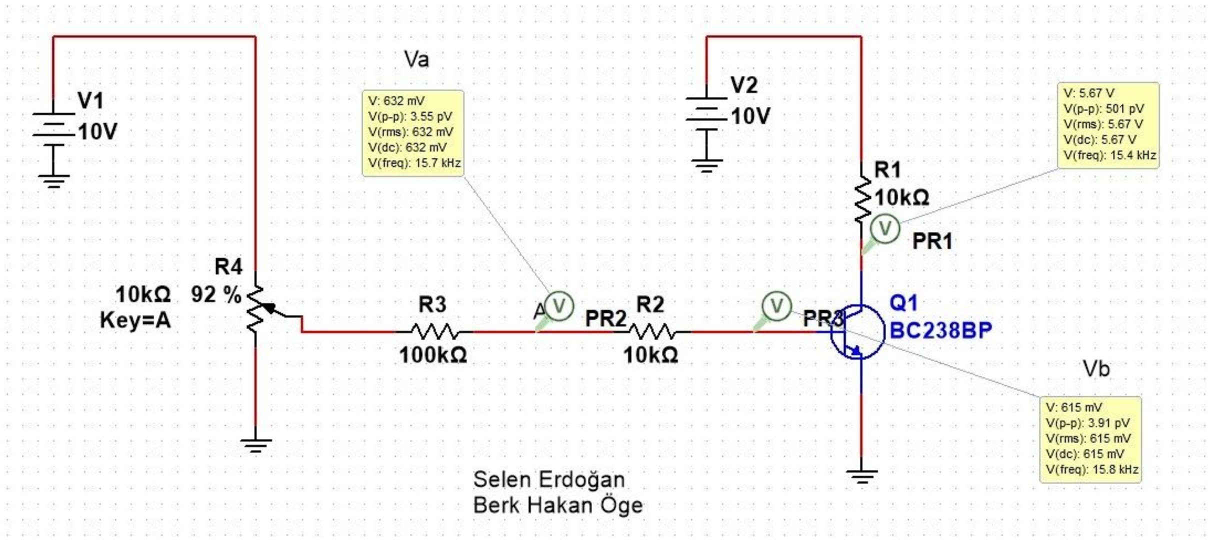
d) Remove the transistor (carefully). Insert another one in its place; repeat the parts b) and c) without changing the potentiometer resistance R_P.

Now we are in part 2 Less-stable biasing schemes we are supposed to but together a different circuit design and continue our measurements. Note our observations down into the table 3 which can be seen down below in Picture 10.

Table 3. Operating points of BJT in Figure 2 under different temperature conditions.

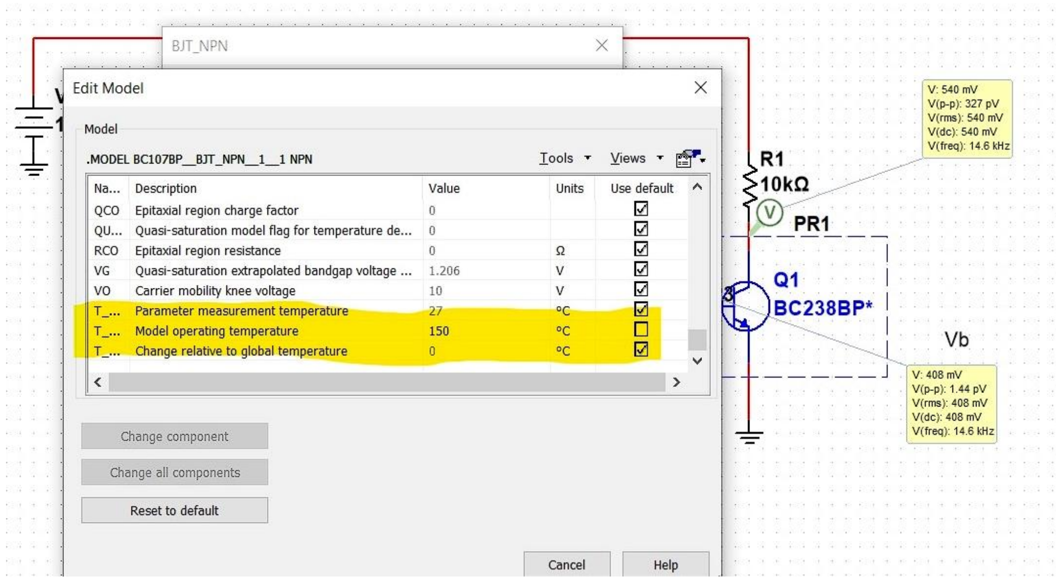
Node Voltage	Transistor 1	Transistor 2
V_A	0.567 Volt	0.587 volt
V_B	280 mV	220 mV
V_{C_cold}	4.76 Volt	4.098 Volt
V_{C_hot}	3.7 Volt	2.65 Volt

Picture 10 table 3



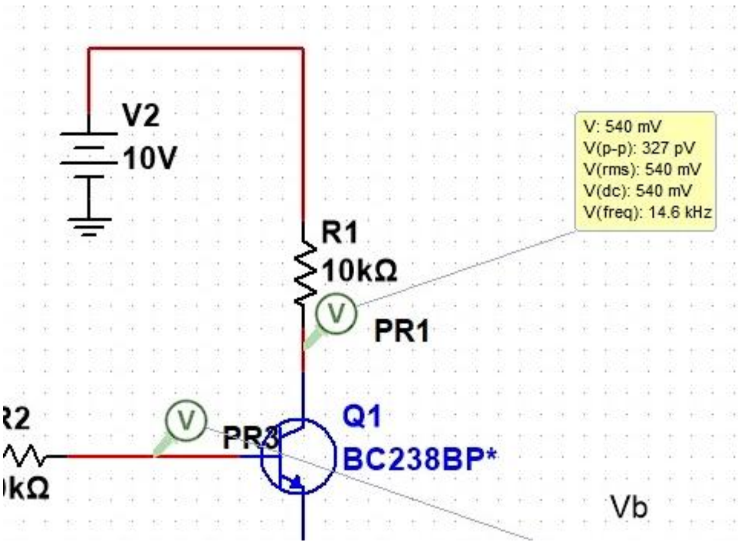
Picture 11 2.1.a and 2.1.b

Here in Picture 11 we have completed the task 2.1.a set our potentiometer value while measuring V_C value and tried to get as much close to 5V as we can. After doing so we move on to the next step 2.1.b measuring the voltages at nodes A and B and noting them down to our table 3. V_B value seems to be bit more off than our value during the session but as we can see the V_C voltage is a bit different than the value we have measured during our experiment aswell and most likely caused by that difference but when we look at V_A we can see that we are actually not that far from our measurements.



Picture 12 settings for changing temperature

Here in Picture 12 you can see that we have changed the simulation settings and heated up the BJT.



Picture 13 V_C value after we heat up the BJT

When we look at the Picture 13 we can notice that our V_C voltage decreased and the current flowing has increased. That is because a transistor can only let current flow as much as charge carriers it has available. When the temperature is above absolute zero (-273 C^o) these carriers also form spontaneously and applying heat can increase the amount of speed these carriers are formed and increase the amount of carriers. Thus more current can flow through and voltage value decreases.

2.2 Fixed Base-Emitter-Voltage Biasing:

Note, this is clearly the worst bias design of all, unless the desire is to create an electronic thermometer! Connect the circuit as shown in Figure 3.

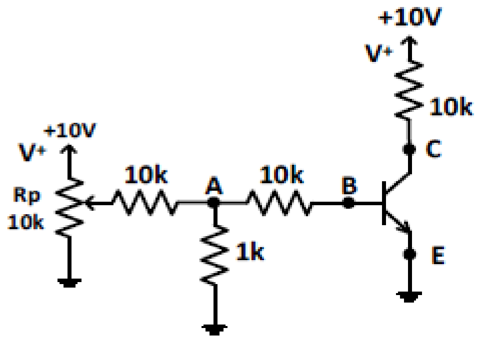


Figure 3. A bad base-voltage-biasing circuit.

a) Measure the voltage at node *C*, adjusting potentiometer R_P until V_C = +5V.

b) Measure the voltages at nodes *A* and *B* with your DVM.

c) While measuring V_C, heat the transistor (ask your TA for a soldering iron). Note the new value of V_C.

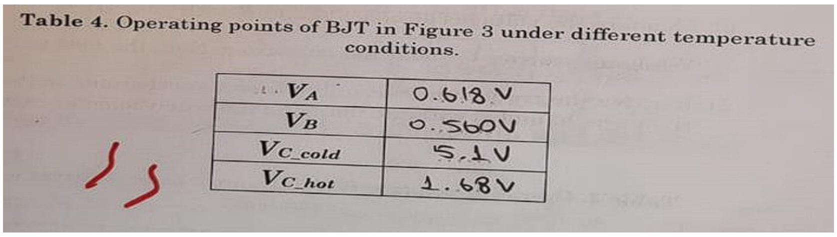
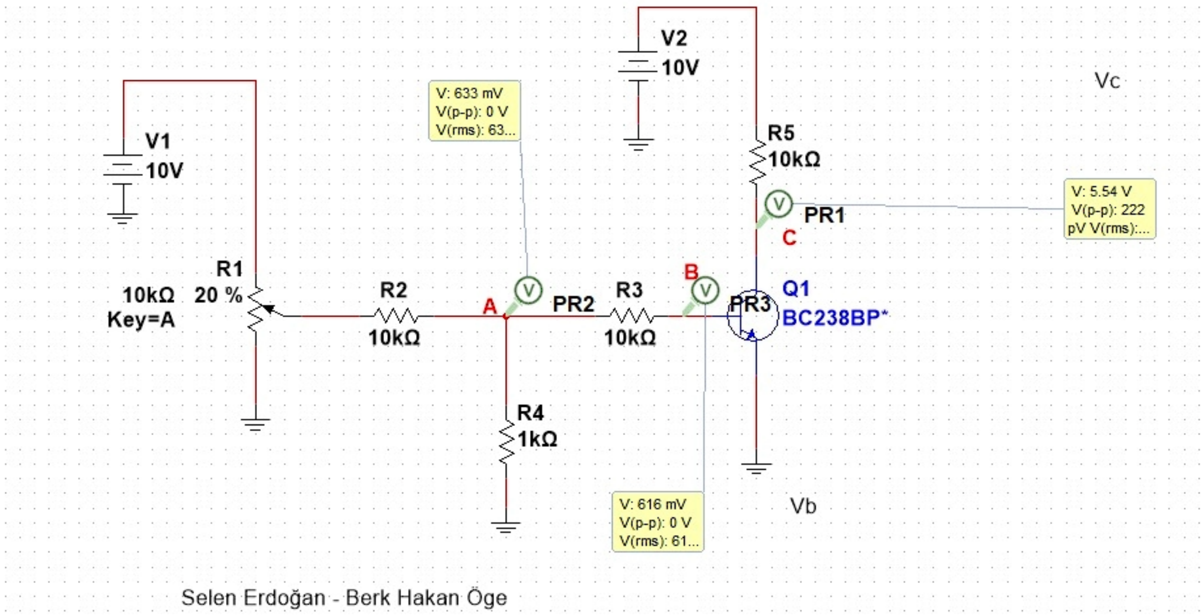


Table 4. Operating points of BJT in Figure 3 under different temperature conditions.

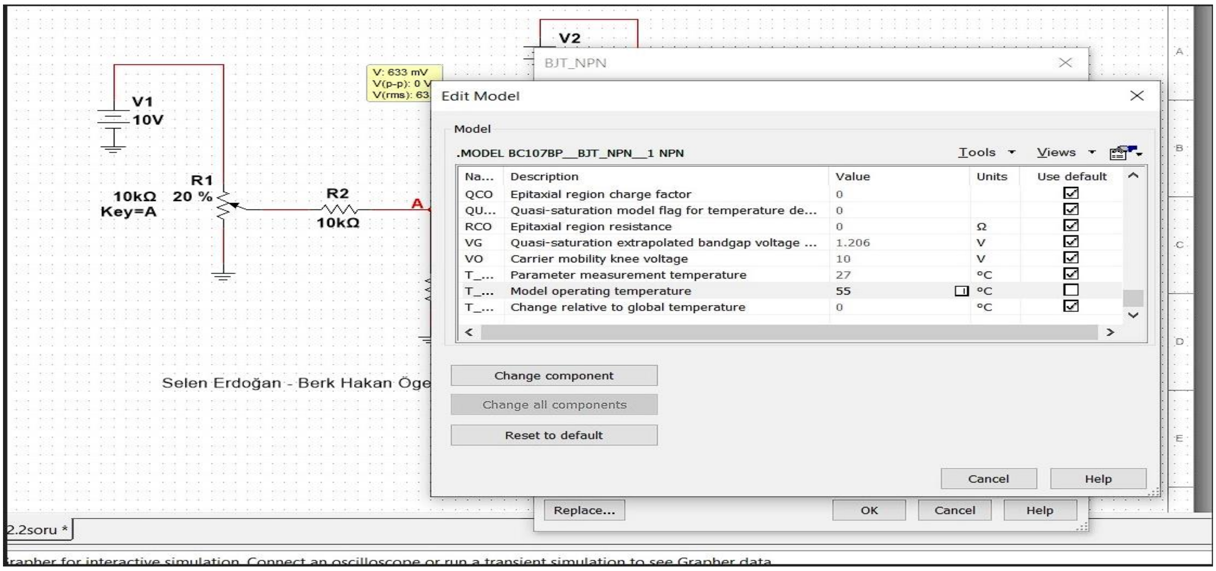
V_A	0.618 V
V_B	0.560V
V_{C_cold}	5.1V
V_{C_hot}	1.68V

Picture 14 table 4



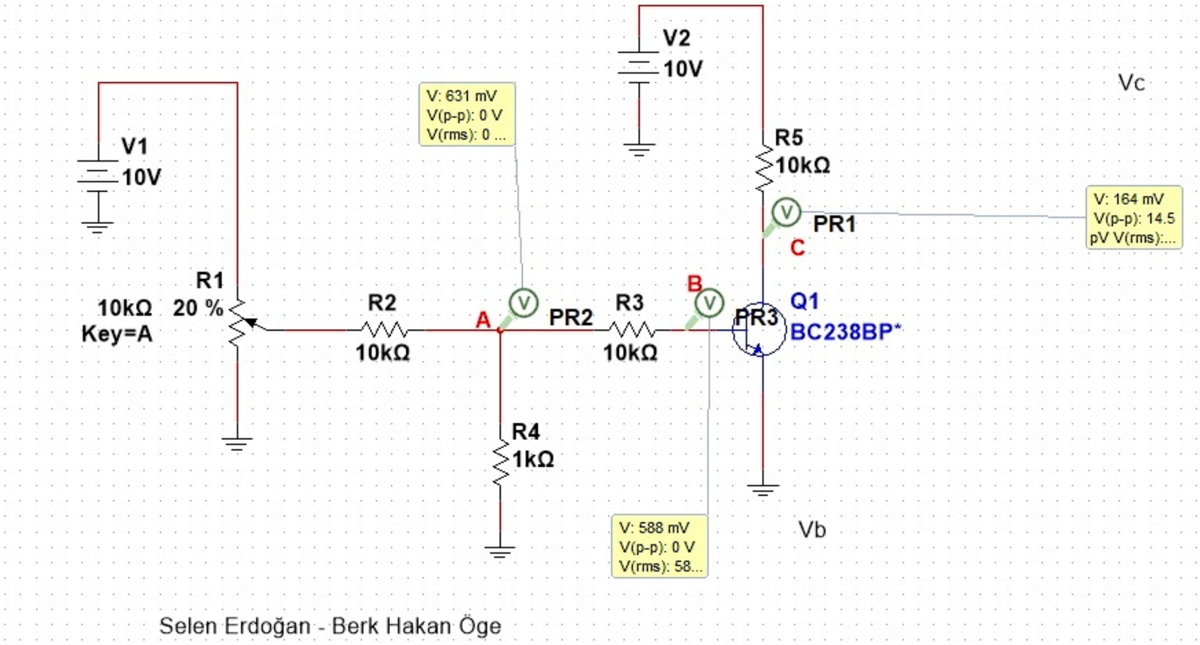
Picture 15 2.2.a and 2.2.b

If you look at the Picture 15 above the values for V_{C_COLD}, V_A and V_B are noted down to table 4 in Picture 14 the V_C value is a bit higher than the value we have seen during the experiment which is the main cause of other voltage values being slightly higher but this can be ignored and say that our system is working just fine.



Picture 15 temperature changing screen

Above at Picture 15 we can see that we changed the temperature value of the BJT and heated it up.



Picture 16 2.2.c after the temperature is changed

In Picture 16, we can see that our V_C voltage has reduced while the current flowing has increased. This is because a transistor can only allow as much current to pass as it has accessible char carriers. These carriers emerge spontaneously at the tamperatures above absolute zero (-273C^o), and providing heat can speed up the formation of these carriers and increase the number of carriers. As a result, more current may flow through, and the voltage value drops.

3.The BJT as Amplifier

While the circuit shown in Figure 4 uses a rather bad bias design, being a combination of base-current and base-voltage biasing, it is relatively convenient for the measurement of gain of a particular transistor under stable environmental conditions. Incidentally, the presence of the potentiometer R_P is, generally speaking, a sure sign of less-than-ideal design.

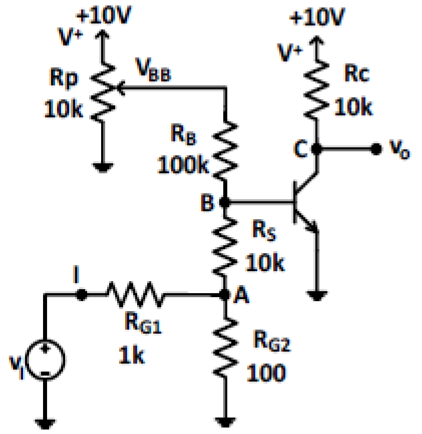
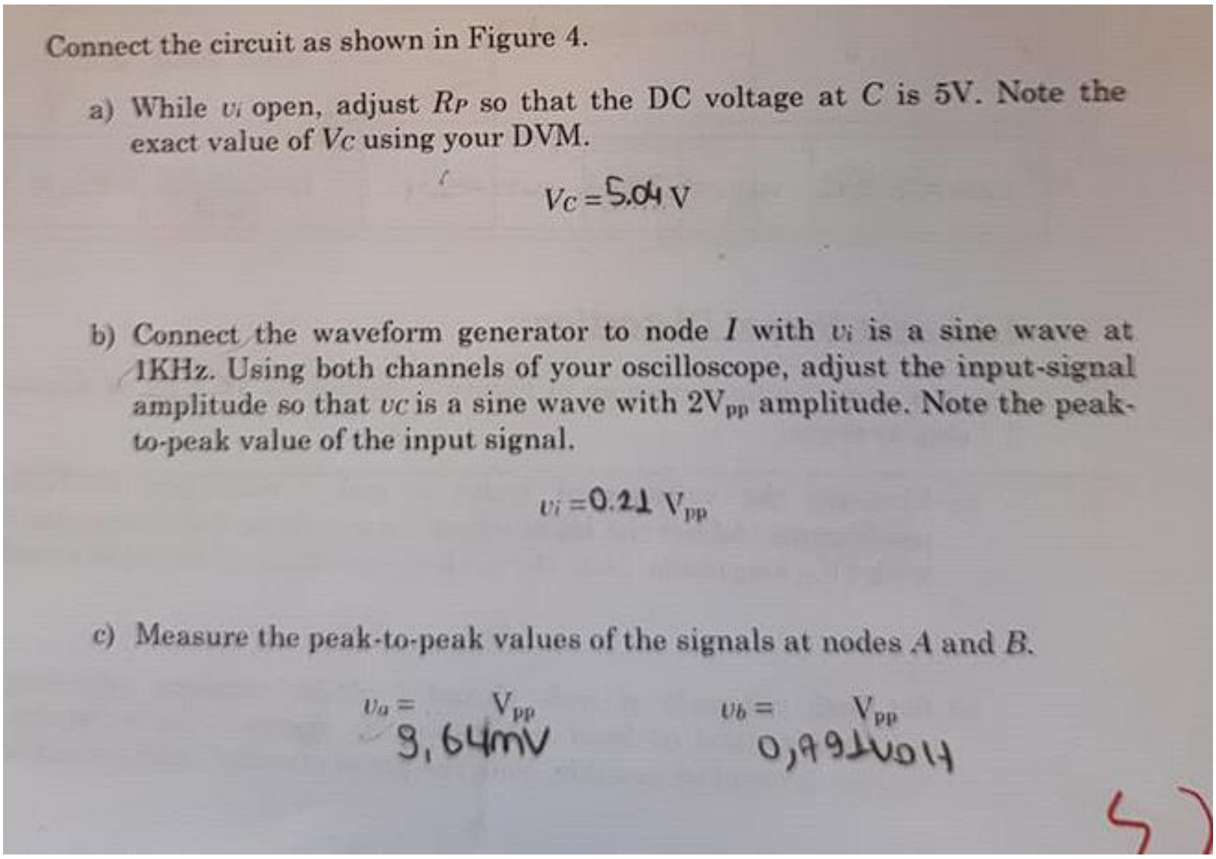


Figure 4. A badly-biased but otherwise-interesting amplifier.



Connect the circuit as shown in Figure 4.

a) While v_i open, adjust R_P so that the DC voltage at C is 5V. Note the exact value of V_C using your DVM.

$V_C =$ 5.04 V

b) Connect the waveform generator to node I with v_i is a sine wave at 1KHz. Using both channels of your oscilloscope, adjust the input-signal amplitude so that v_C is a sine wave with $2V_{pp}$ amplitude. Note the peak-to-peak value of the input signal.

$v_i =$ 0.21 V_{pp}

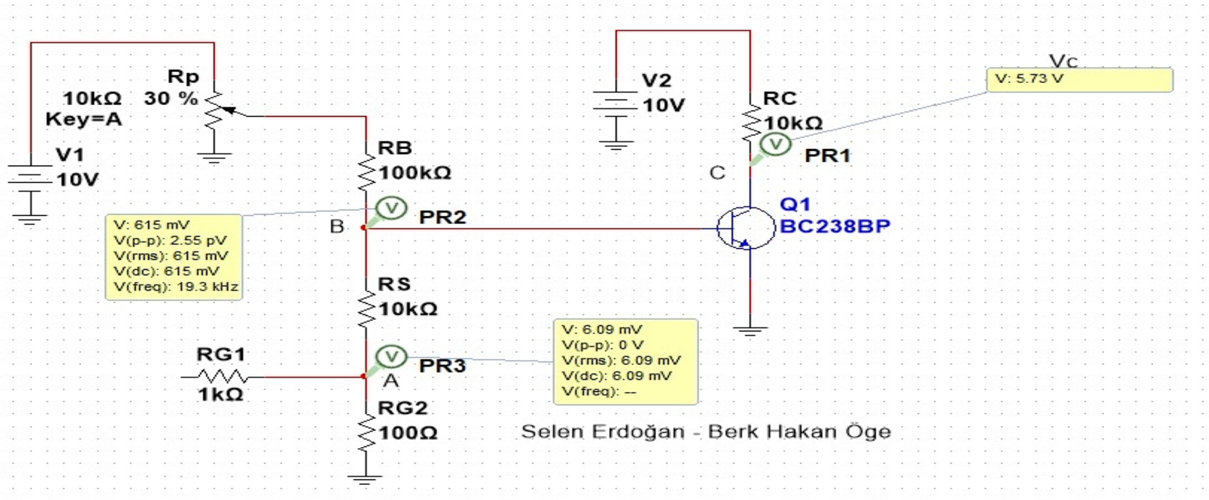
c) Measure the peak-to-peak values of the signals at nodes A and B.

$v_a =$ 9,64mV V_{pp} $v_b =$ 0,991V014 V_{pp}

5)

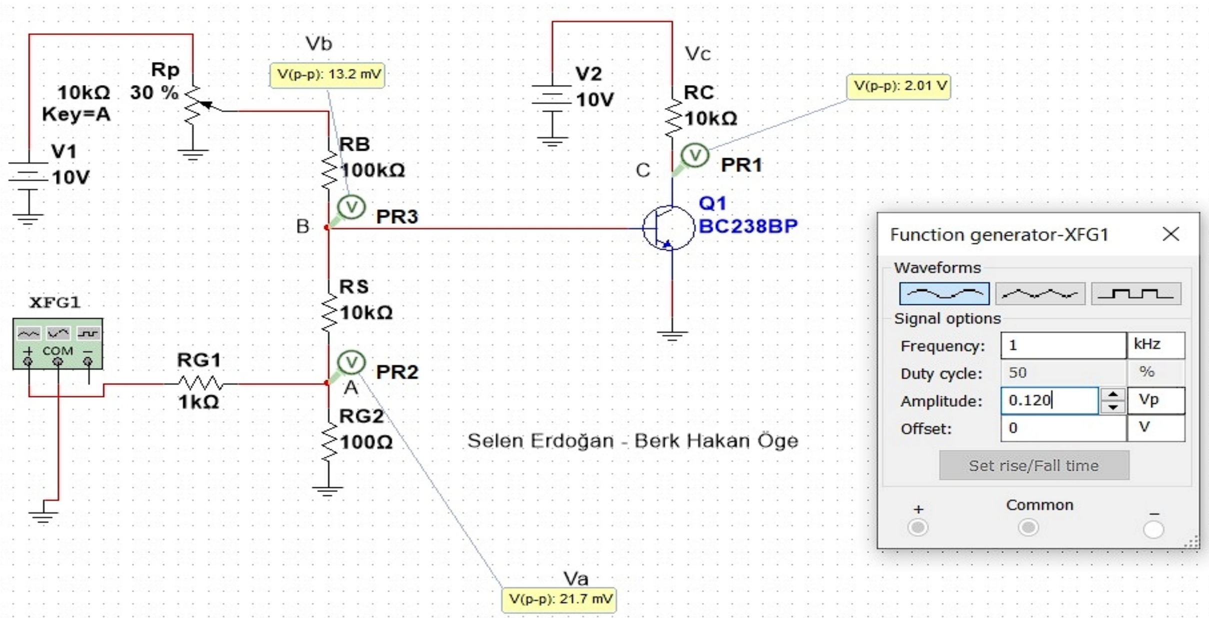
Picture 17 3.1.a & 3.1.b & 3.1.c

Here in Picture 17 we can see the noted down values during the experiment for the part 3.



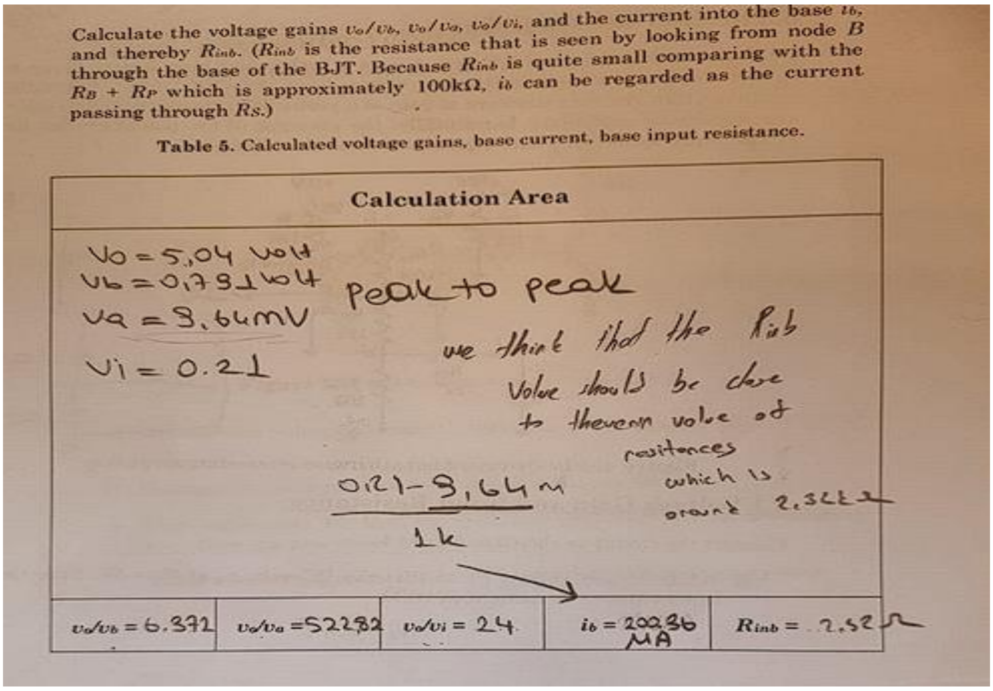
Picture 18 3.1.a circuit

If we look at Picture 18 this design is representing the curcuit for step 3.1.a V_i value is open and we have our V_C value. It seems to be off but it is most likely caused by the fact that we do not work in a ideal environment like the simulation. Other than that this slight difference can be ignored.



Picture 19 V_i connected 3.1.b & 3.1.c

During the part of Picture 19 in the lab session we increased our amplitude value and watched how the V_C value changed and waited for it to increase up to $2V_{P\text{-}P}$. We were having some difficulties and changed to DVM machine and used RMS values to calculate $V_{P\text{-}P}$ values. To convert RMS to $V_{P\text{-}P}$ we have multiplied it by $2\sqrt{(2)}$. Our way of solving the problem we have faced and the given question seems to be right since the value we have found and the simulation result ($V_i = 0.24V_{P\text{-}P}$) are very close to each other. After we set our $V_C = 2V_{P\text{-}P}$ it is time to measure the peak to peak values for nodes A and B.



Calculate the voltage gains v_o/v_b, v_o/v_a, v_o/v_i, and the current into the base i_b, and thereby R_{inb}. (R_{inb} is the resistance that is seen by looking from node B through the base of the BJT. Because R_{inb} is quite small comparing with the $R_B + R_P$ which is approximately 100kΩ, i_b can be regarded as the current passing through Rs.)

Table 5. Calculated voltage gains, base current, base input resistance.

Calculation Area				
Vo = 5,04 volt Vb = 0,791 volt Va = 9,64mV Vi = 0.21 peak to peak we think that the Rib value should be close to thevenin value of resitances which is around 2,5kΩ $\frac{0{,}21 - 9{,}64m}{1k}$				
v_o/v_b = 6.372	v_o/v_a = 522,82	v_o/v_i = 24	i_b = 200,36 μA	R_{inb} = 2,52 Ω

Picture 20 calculation area

Using the values we found during Picture 17 we calculated the voltage gains, I_b and R_{inb}.

3.2 Large Signal Distortion:

Use the same configuration as in Figure 4. Adjust for V_C = 5V as directed in 3.1 step a) above.

a) Measure the voltages at nodes C and I with your dual-channel oscilloscope. Adjust the input-signal amplitude so that v_C is a sine wave with 1V_{pp} amplitude. Note the peak-to-peak value of the input signal.

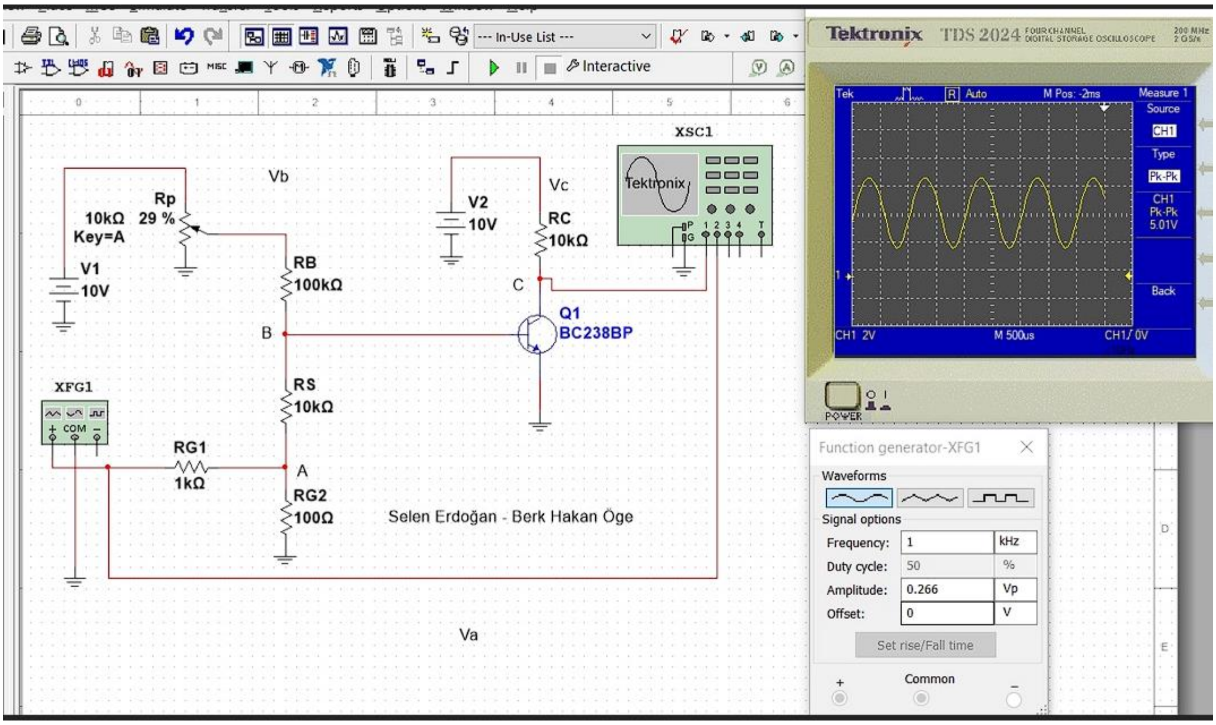
$$v_i = \ldots\ldots \; V_{pp}$$

b) Set both channels of node C and I on AC coupling. Adjusting the volt/division and dc level settings of the channels, try to overlap two signals as exact as possible. Note the phase of node C with respect to I.

$$\Phi = \ldots\ldots$$

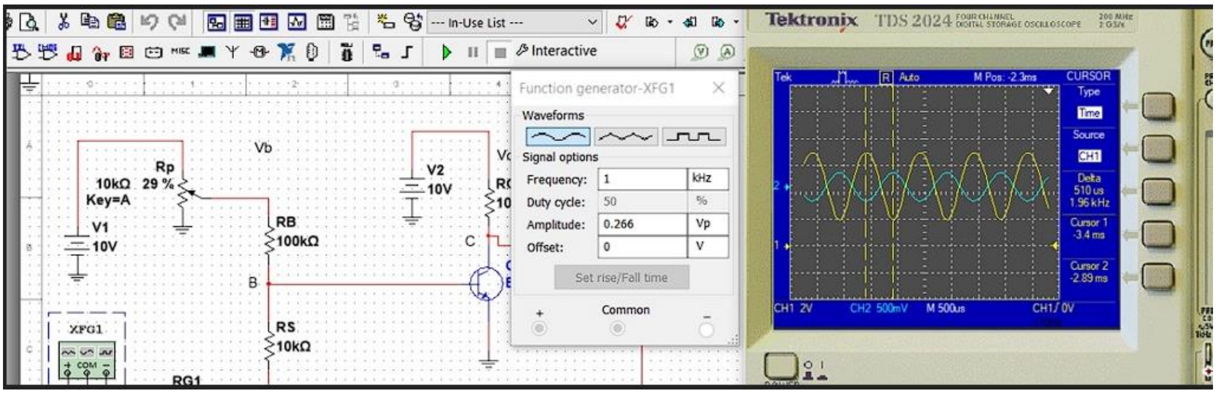
This experiment has been adopted from Department of Electrical and Electronics Engineering, Boğaziçi University

c) Raise the input voltage slowly, while observing the voltages at nodes I and C. Observe that the gain will start to change slightly at some point. Note the necessary values to the table below.



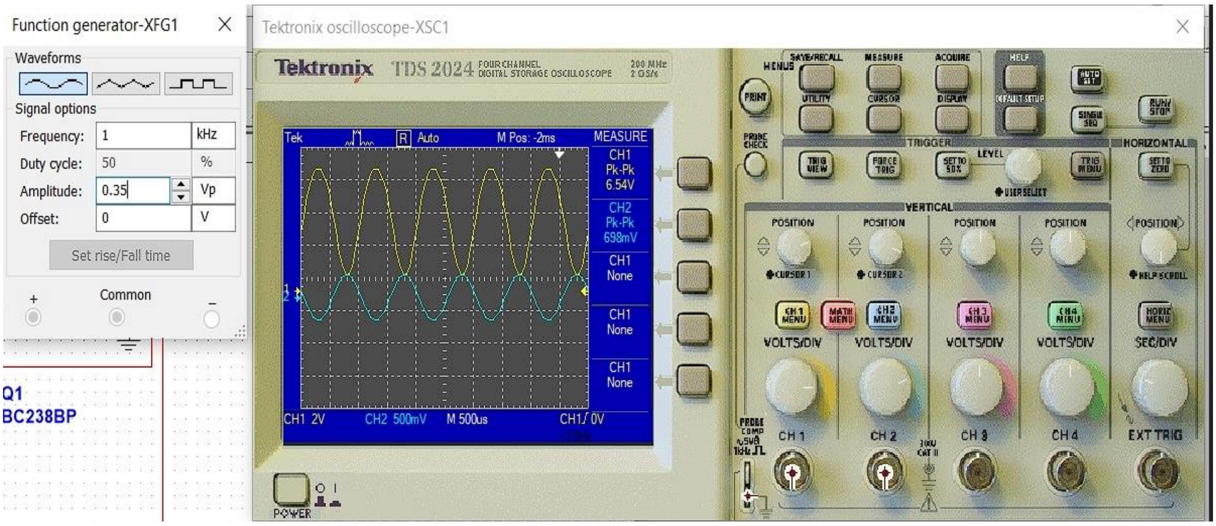
Picture 21 3.2.a

Same steps as before has been followed and the V_C value is set to 5V. Afterwards to set the V_C value to $1V_{P-P}$ amplitude input signal has been adjusted to 0.532 V_{P-P}.



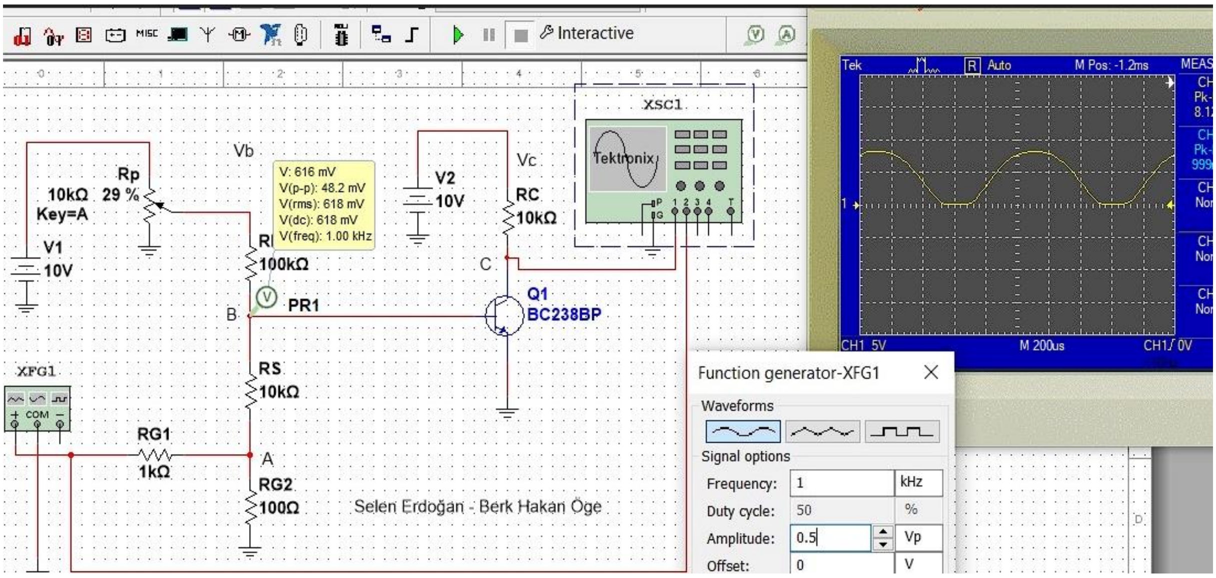
Picture 22 3.2.b phase shifting

When we place both waves overlap to each other and take the time shift between them according to $\mathbf{\Phi = 2*\pi*f*t = 360 * 1x10^3 * 510us = 180^o}$. And we know that a small base current at the transistor amplifier produces a current which is phase shifted by 180 degrees.



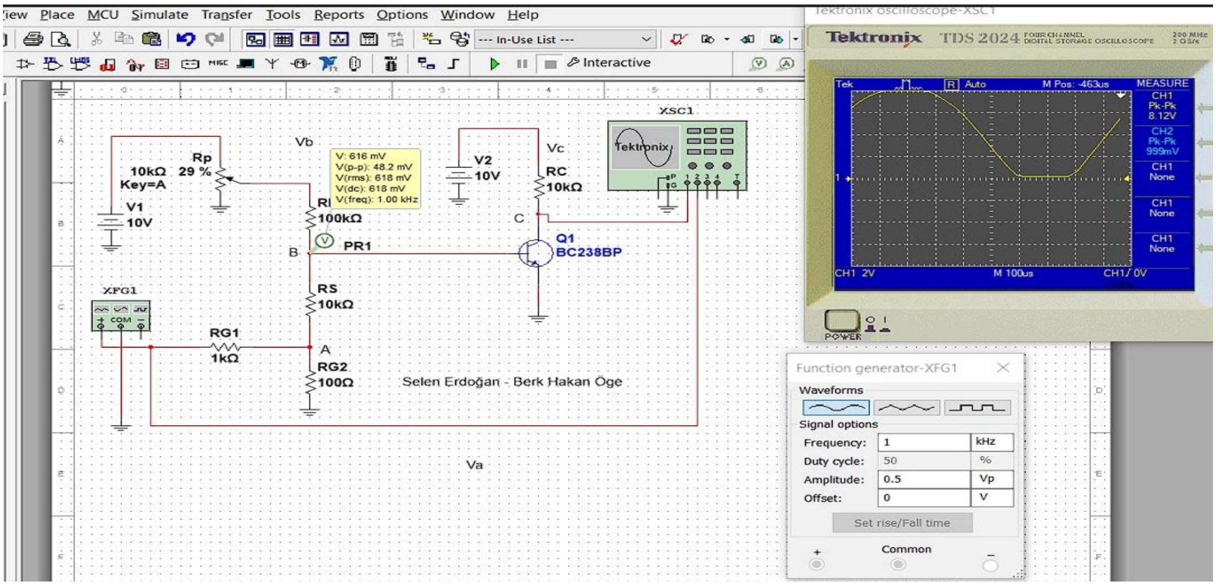
Picture 23 3.2.c gain value starting point

We started our gain calculations from 0.7 $V_{P\text{-}P}$ and slightly increased it each time and noted the gain value slightly going down or staying around the same numbers.



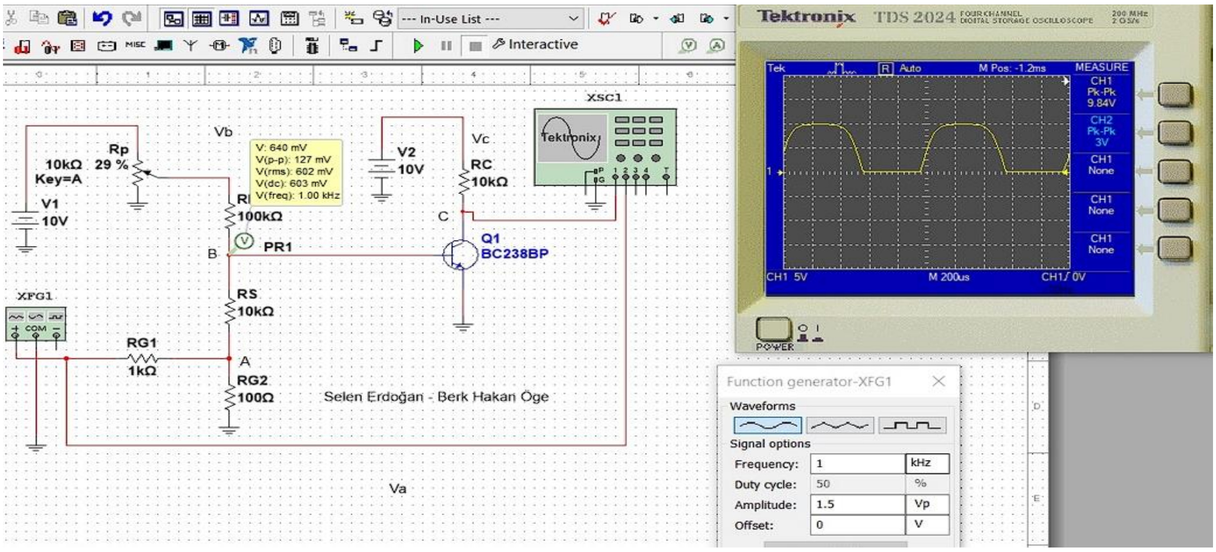
Picture 24 most significant gain change point

When we arrived at the 1$V_{P\text{-}P}$ value our gain shows some high change values while it was around 9.3V now it has gone all the way down to 8.12 V so this is our point for step 3.2.c.



Picture 25 When the negative peak flattens 3.2.d

In this particular part we need to observe our V_C voltage values peak to peak form to start flattening on one of the peaks first and afterwards the other one. In Picture 25 when we hit the V_i value to $1V_{P-P}$ negative peak of output voltage flattens out. This is our first peak to flatten.



Picture 26 positive peak of output voltage flattens 3.2.d

Finally when we keep increasing the V_i after the negative edge flattens around $3V_{P-P}$ and our sine wave of output starts to shape like a square wave. Main reason for it is the DC input above the colector which is 10V and DC coupling setting. When both the inputs clash at the colector output voltage starts to flatten.

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