AN68403

# PSoC® 3 and PSoC 5LP Analog Signal Chain Calibration

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**Software Version: PSoC® Creator™ 2.1 SP1**
**Related Application Notes: AN60263**

**If you have a question, or need help with this application note, contact the author at dasg@cypress.com**

AN68403 explains how to calibrate an analog signal chain by using a calibrated delta sigma ADC and an on-chip EEPROM that is available in PSoC® 3 and PSoC 5LP. An example of a programmable gain amplifier as part of the analog signal chain is also described. AN68403 also shows how the gain and offset errors can be eliminated in the entire signal chain.

## Contents



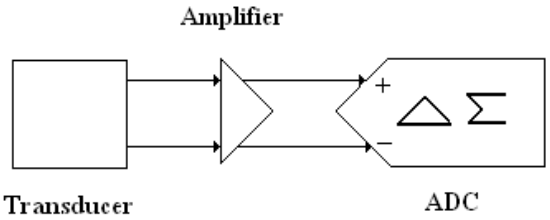
## Introduction

PSoC® 3 and PSoC 5LP have a 20-bit delta sigma analog-to-digital converter (ADC). A typical analog signal chain consists of a sensor whose weak analog signal is amplified and is fed to an ADC, which converts it to a digital value. The amplifier that is used can be a programmable gain amplifier (PGA) or a trans-impedance amplifier (TIA).

An amplifier block has inherent errors; mostly gain and offset errors. Because these errors propagate through the signal chain, the value obtained from the ADC deviates from the actual value. For accurate measurement, calibration of the entire signal chain is required.

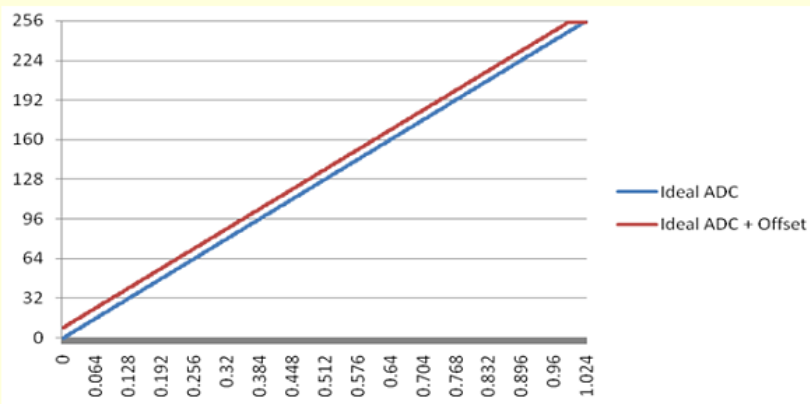
Figure 1 shows a simple analog signal chain that consists of a transducer with output in the form of analog voltage. This analog voltage is passed through an amplifier and then fed to an ADC.

Figure 1. Simple Analog Signal Chain



Offset error is the error that the offset voltage of the ADC creates. Figure 2 shows an ideal ADC transfer characteristic and the one with offset. The characteristics shown are that of an 8-bit ADC that measures 0 to 1.024 V with an offset of 32 mV. The figure shows that the offset causes a fixed additive error in all measurements. Offset also causes a loss of ADC input voltage range. The output is at full capacity at 32 mV (offset) below full scale in the following plot that sets a maximum input of only 992 mV instead of 1.024 V. The output value for a zero input voltage defines the offset of the ADC. The ideal transfer curve passes through the 0 reading when the input voltage is 0.

Figure 2. Offset Error




The following equation gives the ideal ADC transfer function:

$$\text{Voltage} = \text{ADC Count} * \frac{\text{ADC Voltage Range}}{2^n}$$

Any multiplicative factor in this equation, as shown in the following equation, causes a gain error:

$$\text{Voltage} = \text{ADC Count} * \frac{\text{ADC Voltage Range}}{2^n} * k$$

Where n is the resolution of the ADC.

Figure 3 shows a plot of the above two equations with ADC counts along the y-axis and input voltage along the x-axis. The graph shows an 8-bit ADC that measure from 0 to 1.024 V. The blue line represents the ideal transfer characteristic. The red line represents the characteristic with gain error (10%) (put k = 0.9 in the previous equation).

Figure 3. Gain Error

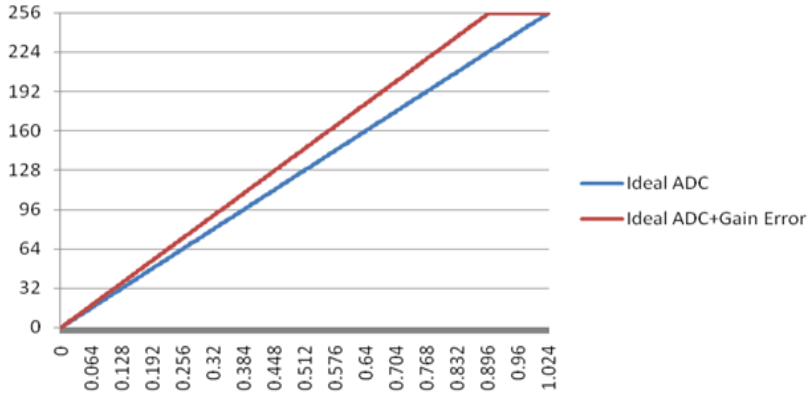
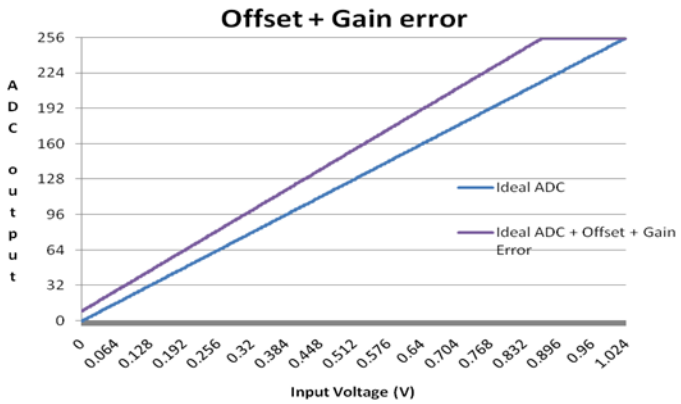


Figure 4 shows the effect of both the gain and offset error in a system. The blue line represents the ideal characteristic without gain and offset error, and the violet line represents the characteristic with gain and offset error.

Figure 4. Gain and Offset Error




## Calibration

Calibration of an analog signal chain involves eliminating the gain and offset errors in the entire signal chain. Based on where and how the calibration is performed, there can be different types of calibration, such as the following:

- Manufacturing calibration
- User calibration
- Run-time calibration

In manufacturing calibration, the analog block under consideration is calibrated during the manufacturing process. This can be during IC manufacturing or assembly manufacturing. For example, the ADC in PSoC 3 is calibrated during IC manufacturing. However, a multimeter is calibrated as an assembly in the multimeter manufacturing plant.

In the user calibration method, the user calibrates the analog block used in the chain. As an example, some cameras have a mode to calibrate the level sensor. The user who initiates this mode does not require any standard except for a level surface. Another user calibration includes the periodic calibration of test equipment.

In the runtime calibration method, the analog block is calibrated in runtime for voltage offsets and system gain errors.

### ADC Calibration

The delta sigma ADC available in PSoC has 20 input ranges that require calibration. This includes ranges Vref*2, Vref, Vref/2, Vref/4, Vref/8, and Vref/16 in differential mode; Vss to Vref, Vref*2, Vdd and Vref*6 in the single-ended mode for 8-15 bits and 16-20 bits resulting in 20 input ranges. Because the calibration memory has room for eight ranges, the range that will most likely be used has been calibrated. The user can calibrate the remaining non-calibrated ranges using one of the calibrated ranges.

Table 1 shows the eight ranges that have been factory calibrated.

Table 1. Calibrated ADC Ranges

| | Resolution | Range |
|---|---|---|
| 1 | 16-20 bits | +/- Vref (Differential) |
| 2 | 16-20 bits | +/- Vref/2 (Differential) |
| 3 | 16-20 bits | +/- Vref/4 (Differential) |
| 4 | 16-20 bits | +/- Vref/16 (Differential) |
| 5 | 8-15 bits | +/- Vref (Differential) |
| 6 | 8-15 bits | +/- Vref/2 (Differential) |
| 7 | 8-15 bits | +/- Vref/4 (Differential) |
| 8 | 8-15 bits | +/- Vref/16 (Differential) |

The ADC calibration is done to correct any gain error that may be caused by process variations. The input gain is a function of the ADC input capacitor ratio. Slight process variations can cause these capacitors to vary in size and, therefore, affect the ADC input gain. The front-end ADC buffer is set to a gain of 1 during the calibration process. If the front-end buffer, gain is chosen to be any value other than 1 and the factory calibration values no longer hold good.

The delta sigma ADC in PSoC has a post processing block that can multiply the ADC result by a value between 0 and 2, with 16 bits of resolution. The registers, GCOR(LSB) and GCORH(MSB), hold the correction value and can be written during runtime to provide a gain correction factor between 0 and 2.

Table 2 shows the format of GCORH and GCOR registers. Each bit is weighted between 1 and 1/ 32768, similar to an unsigned number, but with fractional bit weights.

Table 2. GCOR Registers

| GCORH | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | 1 | 1/2 | 1/4 | 1/8 | 1/16 | 1/32 | 1/64 | 1/128 |

| GCOR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | 1/256 | 1/512 | 1/1024 | 1/2048 | 1/4096 | 1/8192 | 1/16384 | 1/32768 |

The OCOR registers are used to provide offset correction in an ADC. A 24-bit register consisting of 3 bytes, OCOR (LSB), OCORM, and OCORH (MSB), holds the correction value and can be written during runtime to provide offset correction. In single-ended 0-to-2 Vref range, this value has an offset of about half the full scale range for that resolution.

The gain value written into this register is not just a function of a perfect gain of 1. The value written at the beginning is a function of three values:

1. Gain correction to compensate for the Cap Ratio attenuation.
2. Odd decimation for resolutions of 9, 10, 11, 13, 14, and 15 bits.
3. The gain written in the gain calibration memory locations

## Calibrating the Signal Chain

The following is a generic procedure used to calibrate the signal chain:

1. A stable voltage from PSoC's internal voltage DAC (VDAC) is first measured with one of the calibrated ranges. This is value X.
2. The offset voltage of the system is measured by grounding the input terminals. This is value OS.
3. The same voltage from VDAC is passed through the signal chain. The reading obtained is value Y.
4. This reading is offset calibrated by subtracting the offset from it. The offset calibrated reading is value Y'.

   From the previous discussion, it can be written as

   $Y' = Y - OS$ Equation 1
5. The actual gain, G, of the system can be calculated by dividing the offset calibrated reading after passing through the signal chain by the original reading of the VDAC.

   Therefore,

   $G = Y' / X$ Equation 2
6. The ratio of Ideal Gain to Actual Gain of the signal chain is computed. Call the Ideal gain value I.

   Therefore, Ratio = I / G

   The ratio thus obtained is stored in the EEPROM to complete the process of calibration.

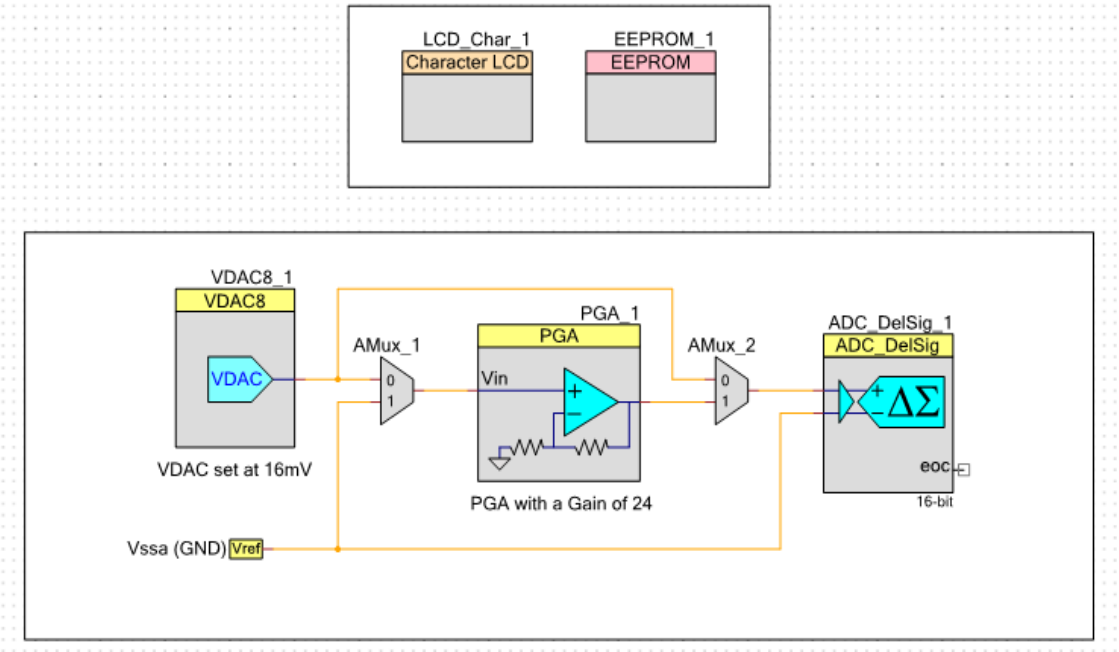
   When the signal chain under consideration is used, the value stored in EEPROM is written into the ADC Gain Correction and Offset Corrections registers.

A PSoC Creator project that writes the gain ratio in the EEPROM is attached. The DAC used in this process need not be accurate, but it should be stable with minimum drift. The calculated ratio is of interest, not the actual value of voltage itself.

A routine is provided at the end. When called in the target project, it writes the gain correction values obtained from the EEPROM to ADC gain correction registers and the offset correction values to the OCOR registers.

Figure 5 on page 5 shows the top design of the project.

Figure 5. Top Design

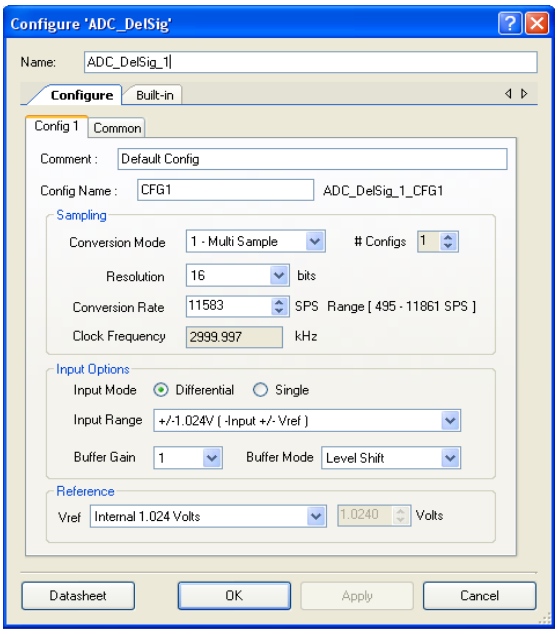



The configuration of individual components used in the project is described in the next section.

### ADC Configuration

The configuration tab of the ADC is as shown in the following figure.

Figure 6. Delta Sigma ADC

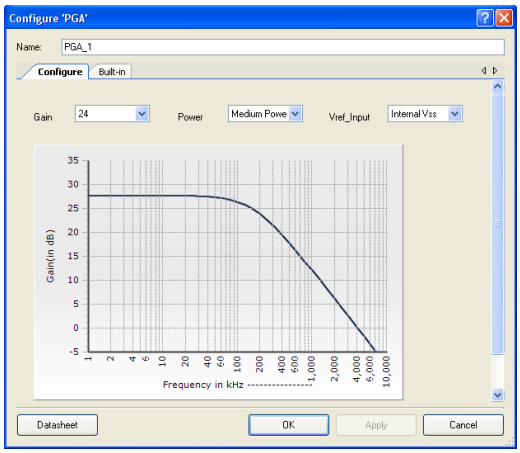



The resolution of the ADC is set to 16 bits, which is used in the differential input mode with an input range of ±Vref. The conversion rate is 11,583 samples per second and the Conversion Mode is set to Multi-Sample mode.

### Programmable Gain Amplifier (PGA)

The PGA used in the top design forms a part of the analog signal chain. The gain of the PGA can be written during runtime. In this case, the gain is set to 24. The Configuration tab is as shown in Figure 7.

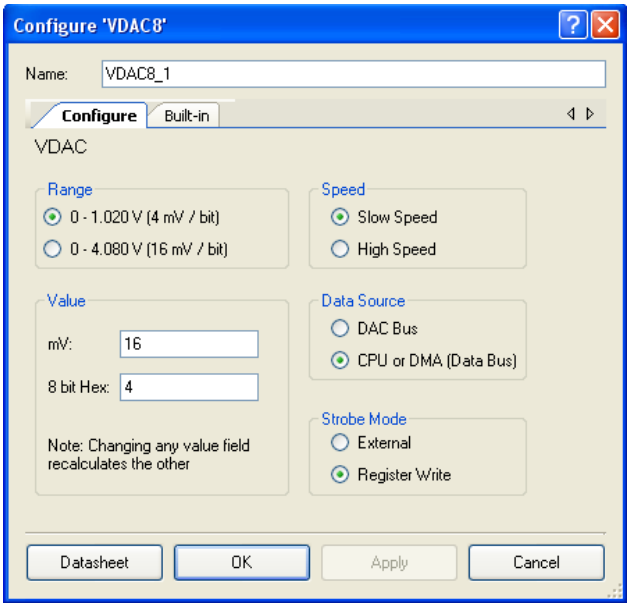
Figure 7. Programmable Gain Amplifier (PGA)



### Voltage DAC (VDAC)

The VDAC component used has been configured to output 16 mV. The Configuration tab is as shown in Figure 8.

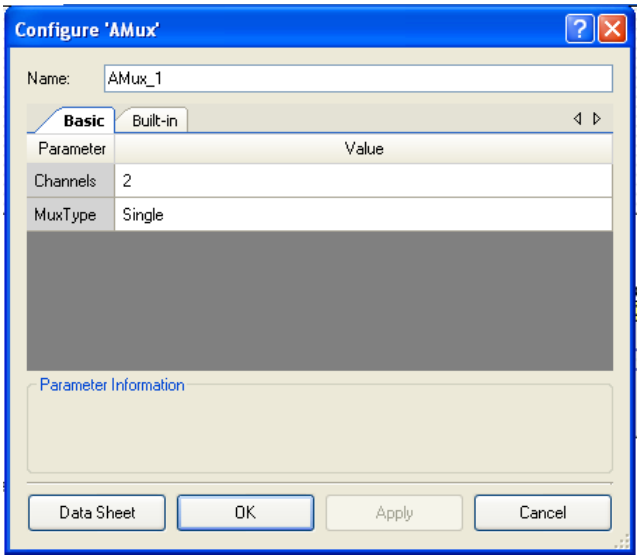
Figure 8. Voltage Digital-to-Analog Converter (VDAC)




### Analog Multiplexer (AMux)

Two software analog multiplexer components are used with two input channel and Single MuxType. This is used to multiplex the analog signals to the PGA and ADC. The Configuration tab is as shown in Figure 9.

Figure 9. Analog Multiplexer (AMux)




On-chip EEPROM is used to store the GCOR and OCOR values computed in the project.

An LCD component is used to display the GCOR and OCOR values computed.

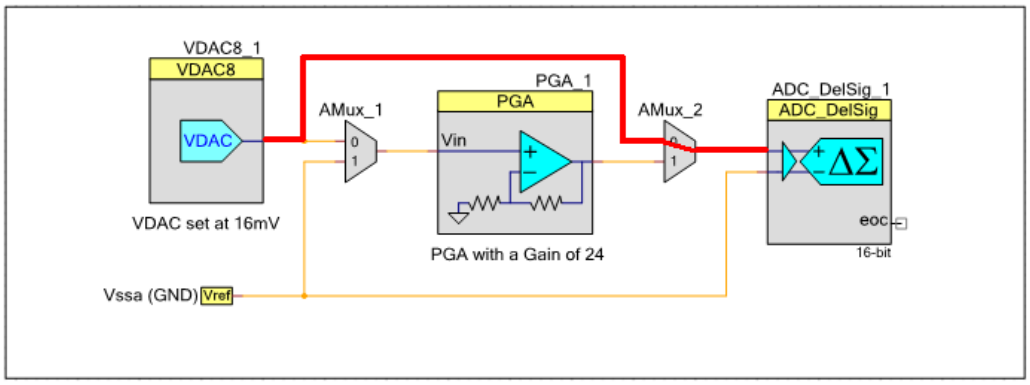
## Calibrating the Analog Signal Chain

When any analog block such as a PGA is cascaded with an ADC, the gain and offset errors of that block affect the entire signal chain. A calibrated ADC is used to calibrate the entire signal chain and compensate for the errors introduced by the analog block. The following procedure is used to calibrate the analog signal chain. See Figure 5 for the complete schematic of the project.

### Step 1

AMux_2 channel 0 is selected. This connects the VDAC output to the ADC. PGA is not used in the signal path in this configuration. This gives a direct reading of VDAC voltage. The samples are averaged. As discussed previously, consider this to be value X. Figure 10 on page 7 shows the signal flow for this step where the red line shows the path taken.

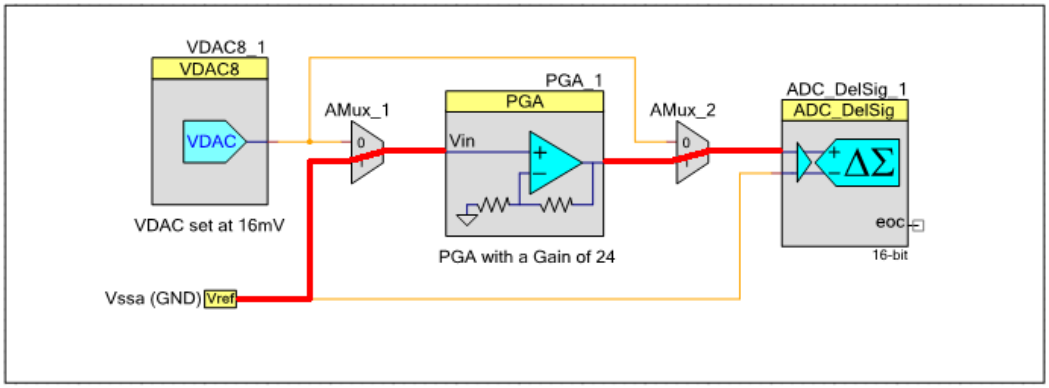
Figure 10. VDAC Direct Measurement




**Step 2**

AMux_1 channel 1 and AMux_2 channel 1 are selected, which connects the input terminal of the PGA to ground. This reading corresponds to the offset error of the PGA. Consider this to be value OS. The red line in Figure 11 shows the path taken by the analog signal.

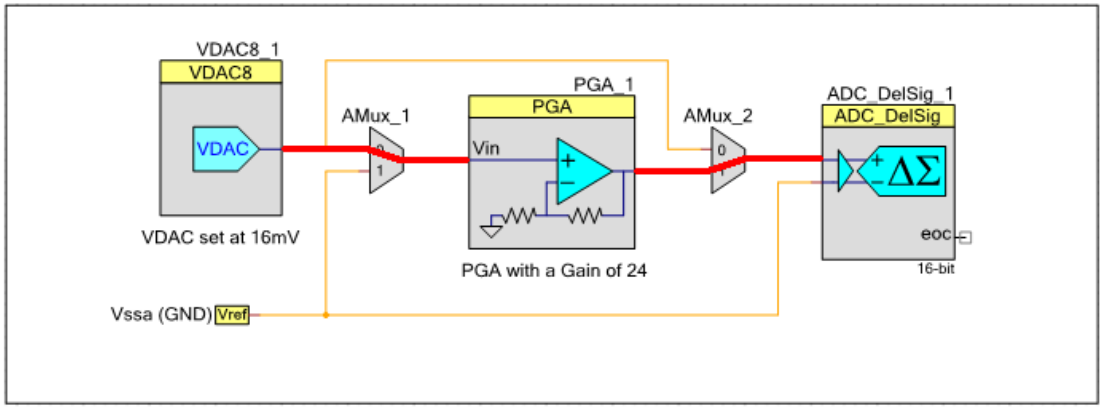
Figure 11. Offset Error Measurement




**Step 3**

The GCOR is disabled. AMux_1 channel 0 and AMux_2 channel 1 are selected, that passes the VDAC output through the PGA. This gives the PGA output that has gain as well as offset error. Consider this measured value as value Y. The red line in Figure 12 shows the path taken by the analog signal.

Figure 12. VDAC Output Passes through PGA



**Step 4**

Offset error is removed from this reading by subtracting the value obtained in Step 2 from that of Step 3. This measurement corresponds to a value free from offset error. Consider this as Y'. From the definition, the value of Y' can be computed as follows: Y' = Y – OS

**Step 5**

Actual gain of the PGA is obtained by dividing the offset free measurement Y' with the direct VDAC reading obtained in Step 1, X. Consider the actual gain as G. It is mathematically written as:

$$G = Y' / X$$

**Step 6**

Ideal gain of the PGA, I (which in this case is 24), is divided by the actual gain obtained, G. This is the ratio that must be written into the EEPROM.

$$Ratio = I / G = 24 / G$$

**Step 7**

The gain ratio and the offset error, OS, is written to the EEPROM.

**Step 8**

PSoC 3 or PSoC 5LP has a switched capacitance (SC) continuous time (CT) block, which is a general-purpose block, constructed on a rail-to-rail amplifier with arrays of switches, capacitors, and resistors. PGA is a CT opamp with selectable taps for input and feedback resistors. There are four SC/CT blocks available in PSoC 3 or PSoC 5LP. Because the gain and offset errors of the PGA differs depending upon the SC block used, it is necessary to force the fixed SC block for a particular design. This is done on the directives tab of *.cydwr* of the project.

Figure 13 shows the settings used to force the SC3 block.

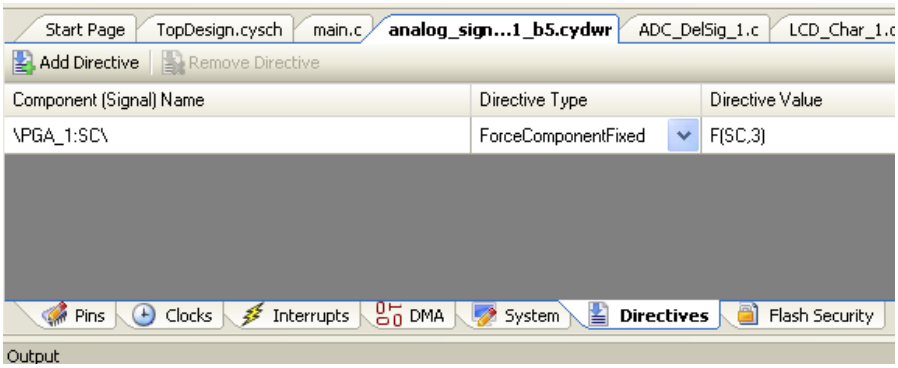
In the 'Component (Signal) Name' tab, the name of the component is written, which in this case is PGA_1 followed by SC, which is separated by a colon. This is written between backslashes.

In the Derive Type, 'ForceComponentFixed' is chosen to force one specific SC block among the available four blocks (0,1,2,3) to implement the PGA.

The 'Directive Value' tab is used to select the required SC block to be used for the given component. In this case, SC3 is chosen to implement PGA_1; therefore, the Directive Value is F(SC,3).

The placement of PGA_1 can be confirmed by verifying the report file (*.rpt*) in the project.

Figure 13. Forcing the SC Block for PGA




**Step 9**

The gain ratio and offset error value thus obtained is written into the on-chip EEPROM.

**Step 10**

In the final target project, where the particular signal chain is to be used; the gain ratio and the offset error values are read from EEPROM.

**Step 11**

The gain ratio read from EEPROM is written to the GCOR. The offset error value read is added to the current value of OCOR and the result is written back to the OCOR register. The GCOR is enabled.

There are three gain correction registers that set the correct gain correction value and one gain correction bit that enables gain correction.

- The registers DEC.GCOR and DEC.GCORH set the actual gain correction value.
- Register DEC.GVAL specifies the number of bits that are valid out of the 16 bits written in the DEC.GCOR and DEC.GCORH registers starting from the LSB.

Number of valid bits is the value written in the GVAL register + 1. If five bits are valid, the binary point is automatically implied between the fourth and fifth digit. For example, values of 0b11000111 and 0b00000101 in GCORH and GCOR registers, respectively, with a value of 0b00001000 in the GVAL register mean a gain correction factor of 1.00000101 (9 valid bits starting from LSb with binary point between eighth and ninth bits) in binary, which corresponds to a decimal value of 1.01953125. Use the following procedure to find the appropriate register values:

Find the gain correction value (see Step 2).

Convert the value to the closest 16-bit binary number. For a gain correction factor of 1.000069, the closest 16-bit binary value is 1.00000000000001(1.000061).

Count the number of digits in the resulting binary number (ignore trailing zeroes). This value minus 1 is written to the gain DEC.GVAL register. In this case, there are 16 valid bits; therefore, the DEC.GVAL register is written with 0x0F(15).

Write the binary value (ignoring the binary point) in the GCOR registers appending zeroes to the MSB until it is a 16-bit value.

Enable gain correction by setting the gain correction enable bit in DEC.CR register:

**DEC.CR | = 0x10**

## Routine to Write into GCOR and OCOR from EEPROM

Let gcor_new be the GCOR value read from EEPROM and let ocor_old be the old OCOR value in the final project that uses the analog signal chain. The ocor_new value is computed by adding the ocor_old and the value read from EEPROM.

The value written into GVAL is 15 (0x0F). The following is the routine to be written in the project that uses the analog signal chain and reads the GCOR and OCOR values written in the EEPROM.

(Assume that the name of ADC is ADC_DelSig_1)

```
ocor_old = (int32)(ADC_DelSig_1_DEC_OCOR_REG) + ((int32)
(ADC_DelSig_1_DEC_OCORM_REG) << 8) + ((int32)
(ADC_DelSig_1_DEC_OCORH_REG) <<16);
ocor_new = ocor_old + ocor_error;

ADC_DelSig_1_DEC_OCOR_REG = (int8) (ocor_new);
ADC_DelSig_1_Dec_OCORM_REG=(int8)(ocor_new>>8);
ADC_DelSig_1_DEC_OCORH_REG=(int8)(ocor_new>>16);
ADC_DelSig_1_DEC_GCOR_REG=(int8)(gcor_new);
ADC_DelSig_1_DEC_GCORH_REG=(int8)(gcor_new>>8);
ADC_DelSig_1_DEC_GVAL_REG = 0x0f;
ADC_DelSig_1_DEC_CR_REG |= 0x10;
```

## Summary

The analog signal chain can be calibrated by using a VDAC, EEPROM, and a calibrated range of delta sigma ADC in PSoC 3 and PSoC 5LP.

## Document History

Document Title: PSoC® 3 and PSoC 5LP Analog Signal Chain Calibration

Document Number: 001-68403

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 3205526 | DASG | 03/23/2011 | New application note |
| *A | 3441350 | DASG | 11/21/2011 | Template update<br>Updated Software Version to PSoC Creator™ 2.0<br>Updated snap-shots of ADC, PGA and VDAC<br>Conversion rate of ADC is changed from 10,000 to 11,583. |
| *B | 3564143 | DASG | 03/28/2012 | Updated author's contact information according to the template.<br>Added definition of Offset error and Gain error.<br>The reference made to AN60263 for gain and offset error definition is removed.<br>The project is updated with latest components. |
| *C | 3642517 | DASG | 06/11/2012 | Updated template to current CY standards.<br>Updated associated project. |
| *D | 3819305 | DASG | 11/22/2012 | Updated for PSoC 5LP |
| *E | 3889066 | DASG | 01/29/2013 | Corrected headers and footers<br>Sunset review |

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