Middle East Technical University - Department of Computer Engineering

CENG 232

Logic Design

Spring 2018-2019
Lab Assignment 2

Due date: Sunday, March 24, 2019, 23:59hrs

1 Introduction

This laboratory aims to get you familiar with some of the most important IC components like multiplexers and decoders. You will draw the circuit using Logisim tool with the given gates.

The logisim submission will be different from the demo circuit you will build in lab. It will contain an additonal output and related IC components to generate that output.

2 IC Pool

- 74LS08 (AND)
- 74LS32 (OR)
- 74LS04 (Inverter)
- 74LS02 (NOR)
- 74LS00 (NAND)
- 74LS153 (Multiplexer)
- 74LS86 (XOR)
- 74LS138 (Decoder)

3 Lab Work

In this lab, you will be given three 2-bit numbers, A, B, S as input and you will produce the 3-bit output X. Additionally, for the **logisim part** you will produce an 8-bit output Y. Requirements are given as follows:

- The digits of input **A** should be labelled as A1 and A0 where A0 is the least significant digit and A1 is the most significant digit.

- The digits of input **B** should be labelled as B1 and B0 where B0 is the least significant digit and B1 is the most significant digit.

- The digits of input **S** should be labelled as S1 and S0 where S0 is the least significant digit and S1 is the most significant digit.

- Your output **X** is a 3-bit number which should be labelled as X2, X1 and X0 where X0 is the least significant digit and X2 is the most significant digit.

- Your 8-bit output **Y** [Y7..Y0] will be used to display decimal numbers corresponding to binary representation of X. Only one bit of Y is set at a time. Y0 means 0, Y5 means 5 (or -3, see Figure 1).

  If X is 110, Y is 01000000 or if X is 011, Y is 00001000

- You are expected to perform the following 4 tasks depending on the value of S:

  - If S is 0 the outputs will be A-B.
  - If S is 1 the outputs will be max(A,B).
  - If S is 2 the outputs will be 2*B.
  - If S is 3 the outputs will be 2*A+1.

3.1 Implementation of A-B

A-B will return a 3 bit number and you will use X to represent it. For the negative values generated from A-B you can use Figure- 1 for the mapping of negative values to positive values in 3 bit representation.
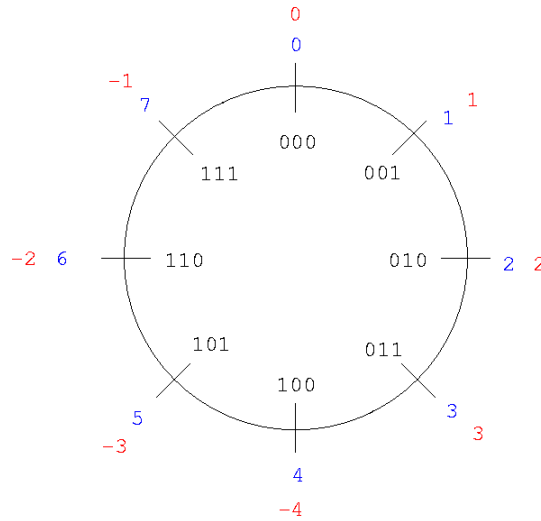

Figure 1: Mapping of negative numbers to positive numbers in 3 bit representation.

Example: $(00)_2$ - $(01)_2 \rightarrow (111)_2$, $(11)_2$ - $(10)_2 \rightarrow (010)_2$

3.2 Implementation of max(A,B)

This will always print the larger number between A and B to X.

Example: $max((10)_2, (01)_2) \rightarrow (010)_2$, $max((00)_2, (11)_2) \rightarrow (011)_2$

3.3 Implementation of 2*A+1 and 2*B

This will calculate the expression (decimal multiplication and addition) and set the 3 bit value to X.

Example: $2 * (10)_2 + 1 \rightarrow (101)_2$, $2 * (01)_2 \rightarrow (010)_2$

4 Logisim-Only Part

In your logisim submissions, you also need to display the decimal conversion of X in the output Y for every task. **You will not build the circuit components that generate output Y in the lab.**

5 Free Session

There will be a *free session week* after your homework is announced. You will have 2 hours in your free session slot. During the free session, you will try to build your circuit on a breadboard by using IC components, and you will practice how to handle possible problems related to physical circuit.

6 Demo Session

There will be a 2-hour-long *demo session week* following the free session week. In the demo session:

- You will take a short quiz about the logic concepts that involve the coverage of this lab.
- You will reconstruct your circuit on your breadboard (without the output Y).
- You will show that the circuit drawn in Logisim works as specified (without the output Y).

7 Labelling Specifications

- You have to use **pins** for your inputs and outputs. Only set **label property** of the **pin** objects, do not add a **label object**.
- Your input pins should be labelled as A1, A0, B1, B0, S1 and S0.
- Your output pins should be labelled as X2, X1, X0, Y7, Y6, Y5, Y4, Y3, Y2, Y1 and Y0.
- Label properties are case-sensitive. Note that all labels consist of an uppercase letter followed by a number. **Please be very careful on correct naming of labels.**
- If you need to feed any input with a constant value, you can use a constant gate. This gate is under CENG232 gates. We will only set values for A1, A0, B1, B0, S1 and S0.
- You will receive **20% penalty** if you fail to obey these specifications.

8 Deliverables

- Submit the circuit named e1234567.circ prepared in Logisim, which is your preliminary work, until the specified deadline. Do not forget to replace e1234567 with your 7-digit student ID.
- The evaluation of the submission will be a **black-box test**.
- In demo session, you will reconstruct and show that the circuit drawn in Logisim works. This part will be graded in lab.
- You should use CENG version of Logisim which is available on ODTUClass course page. Circuits designed with other Logisim versions, other tools or that are not named properly **will not be graded**!
- Please note that submission of a working circuit is a must to attend DEMO lab sessions.

9 What to Bring in the Lab

- Print-out of submitted file of the circuit.
- Chips and their data-sheets. www.alldatasheet.com
- Pencil, as you will have a quiz at the very beginning of the DEMO lab.

10 Cheating Policy

All the lab work should be individual and there is zero tolerance policy for cheating. See the course website for further information about cheating policy.

11 References

CENG Logisim Version