FPGA Ethernet Packet Parser – Case Study Report

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1. Introduction

This project focuses on implementing an FPGA-based hardware module that parses Ethernet packets received through an AXI-Stream interface. The goal is to extract Ethernet, IPv4, and UDP headers from incoming frames and forward the payload without any modifications.

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2. Design Approach

Packet parsing is controlled by the following FSM

- **IDLE**: Waits for the beginning of a new packet.
- **ETHERNET**: Parses the 14-byte Ethernet header (dst_mac, src_mac, ethertype).
- **IPV4**: Extracts source IP, destination IP, and protocol fields from the IPv4 header.
- **UDP**: Extracts source port, destination port, and UDP length.
- **PAYLOAD**: Forwards the remaining payload data without modification.

Once parsing is completed, the parsed_valid_pulse signal goes high for exactly one clock cycle, indicating that the parsed header information is valid. The FSM operates in full compliance with the AXI-Stream protocol, synchronized via tvalid, tready, and tlast signals.

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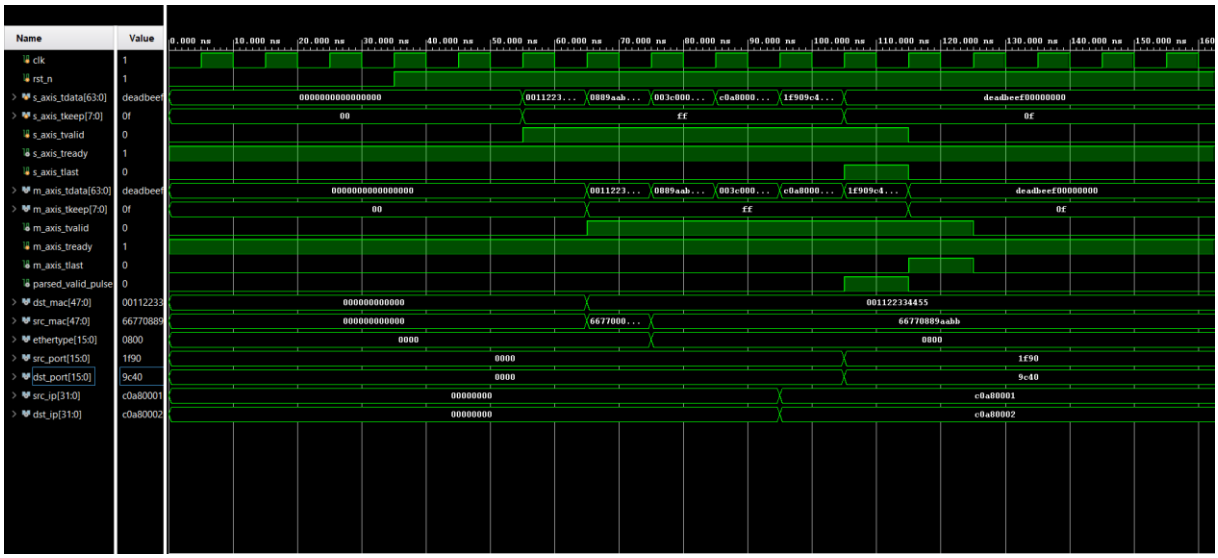
3. Test Results

The design was verified using a testbench simulation based on the following example packet:

send_word(64'h0011223344556677, 8'hFF, 0); // dst_mac = 00:11:22:33:44:55, partial src_mac = 66:77
send_word(64'h889AABB080045000, 8'hFF, 0); // src_mac continued: 88:9A:AB:BB, ethertype = 0x0800,
send_word(64'h003C000040004011, 8'hFF, 0); // protocol = 0x11 (UDP)
send_word(64'hC0A80001C0A80002, 8'hFF, 0); // src_ip = 192.168.0.1, dst_ip = 192.168.0.2
send_word(64'h1F909C40001C0000, 8'hFF, 0); // src_port = 0x1F90, dst_port = 0x9C40
send_word(64'hDEADBEEF00000000, 8'h0F, 1); // UDP payload = 0xDEADBEEF, tkeep = 0x0F (4 bytes), tlast = 1



Observed from the simulation that the header fields were extracted correctly.

- dst_mac: 00:11:22:33:44:55
- src_mac: 66:77:88:9A:AB:BB
- ethertype: 0x0800
- src_ip: c0.a8.00.01 (192.168.0.1 in hexadecimal)
- dst_ip: c0.a8.00.02 (192.168.0.2 in hexadecimal)
- src_port: 0x1F90
- dst_port: 0x9C40
- parsed_valid_pulse: Asserted for one cycle immediately after the UDP header was parsed

These results meet the following implementation requirements:

- The parsed_valid_pulse is generated for exactly one clock cycle.
- All packets are parsed independently, which prevents problems when they arrive out of order.
- Synchronization between AXI-Stream data and header extraction is properly maintained.

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4. Conclusion

This project successfully implements an AXI-Stream Ethernet packet parser capable of extracting key headers and forwarding the payload in real-time.