Prof. Dr. Berna Örs Yalçın **Due Date:** 26.01.2025

EHB205 Introduction to Logic Design
Homework 5

Part 1

1) A sequential circuit has two *JK* flip-flops *A* and *B* and one input *x* . The circuit is described by the following flip-flop input equations:

$JA = x$ $KA = b$
$JB = x$ $KB = a'$

a) Derive the state equations $A(t + 1)$ and $B(t + 1)$.
b) Draw the state diagram of the circuit.

2) A sequential circuit has two *JK* flip-flops *A* and *B*, two inputs *x* and *y*, and one output *z* . The flip-flop input equations and circuit output equation are

$JA = bx + b'y'$ $KA = b'xy'$
$JB = a'x$ $KB = a + xy'$
$z = ax'y' + bx'y'$

a) Draw the logic diagram of the circuit.
b) Tabulate the state table.
c) Derive the state equations for *A* and *B* .

3) Design a sequential circuit with two *D* flip-flops *A* and *B*, and one input *x_in* .

a) When *x_in* = 0, the state of the circuit remains the same. When *x_in* = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats.
b) When *x_in* = 0, the state of the circuit remains the same. When *x_in* =1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeats.

4) Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output.

5) Design a sequential circuit with two *JK* flip-flops *A* and *B* and two inputs *E* and *F* . If *E* = 0, the circuit remains in the same state regardless of the value of *F* . When *E* = 1 and *F* = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When *E* = 1 and *F* = 0, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

Part 2

1) A JK latch (http://www.asic-world.com/digital/seq4.html) will be implemented.
    a. Create a new project as explained in your first homework.
    b. Write the VHDL code. Save this file by giving name as "JK_Latch.vhd".
    c. Add your "JK_Latch.vhd" by "Add Sources", "Add or create design sources" to your project.
    d. Produce the RTL schematic of your design.
    e. Implement JK latch on an FPGA using "implement", "place and route ".
    f. Write a test bench file with name "JK_Latch_tb.vhd" to test your design.
    g. Add your "JK_Latch_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.
    h. Simulate your circuit by using the "post place and route simulation" option in "simulation".
2) A JK flip-flop (https://www.geeksforgeeks.org/master-slave-jk-flip-flop/) will be implemented.
    a. Write the VHDL code. Save this file by giving name as "JK_FF.vhd".
    b. Add your "JK_FF.vhd" by "Add Sources", "Add or create design sources" to your project.
    c. Produce the RTL schematic of your design.
    d. Implement JK latch on an FPGA using "implement", "place and route ".
    e. Write a test bench file with name "JK_FF_tb.vhd" to test your design.
    f. Add your "JK_FF_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.

g. Simulate your circuit by using the “post place and route simulation” option in “simulation”. Show that your circuit satisfies the truth table given on slides of the course.

3) A circuit which detects the paterns 10-10-11 or 11-00-01 from its 2-bit input and gives 1 at its 1-bit output when it detects one of the required paterns.
   a. Draw the state diagram.
   a. Write the VHDL code using the examples given in https://www.xilinx.com › HDL-Design › VHDL › docs-pdf › lab10, https://vhdlguide.readthedocs.io/en/latest/vhdl/fsm.html, https://surf-vhdl.com/how-to-implement-a-finite-state-machine-in-vhdl/. Save this file by giving name as “Pattern_Detector_D_FF.vhd”.
   b. Add your “Pattern_Detector_D_FF.vhd” by “Add Sources”, “Add or create design sources” to your project.
   c. Produce the RTL schematic of your design.
   d. Implement your circuit on an FPGA using “implement”, “place and route ”.
   e. Write a test bench file with name “Pattern_Detector_D_FF_tb.vhd” to test your design.
   f. Add your “Pattern_Detector_D_FF_tb.vhd” by “Add Sources”, “Add or create simulation sources” to your project.
   g. Simulate your circuit by using the “post place and route simulation” option in “simulation”.
4) The same circuit in (3) will be implemented using JK flip-flops.
   a. Assign a code to each state.
   b. Draw the state table with JK flip flop inputs.
   c. Reduce the flip-flop input and output functions.
   d. Draw the circuit.
   h. Write the VHDL code. Save this file by giving name as “Pattern_Detector_JK_FF.vhd”.
   i. Add your “Pattern_Detector_JK_FF.vhd” by “Add Sources”, “Add or create design sources” to your project.
   j. Produce the RTL schematic of your design.
   k. Implement your circuit on an FPGA using “implement”, “place and route ”.
   l. Write a test bench file with name “JK_FF_tb.vhd” to test your design.
   m. Add your “Pattern_Detector_JK_FF_tb.vhd” by “Add Sources”, “Add or create simulation sources” to your project.
   a. Simulate your circuit by using the “post place and route simulation” option in “simulation”.