Prof. Dr. Berna Örs Yalçın **Due Date:** 30.11.2024

EHB205 Introduction to Logic Design
Homework 3

Part 1

1) Design a combinational circuit with three inputs, x, y and z, and three outputs, A, B, C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.
2) A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.

Part 2

1) We will design a circuit called half adder (HA) which adds two 1-bit numbers, a, b and produces 2-bit output, c.
   a. Draw the truth table of the circuit.
   b. Find the Boolean functions of each bit of the output.
   c. Optimize the Boolean functions of each bit of the output.
   d. Draw the logic diagram of the optimized circuits.
   e. Write the VHDL code of the logic diagrams by using "Dataflow modeling" method using the examples given in,
   https://www.electronics-tutorial.net/VHDL/Introduction/Data-Flow-Modeling/
   https://technobyte.org/vhdl-dataflow-modeling-architecture-style/
   https://buzztech.in/vhdl-modelling-styles-behavioral-dataflow-structural/
   f. Simulate the circuit that you have designed in 1.e. Prepare a simulation waveform for you report.
   g. Produce the RTL schematic for the circuit that you have designed in 1.e.
2) We will design a circuit called full adder (FA) which adds three 1-bit numbers, a, b, c and produces 2-bit output, d.
   a. Draw the truth table of the circuit.
   b. Find the Boolean functions of each bit of the output.
   c. Optimize the Boolean functions of each bit of the output.
   d. Draw the logic diagram of the optimized circuit.
   e. Write the VHDL code of the logic diagrams by using "Dataflow modeling".
   f. Simulate the circuit that you have designed in 2.e. Prepare a simulation waveform for you report.
   g. Produce the RTL schematic for the circuit that you have designed in 2.e.
3) We will design a circuit called ripple carry adder (RCA) which adds two 4-bit positive integers, A, B and produces 5-bit output, C.
   a. Draw the logic diagram of the circuit by using one HA and 4 FAs.
   b. Write the VHDL code of the logic diagrams by using "Structural modeling" using the examples given in
   https://surf-vhdl.com/vhdl-syntax-web-course-surf-vhdl/vhdl-structural-modeling-style/
   https://www.electronics-tutorial.net/VHDL/Introduction/Structural-modeling/
   https://technobyte.org/vhdl-structural-modeling-style-architecture/
   https://link.springer.com/chapter/10.1007/978-1-4615-3216-3_7

c. Produce the RTL schematic for the circuit that you have designed in 3.b.
d. Simulate the circuit that you have designed in 3.b.

References

1) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010.
2) Perry, Douglas L, **VHDL,** New York : McGraw-Hill, c1991
3) Botros, Nazeih, **HDL with digital design : VHDL and Verilog,** Dulles, Virginia : Mercury Learning and Information, [2015]
4) Vahid, Frank, V**HDL for digital design,** Hoboken, N.J. : Wiley, c2007
5) Short, Kenneth L, **VHDL for engineers, U**pper Saddle River, NJ : Pearson Prentice Hall, c2009
6) Coelho, David R., **The VHDL Handbook,** Boston, MA : Springer US, 1989
7) Lipsett, Roger., **VHDL: Hardware Description and Design,** Boston, MA : Springer US, 1989