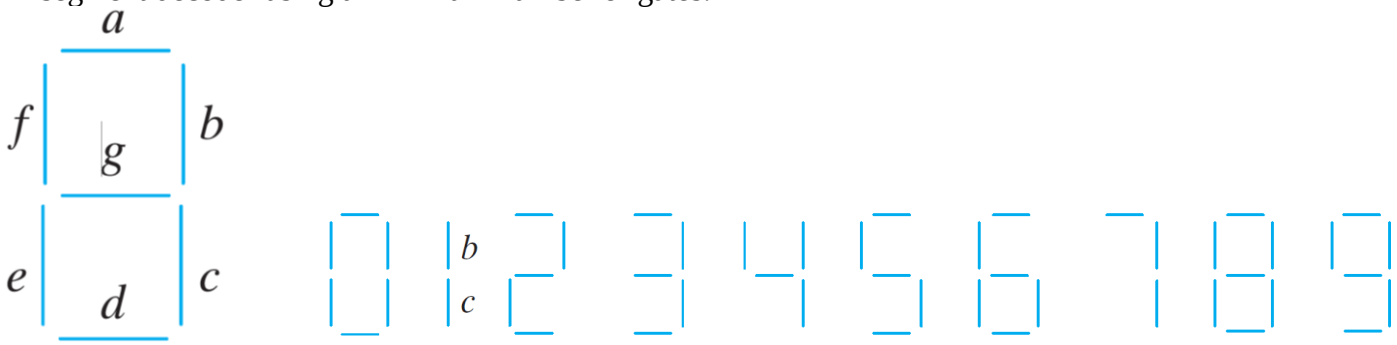
Prof. Dr. Berna Örs Yalçın **Due Date:** 15.12.2024

EHB205 Introduction to Logic Design
Homework 4

Part 1

1) An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in binary coded decimal (BCD) to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder *(a, b, c, d, e, f, g)* select the corresponding segments in the display, as shown in Fig. 1(a). The numeric display chosen to represent the decimal digit is shown in Fig. 1(b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates.



(a) Segment designation (b) Numerical designation for display

Figure 1.

2) Design a four-bit combinational circuit 2's complementor. (The output generates the 2's complement of the input binary number.) Show that the circuit can be constructed with exclusive-OR gates. Can you predict what the output functions are for a five-bit 2's complementor?

Part 2

1) Create a new project as explained in your first homework.

2) You will design a circuit, COMP_1_bit, for comparing two 1-bit positive integers, a and b. The outputs are x, y, z as defined below:
   - a>b ⇒ x=1, y=0, z=0
   - a=b ⇒ x=0, y=1, z=0
   - a<b ⇒ x=0, y=0, z=1

   a) Write a VHDL code for COMP_1_bit. Save this file by giving name as "COMP_1_bit.vhd"
   b) Add your "COMP_1_bit.vhd" by "Add Sources", "Add or create design sources" to your project.
   c) Produce the RTL schematic of your design.
   d) Write a test bench file with name "COMP_1_bit_tb.vhd" to test your design.
   e) Add your "COMP_1_bit_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.
   f) Simulate your design.

3) You will design a circuit, POZ_COMPARE, for comparing two 4-bit positive integers, A and B. The block diagram for comparing 4-bit numbers is shown in Fig. 2. The outputs are X, Y, Z as defined below:
   - A>B, then X=1, Y=0, Z=0
   - A=B, then X=0, Y=1, Z=0
   - A<B, then X=0, Y=0, Z=1

Figure 2 is the block diagram of the circuit which is used to calculate the following equations.

$$X = x_3 + y_3x_2 + y_3y_2x_1 + y_3y_2y_1x_0$$

$$Y = y_3y_2y_1y_0$$
$$Z = z_3 + y_3z_2 + y_3y_2z_1 + y_3y_2y_1z_0$$

a) Write a VHDL code for CONNECT. Save this file by giving name as "CONNECT.vhd"
b) Add your "CONNECT.vhd" by "Add Sources", "Add or create design sources" to your project.
c) Produce the RTL schematic of your design.
d) Write a VHDL code for a CON_COMP_1_bit by using COMP_1_bit and CONNECT as building blocks using "Structural modeling" as in the examples given in

https://surf-vhdl.com/vhdl-syntax-web-course-surf-vhdl/vhdl-structural-modeling-style/
https://www.electronics-tutorial.net/VHDL/Introduction/Structural-modeling/
https://technobyte.org/vhdl-structural-modeling-style-architecture/
https://link.springer.com/chapter/10.1007/978-1-4615-3216-3_7

Save this file by giving name as "CON_COMP_1_bit.vhd".

e) Add your "CON_COMP_1_bit.vhd" by "Add Sources", "Add or create design sources" to your project.
f) Write a VHDL code for POZ_COMPARE by using COMP_1_bit and CON_COMP_1_bit as building blocks using "Structural modeling". Save this file by giving name as "POZ_COMPARE.vhd"
g) Add your "POZ_COMPARE.vhd" by "Add Sources", "Add or create design sources" to your project.
h) Produce the RTL schematic of your design.
i) Write a test bench file with name "POZ_COMPARE_tb.vhd" to test your design.
j) Add your "POZ_COMPARE_tb.vhd" by "Add Sources", "Add or create simulation sources" to your project.
k) Simulate your design.

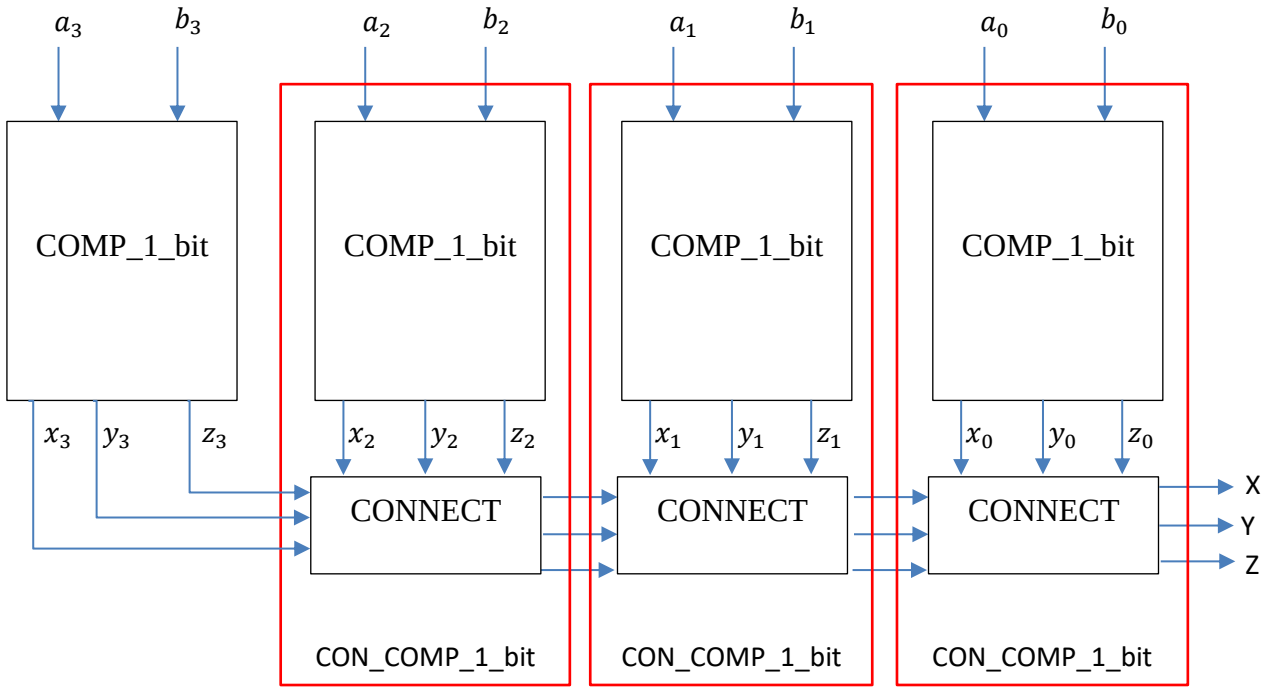


Figure 2

References

1) Frank Vahid, **Digital design, with RTL design, VHDL, and Verilog,** Hoboken, NJ : John Wiley, 2010.
2) Perry, Douglas L, **VHDL,** New York : McGraw-Hill, c1991
3) Botros, Nazeih, HDL with digital design : VHDL and Verilog, Dulles, Virginia : Mercury Learning and Information, [2015]
4) Vahid, Frank, VHDL for digital design, Hoboken, N.J. : Wiley, c2007
5) Short, Kenneth L, VHDL for engineers, Upper Saddle River, NJ : Pearson Prentice Hall, c2009
6) Coelho, David R., The VHDL Handbook, Boston, MA : Springer US, 1989
7) Lipsett, Roger., VHDL: Hardware Description and Design, Boston, MA : Springer US, 1989