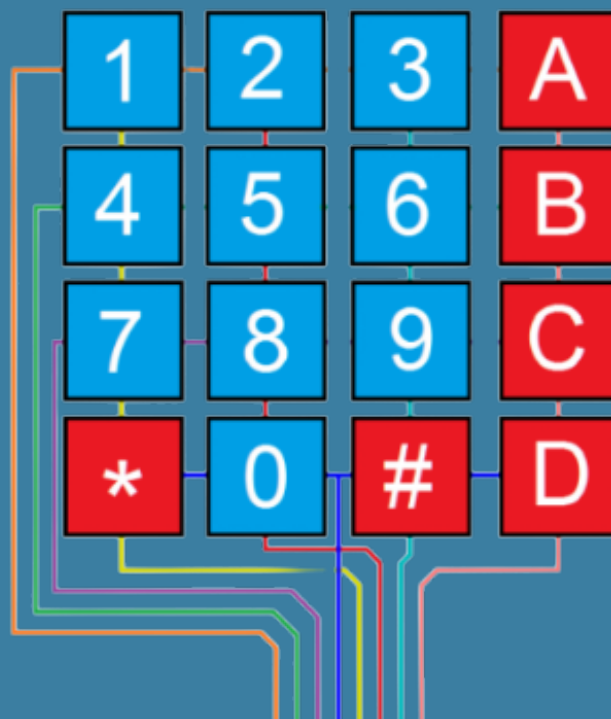


ECE363 Final Project:

Security Control System

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1 Introduction

A chemical plant located out of Lincoln, Nebraska has experienced frequent break-ins over the past year. The various attempts, both successful and not, have targeted Master Lock padlocks used to safe guard their facility entrances. The owner outlined the need to have a 4 number combination that will reset its state when the incorrect combination is detected. They also emphasized the importance of having the enable button which allows the owner to disable the keypad once the work day is over; this ensures malicious attacks are impossible due to the keypad being inoperable in the disabled state. Our hopes are to deliver on these specifications and design a simple yet effective security system for the owner of this company.

2 Design Specifications

This Keypad will prevent the valuable chemicals from being stolen through a tough security system. The owner of the company has reached out to us in hopes of us designing a digital system that has 11 buttons: 10 for inputting the combination numbers, and one for enabling/disabling the system. The system will be connected to lights that will display whether the system is enabled or disabled.

3 Design Development

Before writing any System Verilog code, we understood the importance of outlining all possible states within our system through an FSM (Finite State Machine) Diagram. Upon laying out all possible states, we found there to be nine total states with state zero being the initial state. We also accounted for the reset and enable inputs which would prevent state change and reset to initial state, respectively. Upon outlining every state transition, we approached writing our code by using case-statements which would assign the next state based on the number inputted on the keypad. The present state would then be updated on the clock edge. The output of the system is a one bit value labeled "correct" which would be updated on every present state change. Therefore, "correct" is only assigned the value of 1 when it is in the state after the fourth correct digit is inputted on the keypad.

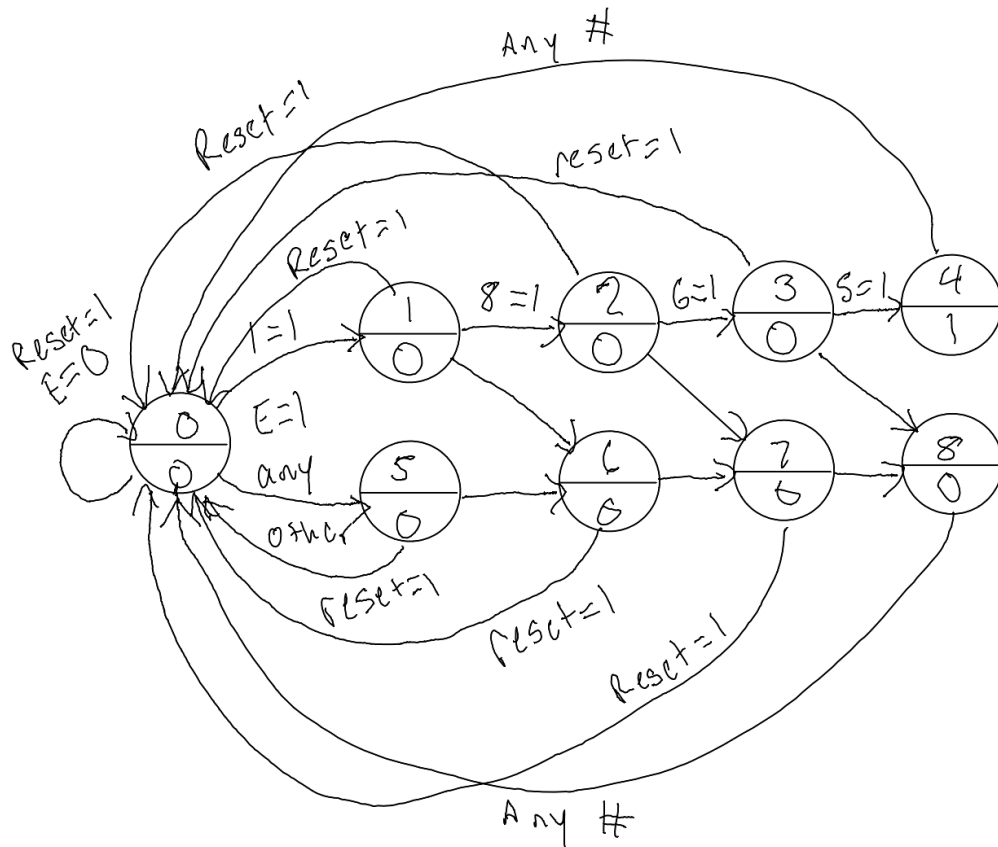


Figure 3.1: FSM Diagram

4 Test Case Development

In our initial testbench, we are looking to confirm the intended behavior of our system. The first behavior we test is the enable switch. The system should not increment the state if a number is inputted and it is not enabled. Next, the exact combination is sent in order to check that the system moves to the next state when expected. If the system gets to the final number, returns a value of one and goes back to its original state, then the sequence for the correct password has worked as intended. Then, we check to make sure at each state, if a wrong number is inputted, it moves to the higher states and does not allow the correct output. Finally, at each of the nine states, we must make sure reset sends the system back to state '0'.

5 Results


```
Contains Synopsys proprietary information.
Compiler version W-2024.09-SP1_Full64; Runtime version W-2024.09-SP1_Full64; Feb 19 23:47 2025

time | enable | number | correct
0     | x       | x       | x
40    | 1       | 1       | 0
80    | 1       | 8       | 0
120   | 1       | 6       | 0
160   | 1       | 5       | 0
200   | 1       | 1       | 1
240   | 1       | 8       | 0
280   | 1       | 6       | 0
320   | 1       | 4       | 0
360   | 1       | 1       | 0
400   | 1       | 8       | 0
440   | 1       | 7       | 0
480   | 1       | 5       | 0
520   | 1       | 1       | 0
560   | 1       | 9       | 0
600   | 1       | 6       | 0
640   | 1       | 5       | 0
680   | 1       | 3       | 0
720   | 1       | 8       | 0
760   | 1       | 6       | 0
800   | 1       | 4       | 0
840   | 0       | 1       | 0
880   | 0       | 8       | 0
920   | 0       | 6       | 0
960   | 0       | 5       | 0
1000  | 0       | 1       | 0

$finish called from file "keypad_tb.sv", line 70.
$finish at simulation time 1040
V C S   S i m u l a t i o n   R e p o r t
Time: 1040
```

Figure 5.1: Testbench output log

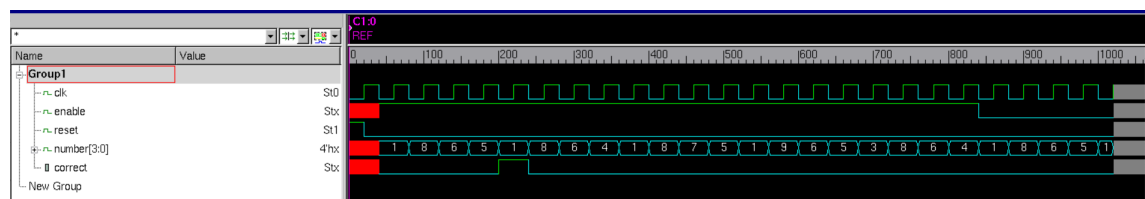


Figure 5.2: DUT waveform

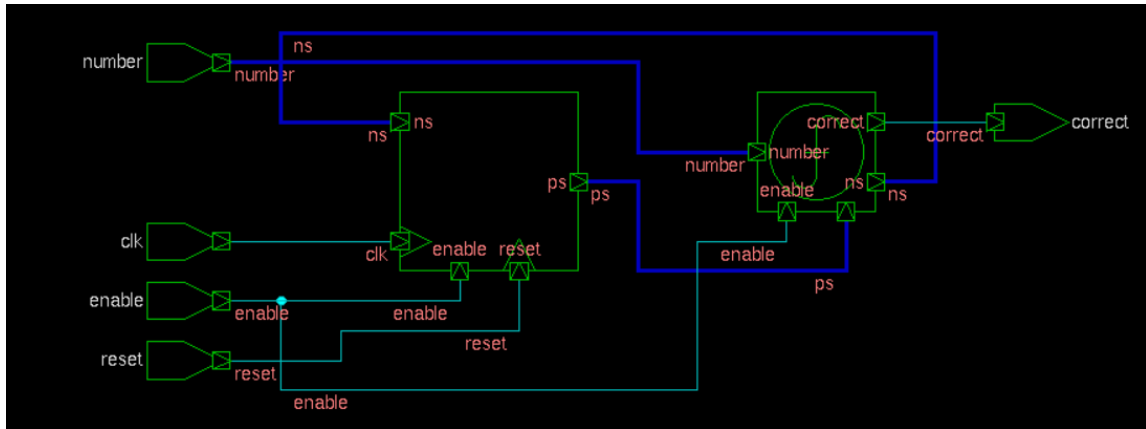


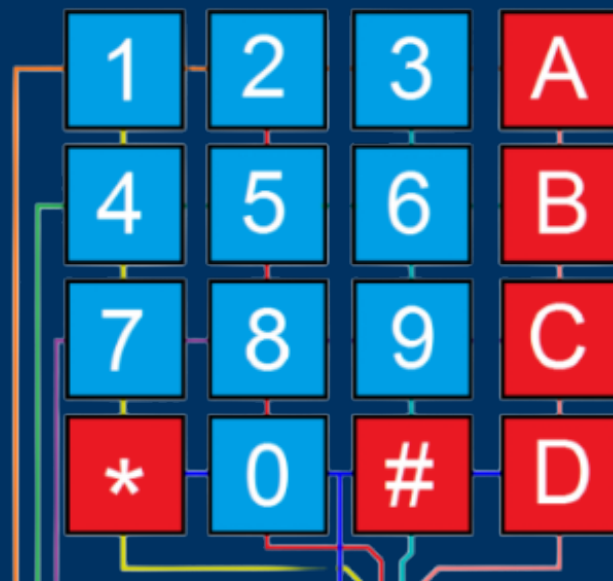
Figure 5.3: DUT synthesis

6 Discussion

Looking at the output of the testbench and the waveform, we can see that the correct output is set to '1' immediately after the correct sequence is entered. We can also verify that at each stage, if the next number is incorrect, this will result in the user being able to input the rest of the numbers in the four digit pass code but will result in an output of '0'. The final four clock cycles show that when enable is set to off, even if the numbers are inputted in the correct order, the correct output will not be '1'. In the future we will have to consider every possible test combination and exhaust each possible state transition. This will ensure our system works as intended and serves as regression testing if we must make adjustments to our code in the future.

7 Conclusion

Developing a digital keypad to secure a chemical plant required planning and thorough development of test cases to ensure our system was working as intended. Creating the FSM diagram allowed us to map out every possible state transition and effectively account for each in our System Verilog program. To develop the testbench we carefully outlined all possible transitions in each state and coded each accordingly into our testbench. Through module development and analysis our testbench outputs, we were successfully able to implement a digital keypad with a reset, enable, and number input while allowing for the output only to be correct on correct pass code input. The owner of the chemical plant is very satisfied with this new security measure and looks to implement more as they expand their security in their facility.



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