UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Digital System I, 894, Fall 1403
Computer Assignment 1
Basic Switch and Gate Structures in Verilog
Week 3-4

Name:
Date:

1. Show switch level structure of a 2-input NAND gate and a NOT gate using nMOS and pMOS structures that have #(3,5,7) and #(4,7,9) delay values respectively.

a. Show the schematic diagram of the circuits.
b. Manually, hand simulate the circuits and, in a timing-diagram, show the two delay values To1 and To0 for each gate.
c. Write switch-level description of the NAND and NOT gates in SystemVerilog.
d. Write a testbench for the above circuits and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady state before the next input change.
e. To the above testbench add a NAND primitive that uses the worst-case delay values of the transistor-level circuit. Let these two circuits simulate in parallel and observe the differences in simulation.
f. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

2. Show switch level structure of a 3-input Majority gate as a complex gate. The output becomes 1 when the majority of the inputs are 1. Use nMOS and pMOS structures that have #(3,5,7) and #(4,7,9) delay values respectively.

a. Show the schematic diagram of the circuits.
b. Manually, hand simulate the circuits and, in a timing-diagram, show the three delay values To1, To0, and ToZ for each gate.
c. Write switch-level descriptions of the Majority gate in SystemVerilog. We refer to this circuit as Maj1.
d. Write a testbench for the above circuits and using test data from the testbench apply inputs to cause the circuits' worst-case delays. Make sure the changes on inputs are far enough apart to put the circuits into a steady state before the next input change.
e. Compare your hand-simulation and the SystemVerilog simulation and explain the differences, if any.

f. Instead of switches, build the Majority gate using NAND and NOT gates of Part 1. Use a NOT gate at the output of your circuit to generate the true output. We refer to this circuit as Maj2.
g. Using an **assign** statement write another circuit description for the majority gate. We refer to this circuit as Maj3.
h. In a testbench instantiate Maj1, Maj2, and Maj3 circuits run test data and see the differences. Make sure you exercise input transitions that cause the circuit's worst-case delays.

3. Using an **assign** statement write a module description for a three-input XOR structure. Estime the delay values based on your findings from Part 2. Refer to this structure as Odd3.

4. In this part you will put the two subcircuits you developed above into a complete circuit.
a. Write a SystemVerilog module with three inputs and two outputs. In the module instantiate a Maj gate and the Odd3 circuit of the above part. The three inputs drive both subcircuits. One of the outputs of the module comes from the Maj structure and another one from the Odd3 circuit.
b. Write a testbench and analyze the functionality and timing of this circuit.
c. What is this circuit?

Deliverables:

Generate a report that includes all the items below:

A. For Parts 1 and 2, do Parts a and b on paper. Calculate hand simulations and include your arithmetic in the report. On paper, show your timing extractions from the waveforms. Show waveforms as proof of simulation. Your simulation run and the project built for this purpose must be demonstrated to the TA.
B. For Parts 3,4 show waveforms. Your simulation run and the project built for this purpose must be demonstrated to the TA.
C. For all parts, project file and Waveforms must be demonstrated to the TA. Using waveforms, circuit diagrams, and other circuit representations justify your answers for transistor count, timing, and power usage of each structure.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.