UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Digital System I, 894, Fall 1403
Computer Assignment 2
Combinational RTL Design & Simulation

Name:	**Date:**
Username:	

A full adder is a digital circuit that performs binary addition on its three inputs: two input bits (usually denoted as **A** and **B**) and a carry-in bit (denoted as $\mathbf{C_{in}}$). It produces two outputs: the sum (**S**) and the carry-out ($\mathbf{C_{out}}$). The circuit you did in your Computer Assignment 1, can be regarded as a Full-Adder.

A one's counter takes a binary number and counts how many bits are '1'. It produces a 2-bit data output that ranges from 00 number of 1's to 11 number of 1's. For instance, in a 3-bit input binary number **ABC**, the number of ones can be:

- 0 (for 000)
- 1 (for inputs like 001, 010, or 100)
- 2 (for inputs like 011, 101, or 110)
- 3 (for input 111)

The circuit you did in your Computer Assignment 1, can be regarded as a 3-input 1's counter.

The idea here is that by adding bits **A**, **B**, and **C** using a full adder, we can obtain a binary result representing the count of '1's on these inputs. For example, if **A**=1, **B**=1, and **C**=0, the sum of these '1's will be 10 (binary for 2), showing two '1's in the input. So, a full adder is a 3-bit one's counter.

Part 1

1. **Gate Level Design**:
   Provide the gate-level design for each of the following adders:
   - **1-bit Adder**: Use the circuit you obtained in the last part of Computer Assignment 1 to build a 1-bit adder (i.e., a full adder). Use worst-case delay values based on the transistor structures of the two outputs of the circuit.
   - **2-bit Adder:** cascade two 1-bit adders in order to make a 2-bit adder.
   - **3-bit Adder**: Extend your design to accommodate three bits by cascading a 2-bit and a 1-bit adders.
   - **4-bit Adder**: Further extend your design to support four bits using two 2-bit adders.
   - **5-bit Adder**: Further extend your design to support five bits using a 2-bit and a 3-bit adder.

2. **System Verilog Modules**:
   Write separate System Verilog modules for each of the adders designed in Step 1. Ensure each module adheres to the following criteria:
   - Include the necessary inputs and outputs.
   - Implement the functionality using ODD3 and MAJ descriptions as defined in your designs.
   - Utilize the gate delays provided in Computer Assignment 1 to simulate the your adders.

3. **Simulation and Waveforms**:
- Simulate your modules using ModelSim.
- Capture the output waveforms for each adder.
- Analyze the waveforms to demonstrate the correct functioning of each adder.

Part 2

Make a 63-input one's counter using the 2-bit, 3-bit, 4-bit, and 5-bit adder modules you developed in Part 1. You must instantiate your previous modules properly and make a new module named "OnesCounter63". Illustrate your circuit design and write appropriate System Verilog codes based on that. Simulate your design and show the output waveform results.

Part 3
- Calculate the worst-case delay of 2-bit, 3-bit, 4-bit, and 5-bit adder.
- Calculate the worst-case delay of the 63-input one's counter.

Deliverables:

Generate a report that includes all the items below:

a. For Parts 1,3 show your design on paper. Include your arithmetic in the report. Show waveforms as proof of simulation. Your simulation run and the project built for this purpose must be demonstrated to the TA.
b. For Part 2 show waveforms. Your simulation run and the project built for this purpose must be demonstrated to the TA.
c. For all parts, project file and Waveforms must be demonstrated to the TA. Using waveforms, circuit diagrams, and other circuit representations justify your answers for transistor count, timing, and power usage of each structure.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.