Experiment #1 - Clock and Periodic Signal Generation

Erfan Iravani,
810197462

***Abstract*— This is the report of first Logic Design Lab experiment. In the following report some examinations and calculation and photo report are included.**

***Keywords*— ring oscillator , LM555 timer , Schmitt trigger oscillator , frequency divider , T Flip Flop**

INTRODUCTION

The goal of this experiment is to introduce the concepts of static characteristics of digital logic
gates, delay times, clock frequency generation and digital system using schematic diagram and *Verilog* HDL

I. CLOCK GENERATION USING ICS AND ANALOG COMPONENTS

We use LTspice for simulating the circuits of this section.

1.1 Ring Oscillator

We want to measure the propagation delay of the chain by measuring the period time of the output.
In this section we use ring oscillator to measure that.
The time at which a value feeds back to the same node is the time period of the ring oscillator which equals $2N * Delay_{invertor}$, where N is the odd number and $Delay_{invertor}$ is the delay of each inverter gate.

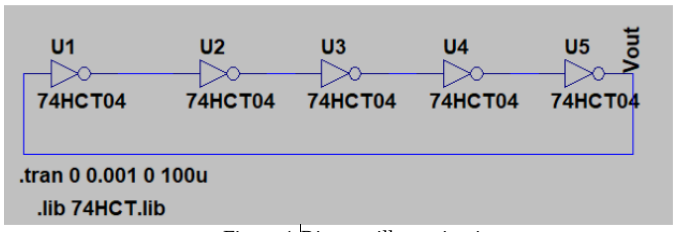

Figure 1: Ring oscillator circuit

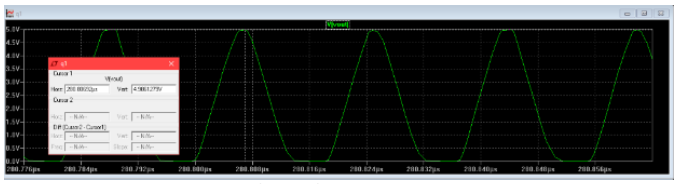

Figure 2: wave form of Ring oscillator circuit

From the wave form and up information :
The propagation delay of this circuit is 0.018 µs.
The dalay of single eache invertor is 0.18 µs / 10 = 0.0018 µs

1.2 LM555 timer

T1 = 0.693 * (R1 + R2) * C
T2 = 0.693 * R2 * C
T = T1 + T2
F = 1 / T
Duty cycle = (R1 + R2) / (R1 + 2R2)

We Change the value of *R2* resistors from 50 kΩ to 1 kΩ , 10 kΩ and 100 kΩ and we redo the calculations.

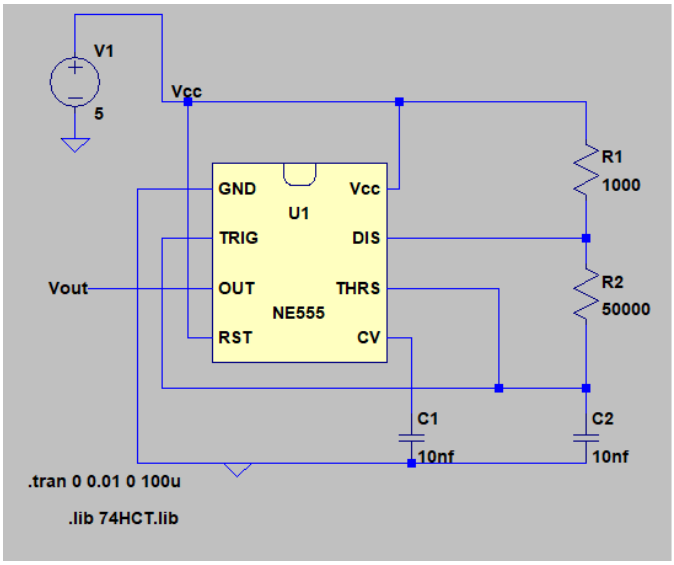

Figure 3: LM555 timer circuit , R2 = 50kΩ

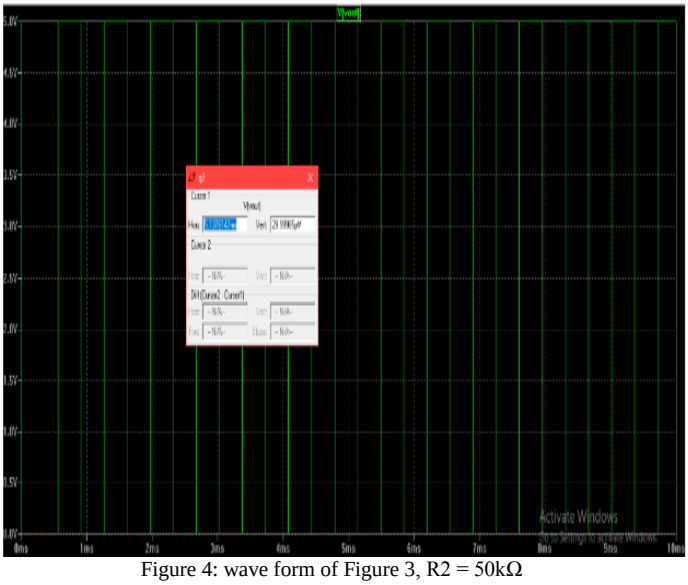

Figure 4: wave form of Figure 3, R2 = 50kΩ

R1 = 1kΩ , R2 = 50kΩ, C = 10nF
T = 699.93 µF ,
F = 1 / T = 1428.7143
Duty cycle = 0.5049
From wave ,: the cycle period is 0.70363 ms and the duty cycle is 359/703=0.51 and f = 1421 Hz.

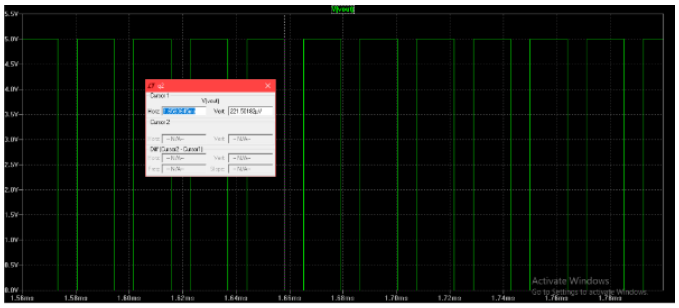

Figure 5: wave form of Figure 3, R2 = 1kΩ

R1 = 1kΩ , R2 = 1kΩ, C = 10nF
T = 20.79 µF ,
F = 1 / T = 48100.048
Duty cycle = 0.666
From wave form : the cycle period is 0.021013 ms and the duty cycle is 0.6578 and f = 47587.7751Hz.

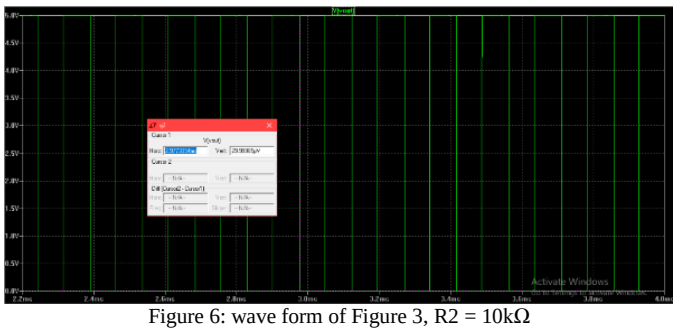

Figure 6: wave form of Figure 3, R2 = 10kΩ

R1 = 1kΩ , R2 = 10kΩ, C = 10nF
T = 145.53 µF ,
F = 1 / T = 6871.45
Duty cycle = 0.5238
From wave form : the cycle period is 0.14609 ms and the duty cycle is 0.5283 and f = 6844.865Hz.

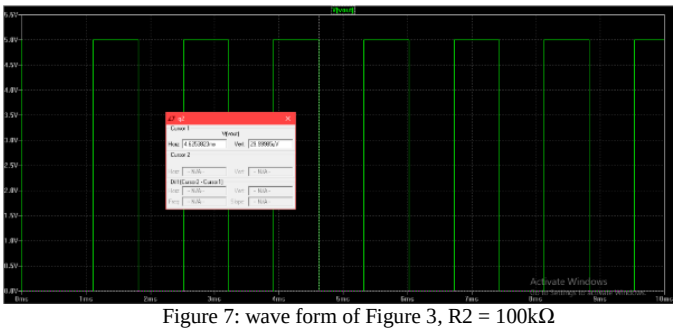

Figure 7: wave form of Figure 3, R2 = 100kΩ

R1 = 1kΩ , R2 = 100kΩ, C = 10nF
T = 1392.93 µF ,
F = 1 / T = 719.911
Duty cycle = 0.502

From wave form : the cycle period is 1.39143 ms and the duty cycle is 0.5054 and f = 718.68Hz.

1.3 Schmitt Trigger Osillator

We use 470 Ω, 1 kΩ and 2.2 kΩ for the resistor and 10 nF for the capacitor.

When R is 470Ω and f is 278465.43 Hz then α is 1.308.
When R is 2.2kΩ and f is 66361.76 Hz then α is 1.45.
Alpha would change a little by changing R but that is not significant and we can assume alpha = 1.4

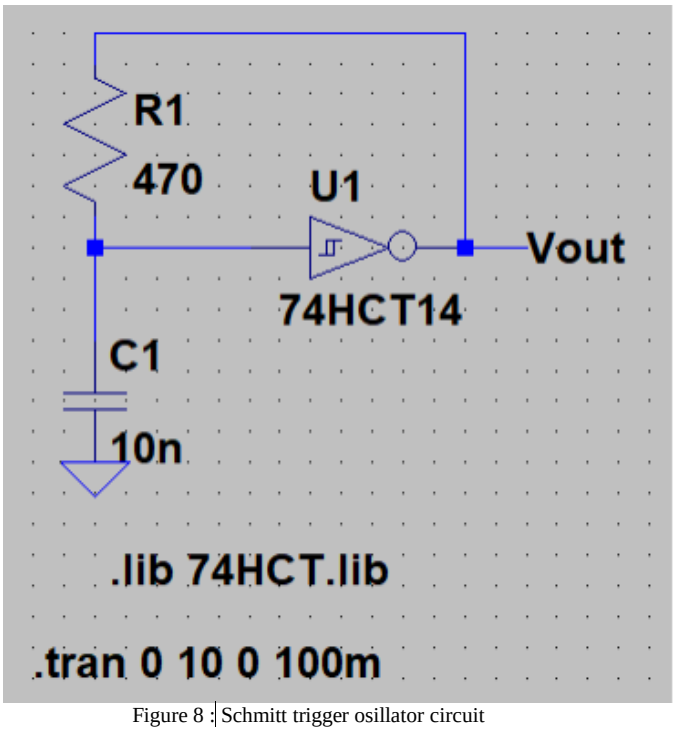

Figure 8 : Schmitt trigger osillator circuit

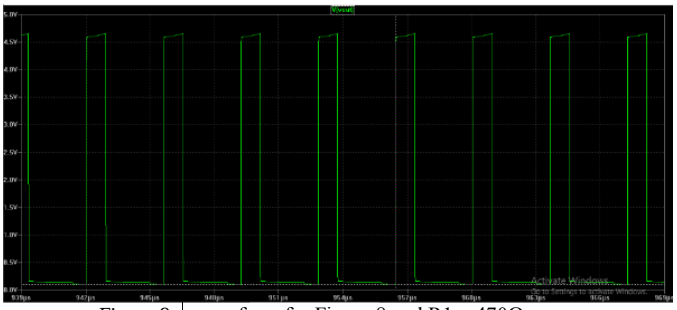

Figure 9 : wave form for Figure 8 and R1 = 470Ω

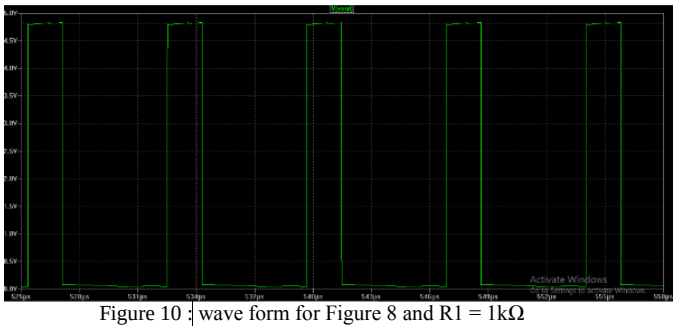

Figure 10 : wave form for Figure 8 and R1 = 1kΩ

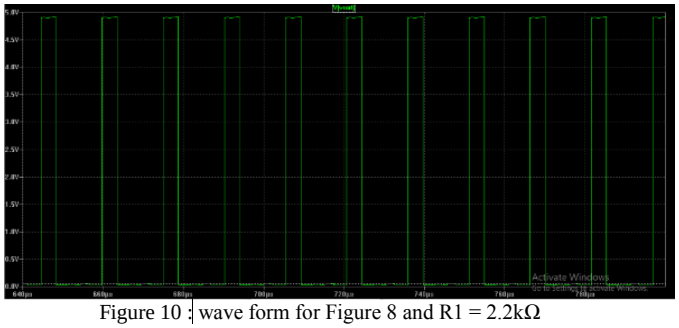

Figure 10 : wave form for Figure 8 and R1 = 2.2kΩ

As we can see by increasing R , frequency will decrease but duty cycle will not change

II. Clock Generation using Verilog HDL

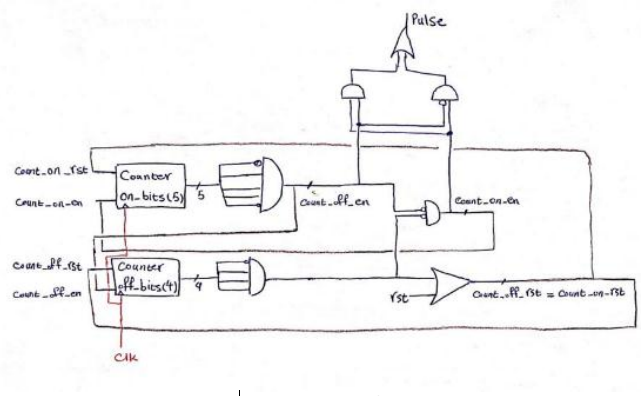

Figure 11 : black digram of LM555

Onduration and Offduration will determine the time periods when the clock is ON and when is OFF
$clog2 function returns the ceiling of logarithm to base 2.
So on_bits=4 and off_bits=3
Then we have 2 counter blocks.
First one will count from 0 to Onduration and after that the Second one will start counting from 0 to Offduration

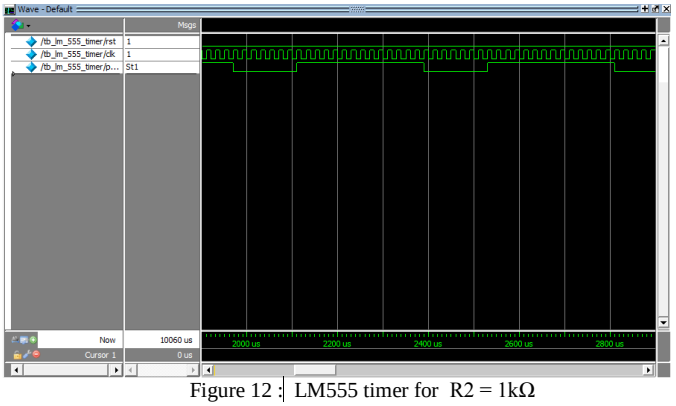

Figure 12 : LM555 timer for R2 = 1kΩ

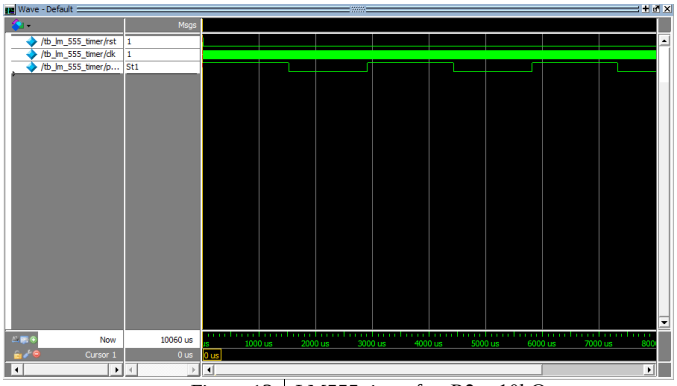

Figure 13 : LM555 timer for R2 = 10kΩ

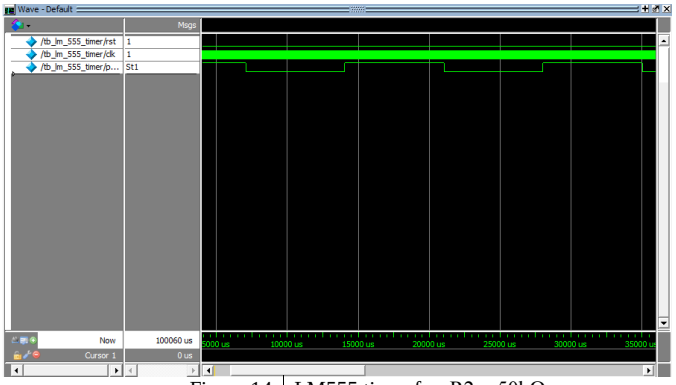

Figure 14 : LM555 timer for R2 = 50kΩ

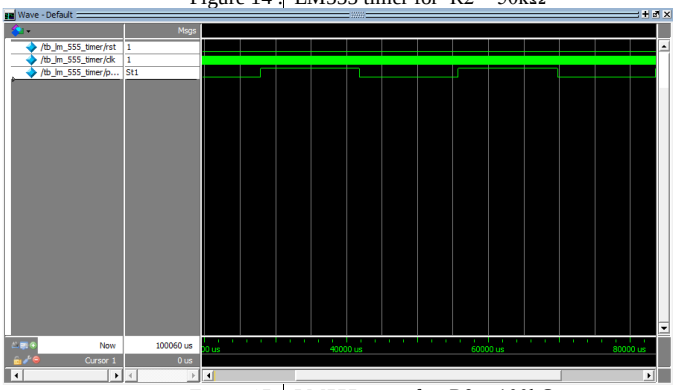

Figure 15 : LM555 timer for R2 = 100kΩ

The duty cycles are very close to what we had in section 1-2 but the frequencies are different and this may be because of the clk timing in our Verilog testbench

Alternative method :
With an always statement and Onduration and Offduration we can change pulse to ~pulse with the proper delay values

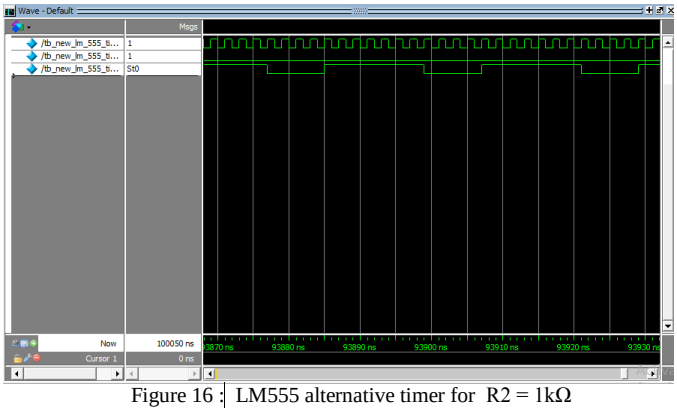

Figure 16 : LM555 alternative timer for R2 = 1kΩ

Duty cycle is 2/3

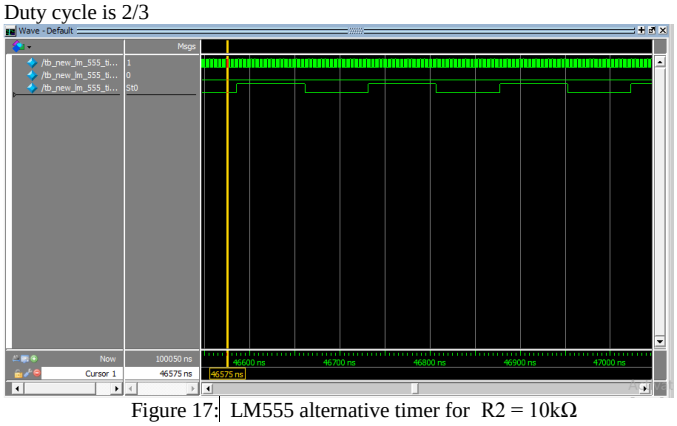

Figure 17: LM555 alternative timer for R2 = 10kΩ

Duty cycle is close to 0.53

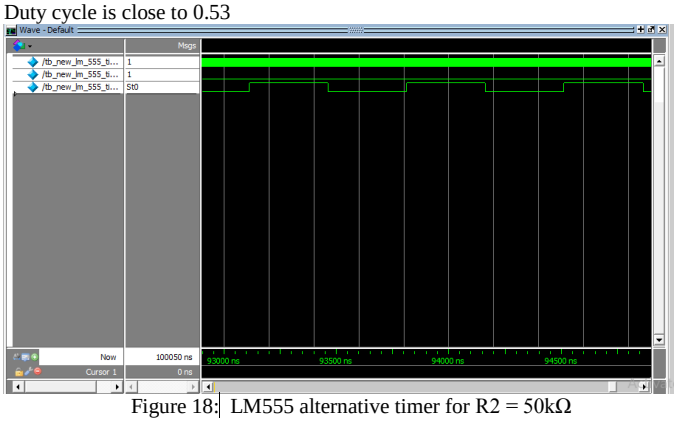

Figure 18: LM555 alternative timer for R2 = 50kΩ

Duty cycle is 0.52

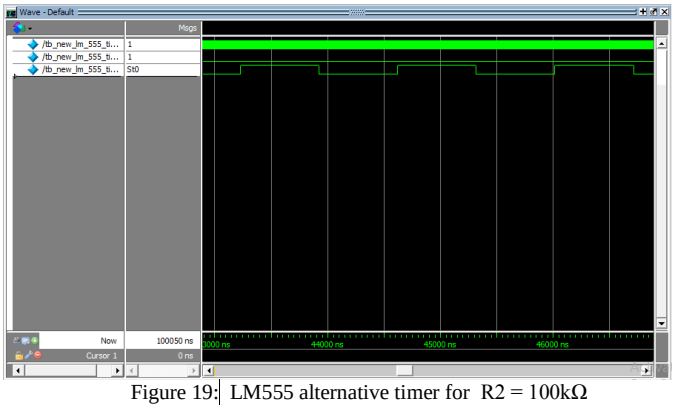

Figure 19: LM555 alternative timer for R2 = 100kΩ

Duty cycle is 0.51

As we see duty cycles are the same as before

III. FPGA DESIGN

3.1

From wave form : the cycle period is 20 ns and the and f = 50000KHz.

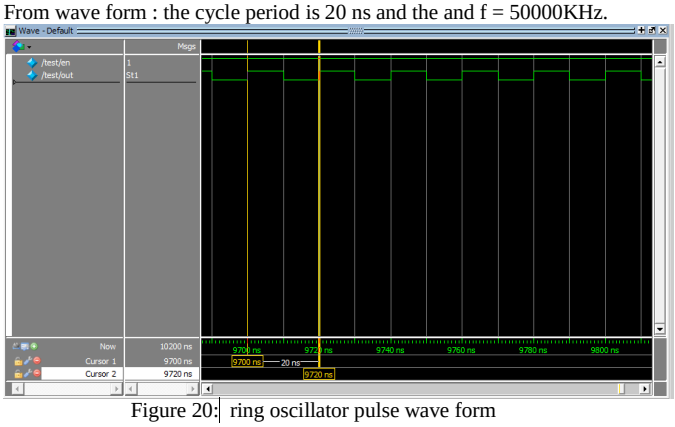

Figure 20: ring oscillator pulse wave form

3.2

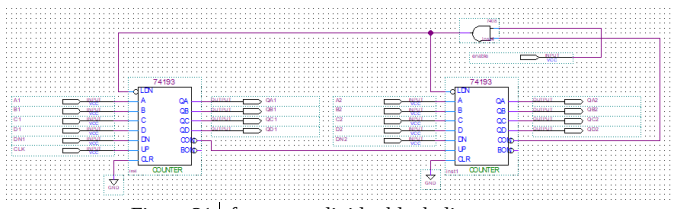

Figure 21: frequency divider block digram

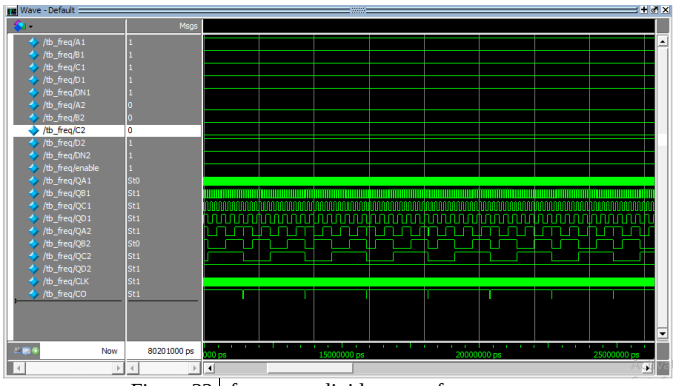

Figure 22: frequency divider wave form

The frequency of ‘co’ is 446.428 KHz

3.3

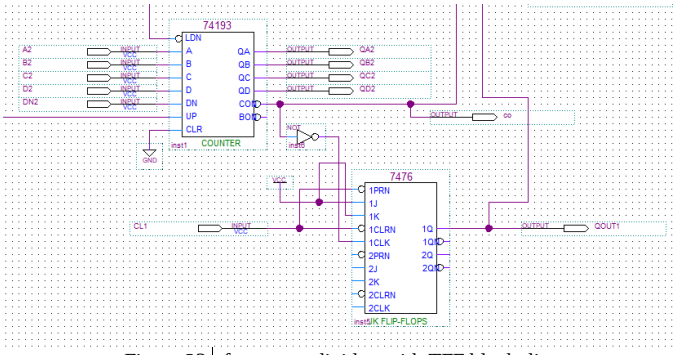

Figure 23: frequency divider with TFF block digram

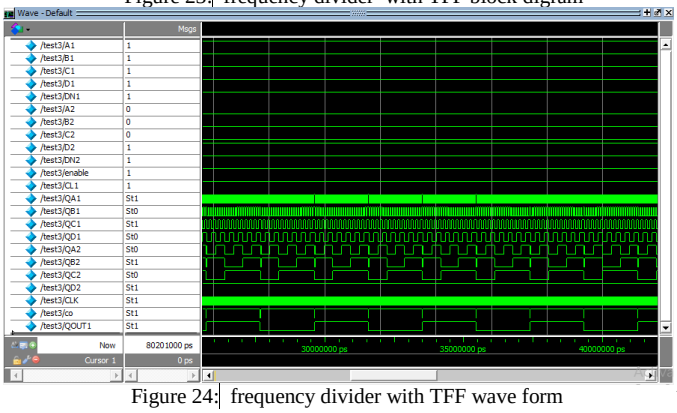

Figure 24: frequency divider with TFF wave form

3.4

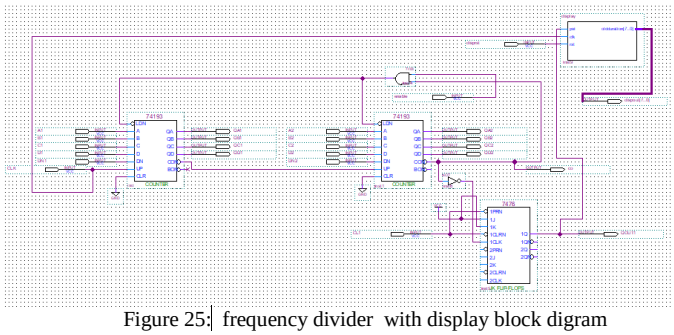

Figure 25: frequency divider with display block digram

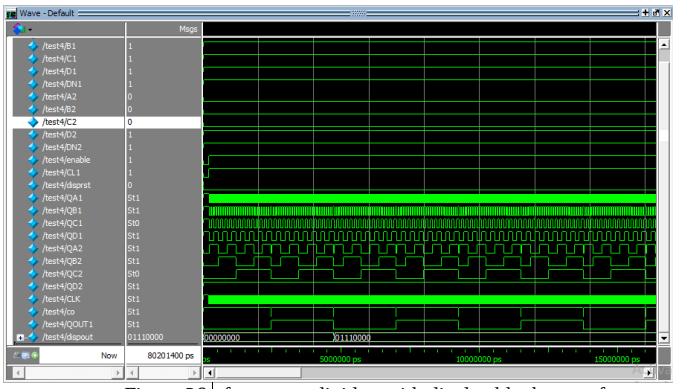

Figure 26: frequency divider with display block wave form

If we briefly look at the display component code , we see that ‘psi’ works as the count enable .

so by connecting ‘psi’ to the output of flip flop we have actually made a frequency divider and display output gives us the quotient
and the frequency of this quotient as we calculated in part 3.2 is 446.428KHz
so the frequency of the main clock (ring oscillator) is 446.428*112=49999.93KHz and that is so close to what we Calculated in part 3.1

CONCLUSIONS

We started by generating a clock signal in 3 different ways both as analog and digital circuits.
We made a frequency divider by connecting 2 counters and by using a flip flop we produced a 50 percent duty cycle signal ; and finally we learned how to measure a high-frequency clock signal with analog oscilloscope using the frequency divider

REFERENCES

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[2]https://www.alldatasheet.com/datasheet-pdf/pdf/15524/PHILIPS/74HCT04.html

[3] Digital Logic Laboratory, University of Tehran, Spring 1399Prepared and developed byKatayoon Basharkhahunder supervision of Professor Z. Navabi