Synchronous Digital Systems - SDS

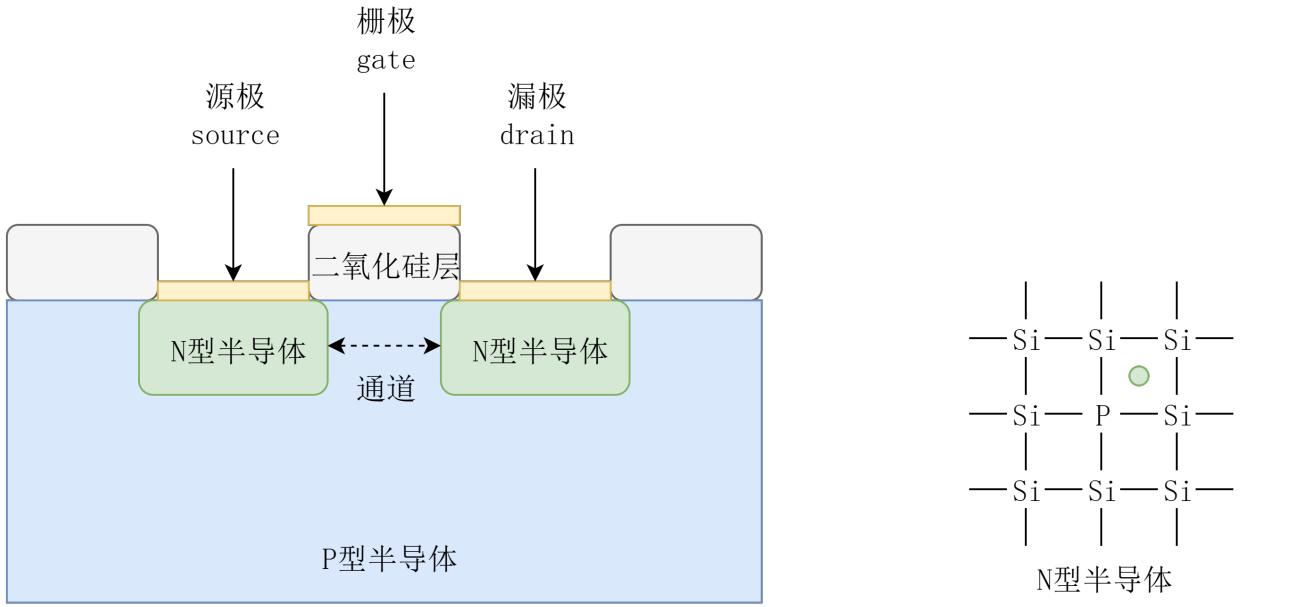
LiHan

2023/03/17

Synchronous Digital Systems

- Synchronous: All operations coordinated by a central clock
- Digital: All operations are limited by 0 and 1
- SDS: Combinational Logic and Sequential Logic

Switch - MOSFET



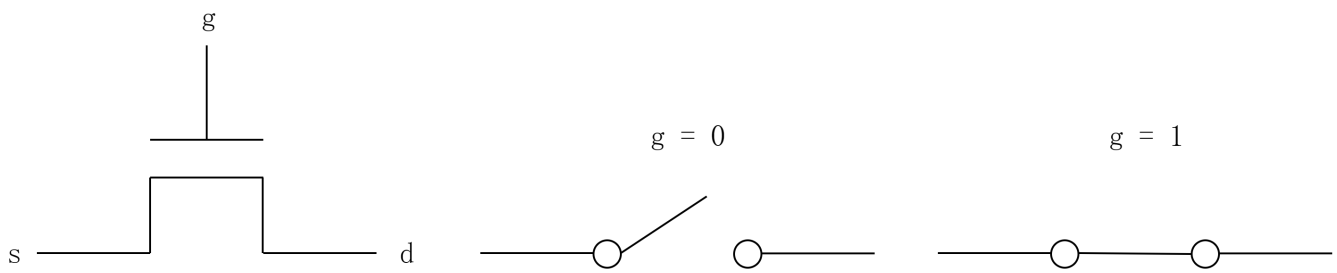


Figure: NMOS

Switch - MOSFET

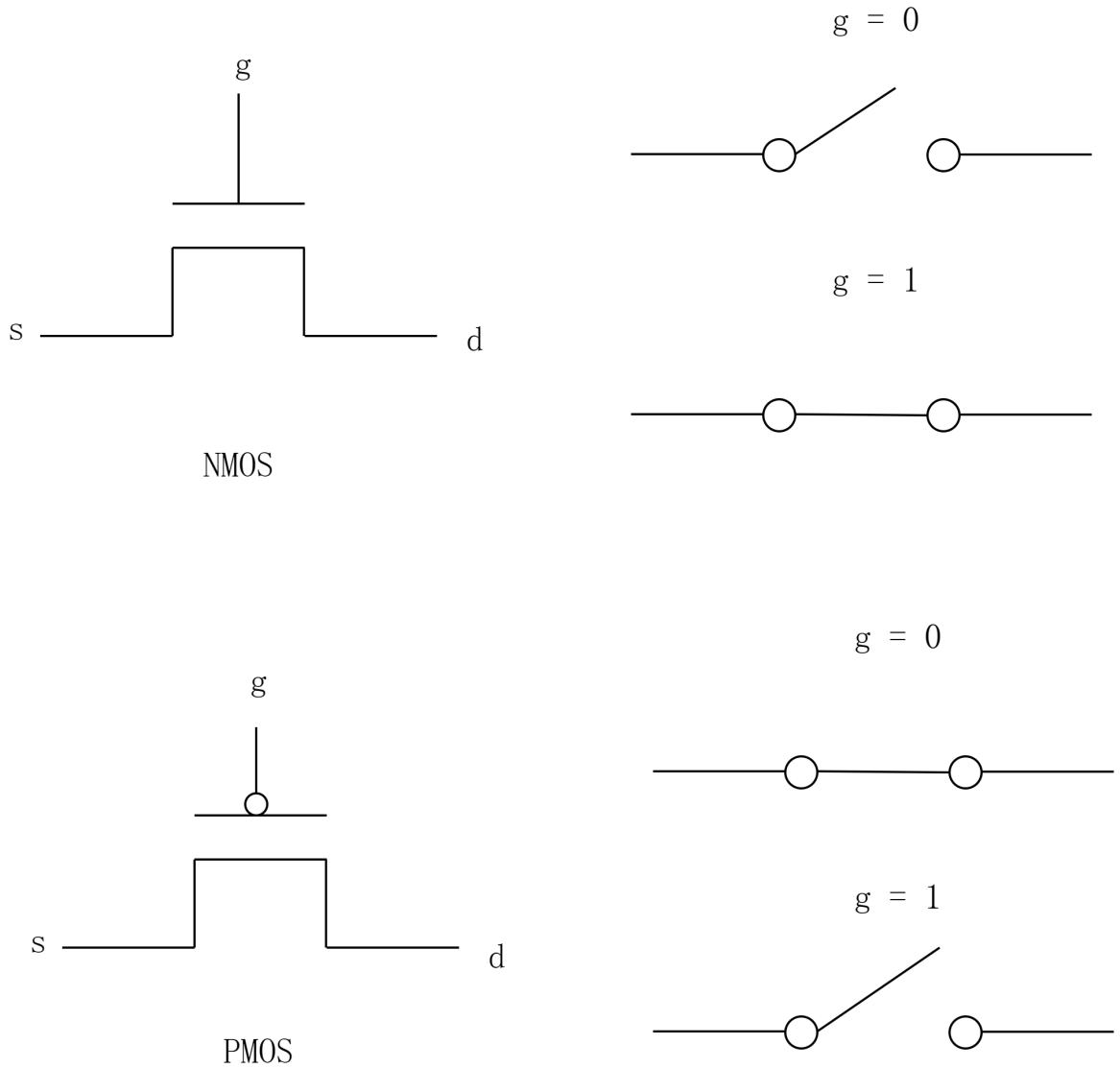
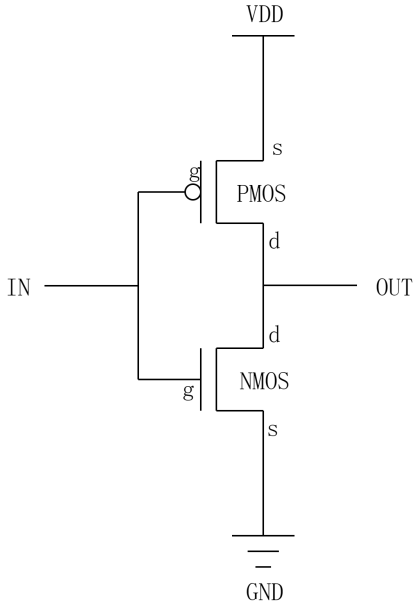
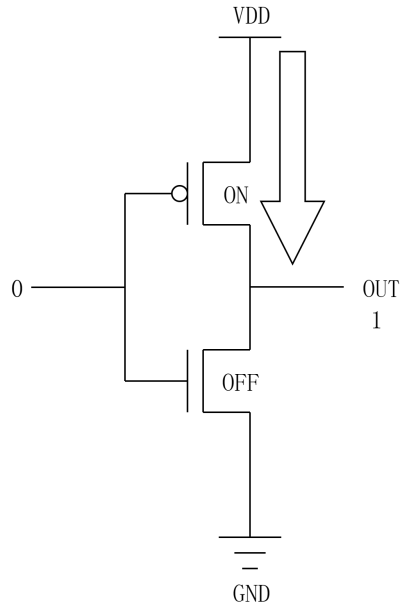
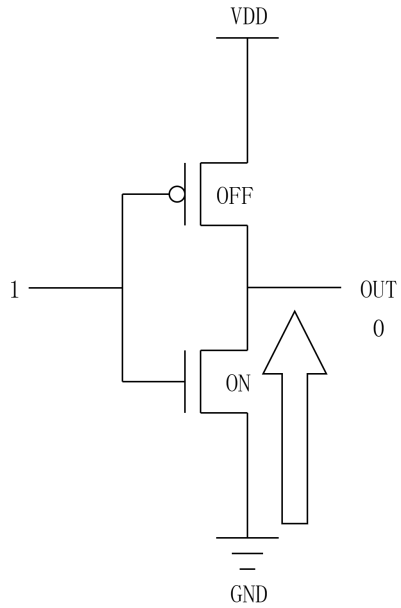


Figure: NMOS AND PMOS

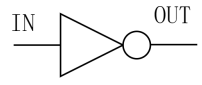
CMOS TO LOGIC







IN	OUT
0	1
1	0



Basic Logic Gates

- NOT
- AND
- OR

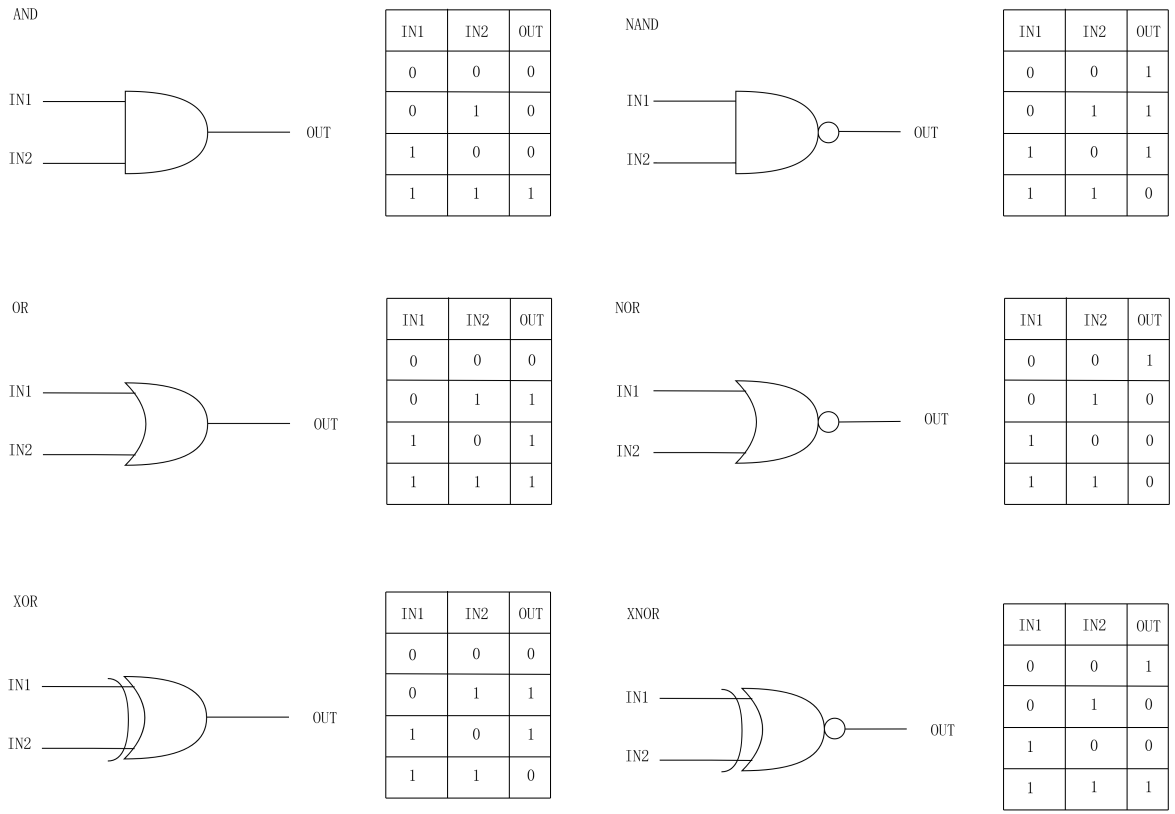


Figure: LOGIC GATES AND TRUTH TABLE

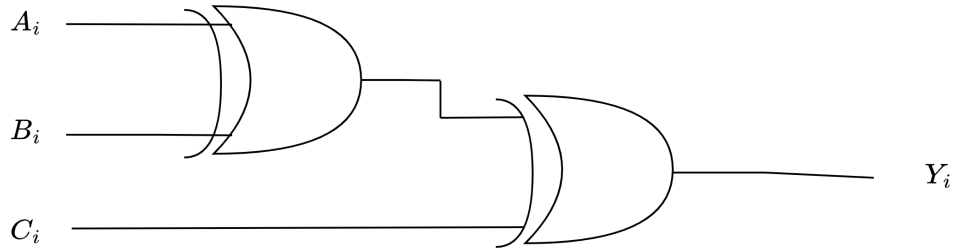
COMBINATIONAL LOGIC

$$Y = A_3A_2A_1A_0 + B_3B_2B_1B_0$$

$$\begin{array}{rr} & C_2C_1 \\ & A_3A_2A_1A_0 \\ + & B_3B_2B_1B_0 \\ \hline & Y_1 \end{array}$$

A_i	B_i	C_i	C_{i+1}	Y_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$Y_i = A_i \oplus B_i \oplus C_i$$



$$C_{i+1} = A_iB_i + A_iC_i + B_iC_i$$

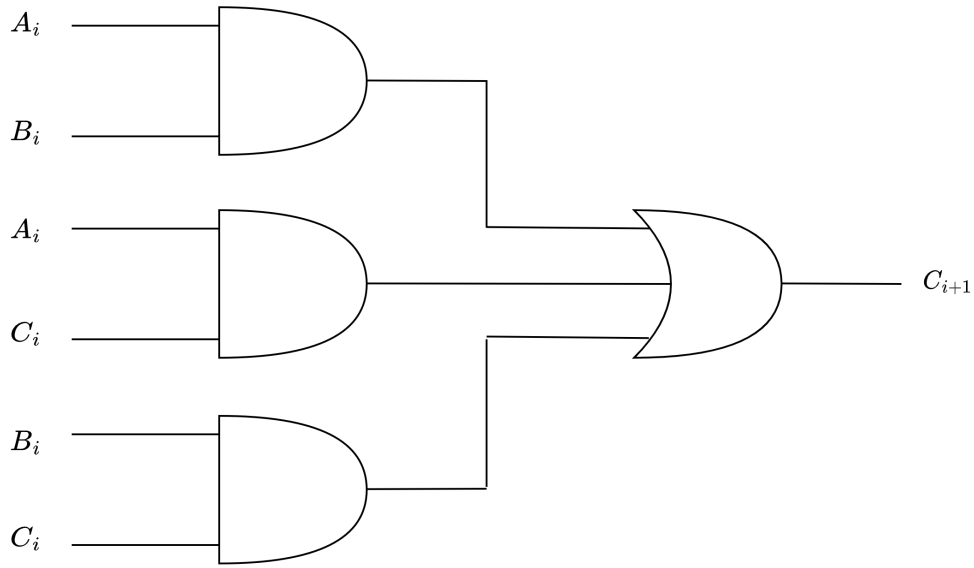
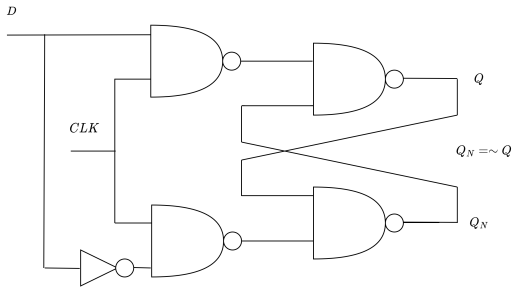
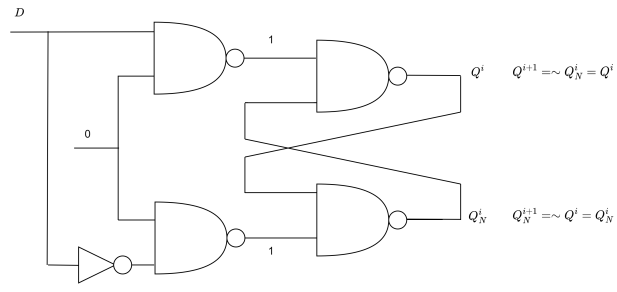


Figure: COMPLEX LOGIC

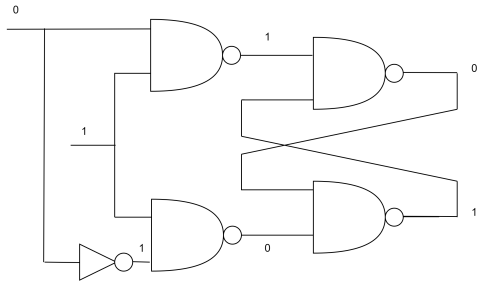
SEQUENTIAL LOGIC

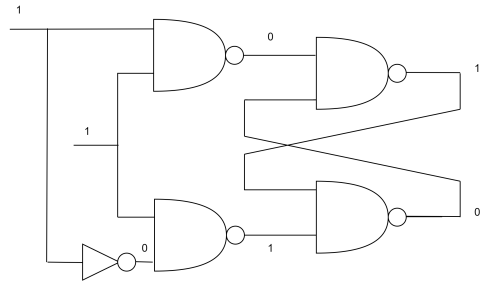
IN1	IN2	OUT
0	0	1
0	1	1
1	0	1
1	1	0





$CLK = 0 \quad Q = Q$





$CLK = 1 \; Q = D$

SDS

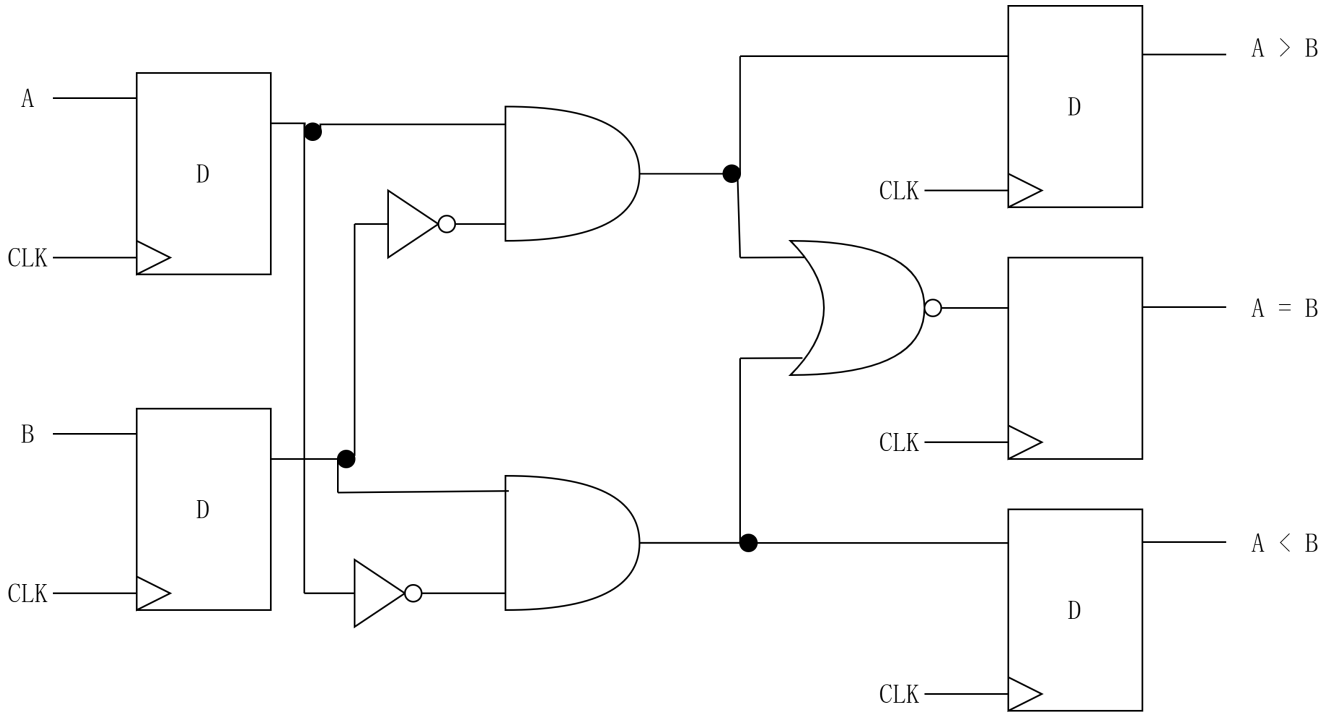


Figure: SDS