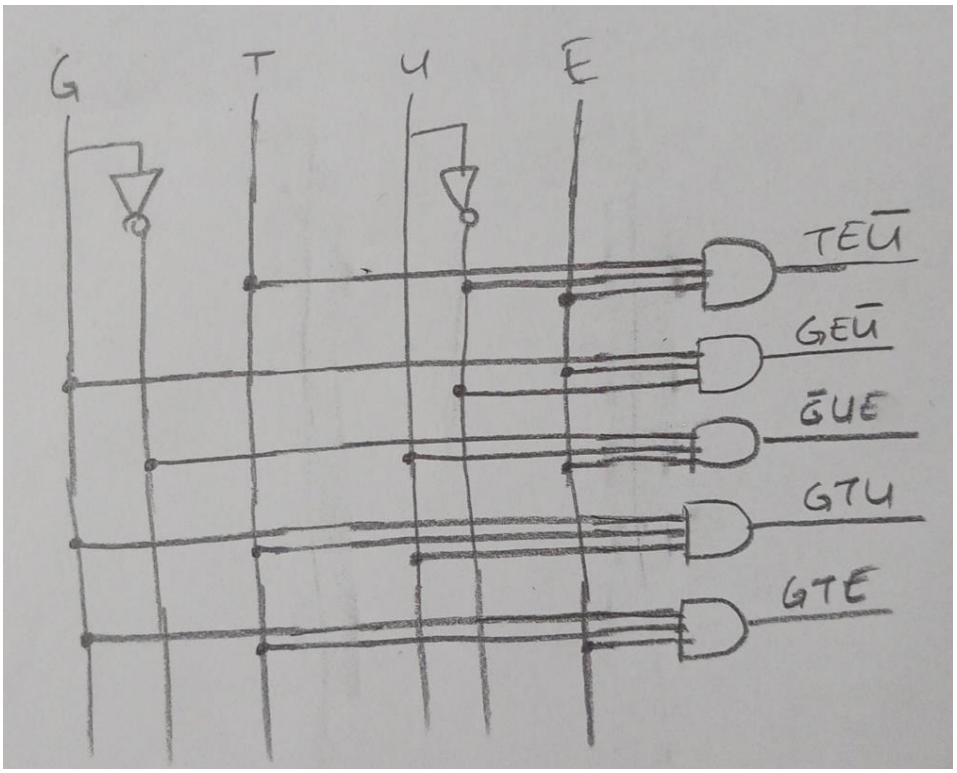
## Problem 1:

**Truth table:**

| G | T | U | E | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Devre Şeması:**



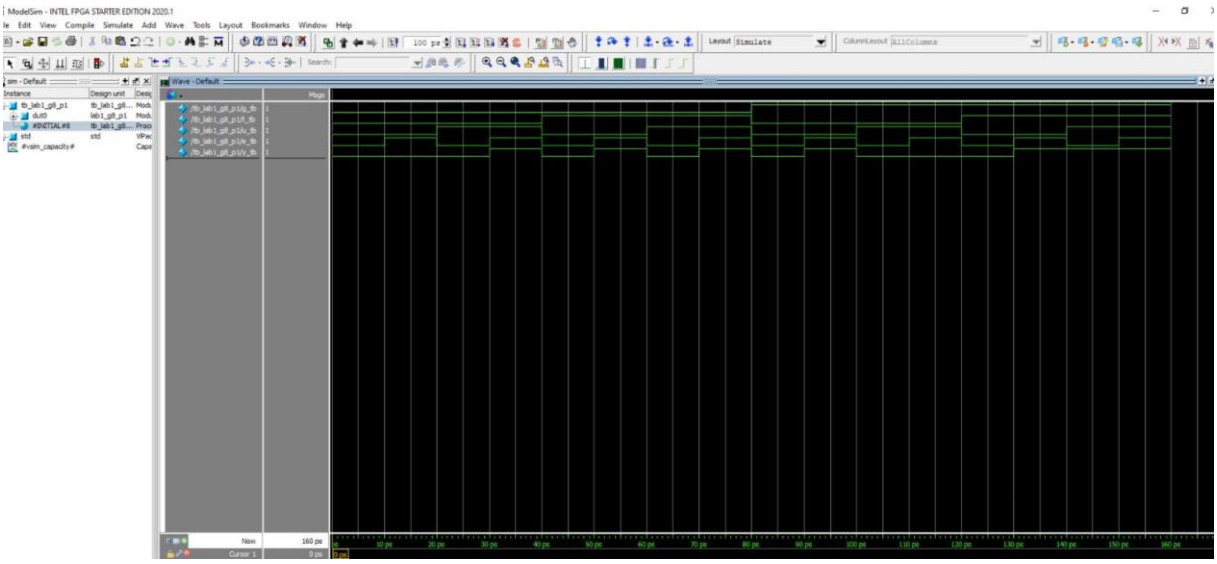
**Kodlar:**

C:/Users/Esra/Documents/quartusmodelsim/lab1_g8_p1.sv (/tb_lab1_g8_p1/dut0) - Default

```
Ln#
1  // Y = G?TU?E + GTUE + GT?U?E + GTU?E + G?TUE + G?T?UE + GTUE?
2  module lab1_g8_p1(
3      input logic g, t, u, e,
4      output logic y
5  );
6
7  assign y = ~g & t & ~u & e | g & t & u & e | g & ~t & ~u & e | g & t & ~u & e | ~g & t & u & e | ~g & ~t & u & e | g & t & u & ~e;
8
9  endmodule
10
```

```
Ln#
1   module tb_lab1_g8_p1 ();
2       logic g_tb, t_tb, u_tb, e_tb;
3       logic y_tb;
4
5
6   lab1_g8_p1 dut0(g_tb, t_tb, u_tb, e_tb, y_tb);
7
8   initial begin
9
10      g_tb = 0; t_tb = 0; u_tb = 0; e_tb = 0;             #10
11      e_tb = 1;                                           #10
12      u_tb = 1; e_tb = 0;                                 #10
13      e_tb = 1;                                           #10
14      t_tb = 1; u_tb = 0; e_tb = 0;                       #10
15      e_tb = 1;                                           #10
16      u_tb = 1; e_tb = 0;                                 #10
17      e_tb = 1;                                           #10
18      g_tb = 1; t_tb = 0; u_tb = 0; e_tb = 0;             #10
19      e_tb = 1;                                           #10
20      u_tb = 1; e_tb = 0;                                 #10
21      e_tb = 1;                                           #10
22      t_tb = 1; u_tb = 0; e_tb = 0;                       #10
23      e_tb = 1;                                           #10
24      u_tb = 1; e_tb = 0;                                 #10
25      g_tb = 1; t_tb = 1; u_tb = 1; e_tb = 1;             #10
26
27      $stop;
28  end
29
30
31  endmodule
32
```

**Zaman Diyagramı:**



**Quartus:**

| Flow Summary | |
|---|---|
| <<Filter>> | |
| Flow Status | Successful - Thu Apr 27 23:08:19 2023 |
| Quartus Prime Version | 22.1std.1 Build 917 02/14/2023 SC Lite Edition |
| Revision Name | lab1_g8_p1 |
| Top-level Entity Name | lab1_g8_p1 |
| Family | MAX 10 |
| Device | 10M08DAF484C8G |
| Timing Models | Final |
| Total logic elements | 2 / 8,064 ( < 1 % ) |
| Total registers | 0 |
| Total pins | 5 / 250 ( 2 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 387,072 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 48 ( 0 % ) |
| Total PLLs | 0 / 2 ( 0 % ) |
| UFM blocks | 0 / 1 ( 0 % ) |
| ADC blocks | 0 / 1 ( 0 % ) |

## Analysis & Synthesis Summary

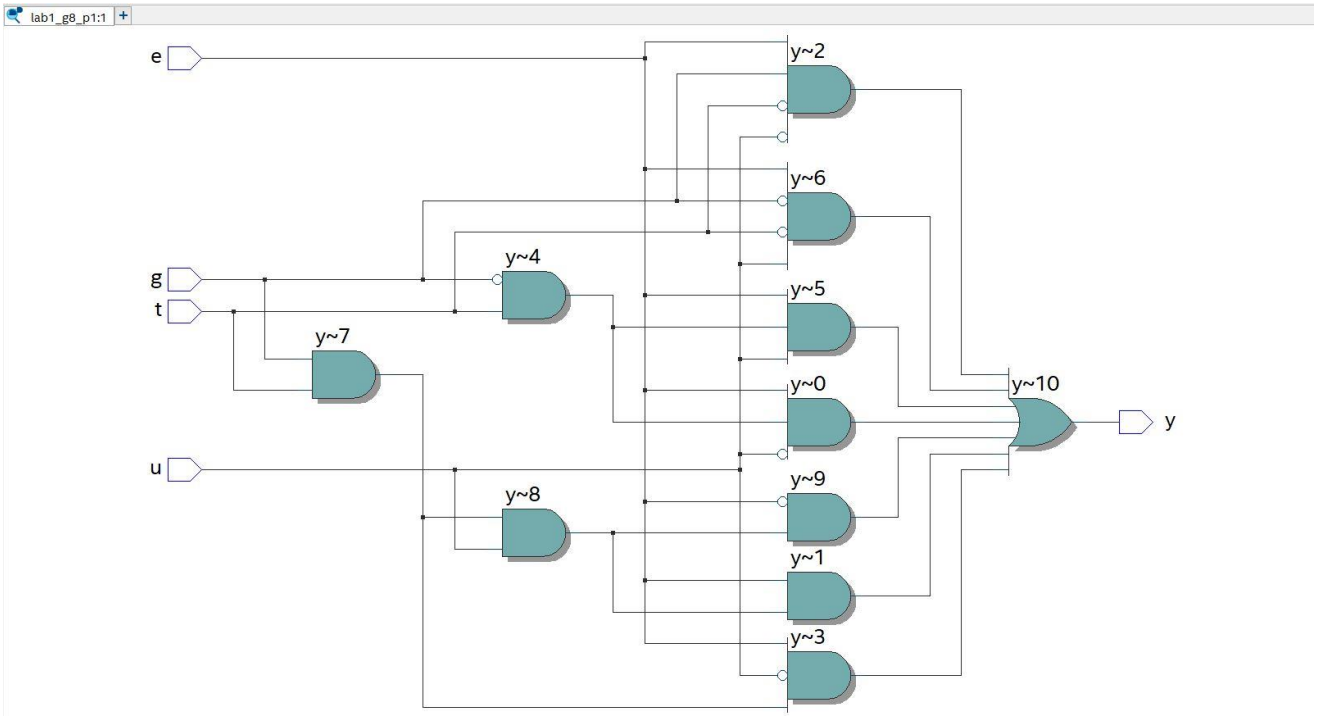
<<Filter>>

| | |
|---|---|
| Analysis & Synthesis Status | Successful - Thu Apr 27 23:08:10 2023 |
| Quartus Prime Version | 22.1std.1 Build 917 02/14/2023 SC Lite Edition |
| Revision Name | lab1_g8_p1 |
| Top-level Entity Name | lab1_g8_p1 |
| Family | MAX 10 |
| Total logic elements | 1 |
| Total registers | 0 |
| Total pins | 5 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |
| UFM blocks | 0 |
| ADC blocks | 0 |

## Analysis & Synthesis Resource Usage Summary

<<Filter>>

| | Resource | Usage |
|---|---|---|
| 1 | Estimated Total logic elements | 1 |
| 2 | | |
| 3 | Total combinational functions | 1 |
| 4 | ▼ Logic element usage by number of LUT inputs | |
| 1 | -- 4 input functions | 1 |
| 2 | -- 3 input functions | 0 |
| 3 | -- <=2 input functions | 0 |
| 5 | | |
| 6 | ▼ Logic elements by mode | |
| 1 | -- normal mode | 1 |
| 2 | -- arithmetic mode | 0 |
| 7 | | |
| 8 | ▼ Total registers | 0 |
| 1 | -- Dedicated logic registers | 0 |
| 2 | -- I/O registers | 0 |
| 9 | | |
| 10 | I/O pins | 5 |
| 11 | | |
| 12 | Embedded Multiplier 9-bit elements | 0 |
| 13 | | |
| 14 | Maximum fan-out node | y~0 |
| 15 | Maximum fan-out | 1 |
| 16 | Total fan-out | 10 |
| 17 | Average fan-out | 0.91 |

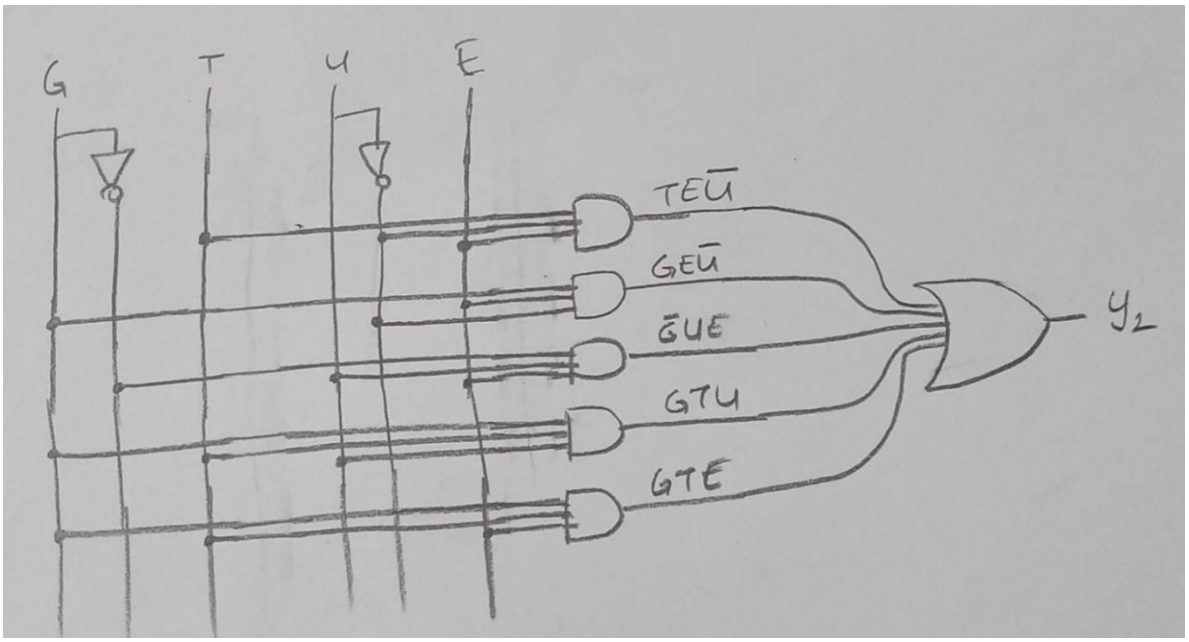



## Problem 2:

**Truth table:**

| G | T | U | E | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Devre Şeması:**




**Kodlar:**

D:/repos/Lojik/Lojik_Lab1/lab1_g8_p2.sv (/tb_lab1_g8_p2/dut0) - Default

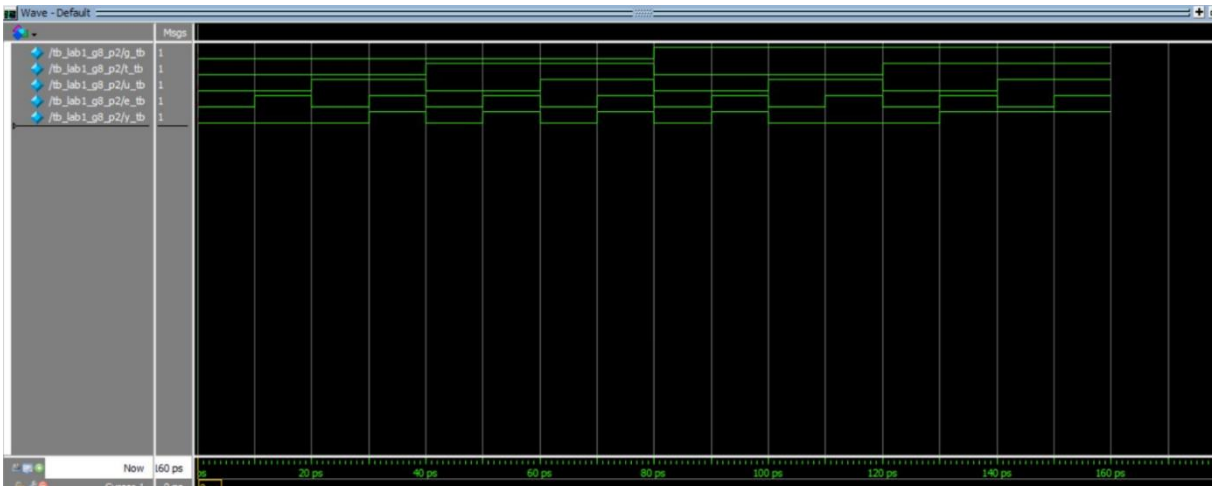
Ln#

```
1
2   // Y = TEU'+GEU'+G'UE+GTU+GTE
3   module lab1_g8_p2(
4       input logic g, t, u, e,
5       output logic y
6   );
7
8   assign y = t&e&~u | g&e&~u | ~g&u&e | g&t&u | g&t&e;
9
10  endmodule
```

D:/repos/Lojik/Lojik_Lab1/tb_lab1_g8_p2.sv (/tb_lab1_g8_p2) - Default

```
Ln#
 1
 2  module tb_lab1_g8_p2 ();
 3      logic g_tb, t_tb, u_tb, e_tb;
 4      logic y_tb;
 5
 6
 7  lab1_g8_p2 dut0(g_tb, t_tb, u_tb, e_tb, y_tb);
 8
 9  initial begin
10
11      g_tb = 0; t_tb = 0; u_tb = 0; e_tb = 0;             #10
12      e_tb = 1;                                           #10
13      u_tb = 1; e_tb = 0;                                 #10
14      e_tb = 1;                                           #10
15      t_tb = 1; u_tb = 0; e_tb = 0;                       #10
16      e_tb = 1;                                           #10
17      u_tb = 1; e_tb = 0;                                 #10
18      e_tb = 1;                                           #10
19      g_tb = 1; t_tb = 0; u_tb = 0; e_tb = 0;             #10
20      e_tb = 1;                                           #10
21      u_tb = 1; e_tb = 0;                                 #10
22      e_tb = 1;                                           #10
23      t_tb = 1; u_tb = 0; e_tb = 0;                       #10
24      e_tb = 1;                                           #10
25      u_tb = 1; e_tb = 0;                                 #10
26      g_tb = 1; t_tb = 1; u_tb = 1; e_tb = 1;             #10
27
28      $stop;
29  end
30
31
```

**Zaman Diyagramı:**



**Quartus:**

**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | Successful - Fri Apr 28 00:03:40 2023 |
| Quartus Prime Version | 22.1std.1 Build 917 02/14/2023 SC Lite Edition |
| Revision Name | lab1_g8_p2 |
| Top-level Entity Name | lab1_g8_p2 |
| Family | MAX 10 |
| Device | 10M08DAF484C8G |
| Timing Models | Final |
| Total logic elements | 2 / 8,064 ( < 1 % ) |
| Total registers | 0 |
| Total pins | 5 / 250 ( 2 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 387,072 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 48 ( 0 % ) |
| Total PLLs | 0 / 2 ( 0 % ) |
| UFM blocks | 0 / 1 ( 0 % ) |
| ADC blocks | 0 / 1 ( 0 % ) |

**Analysis & Synthesis Summary**

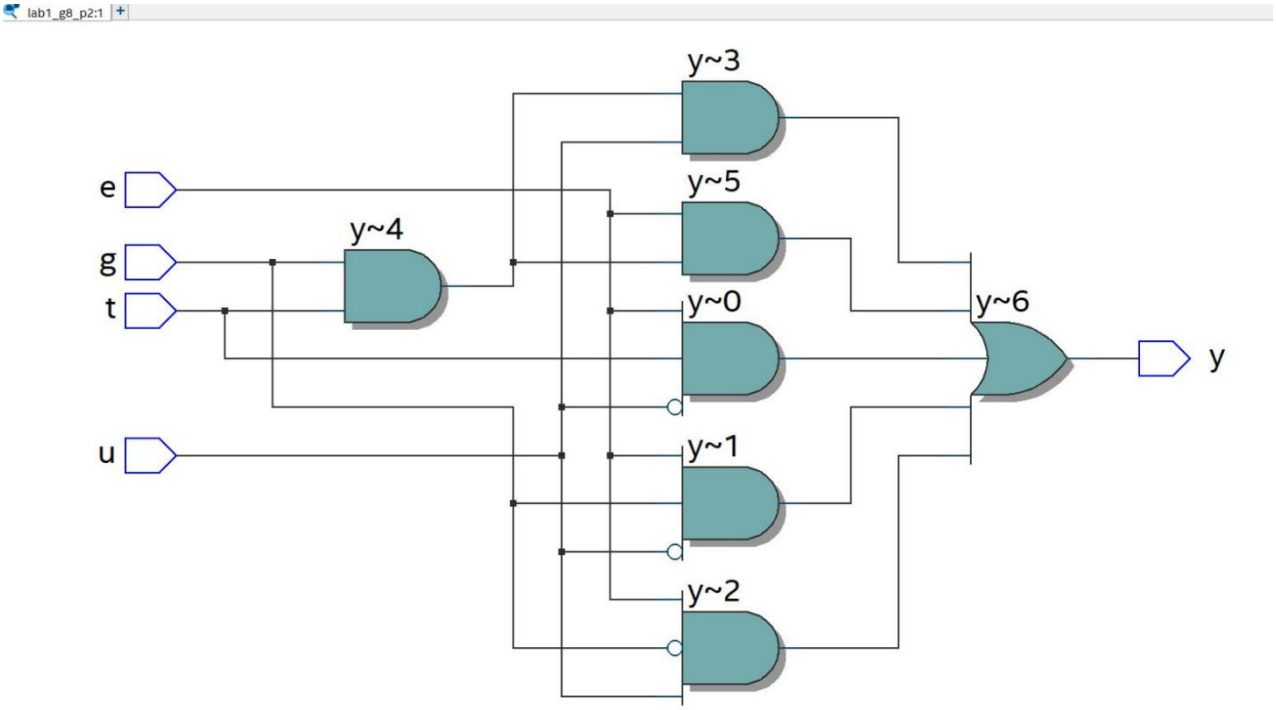
<<Filter>>

| | |
|---|---|
| Analysis & Synthesis Status | Successful - Fri Apr 28 00:03:32 2023 |
| Quartus Prime Version | 22.1std.1 Build 917 02/14/2023 SC Lite Edition |
| Revision Name | lab1_g8_p2 |
| Top-level Entity Name | lab1_g8_p2 |
| Family | MAX 10 |
| Total logic elements | 1 |
| Total registers | 0 |
| Total pins | 5 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |
| UFM blocks | 0 |
| ADC blocks | 0 |

**Analysis & Synthesis Resource Usage Summary**

<<Filter>>

| | Resource | Usage |
|---|---|---|
| 1 | Estimated Total logic elements | 1 |
| 2 | | |
| 3 | Total combinational functions | 1 |
| 4 | ▼ Logic element usage by number of LUT inputs | |
| 1 | -- 4 input functions | 1 |
| 2 | -- 3 input functions | 0 |
| 3 | -- <=2 input functions | 0 |
| 5 | | |
| 6 | ▼ Logic elements by mode | |
| 1 | -- normal mode | 1 |
| 2 | -- arithmetic mode | 0 |
| 7 | | |
| 8 | ▼ Total registers | 0 |
| 1 | -- Dedicated logic registers | 0 |
| 2 | -- I/O registers | 0 |
| 9 | | |
| 10 | I/O pins | 5 |
| 11 | | |
| 12 | Embedded Multiplier 9-bit elements | 0 |
| 13 | | |
| 14 | Maximum fan-out node | y~0 |
| 15 | Maximum fan-out | 1 |
| 16 | Total fan-out | 10 |
| 17 | Average fan-out | 0.91 |

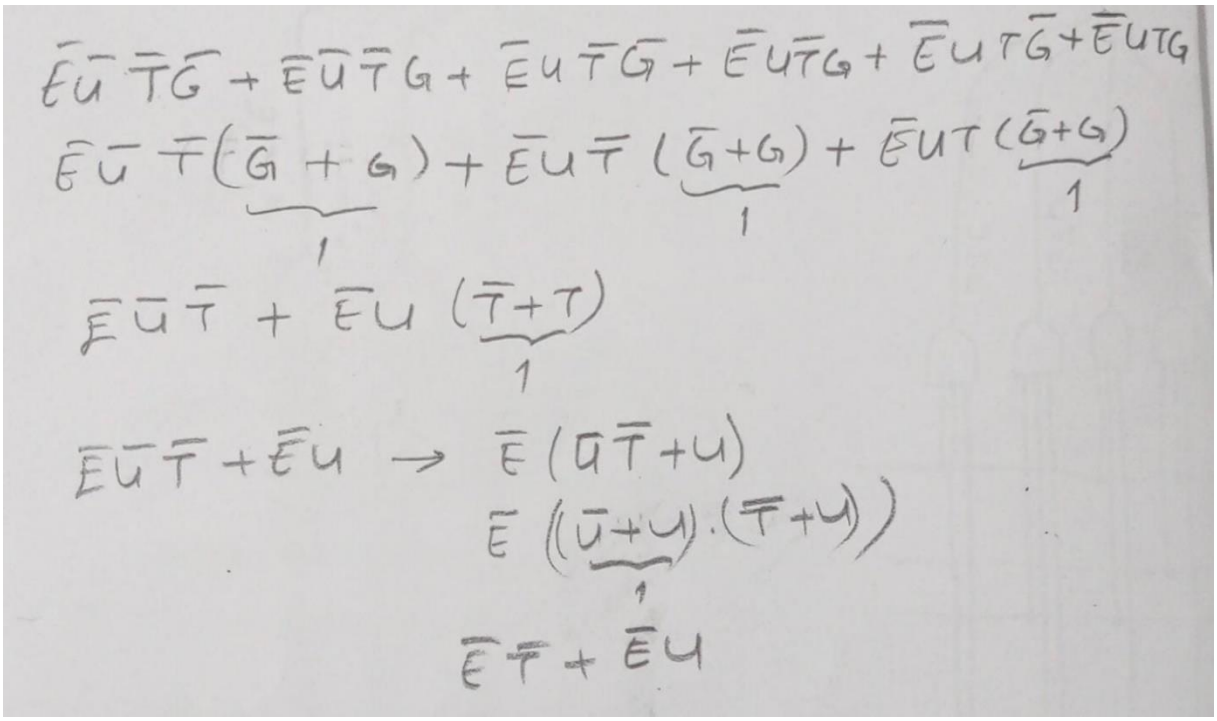


**Problem 3:**

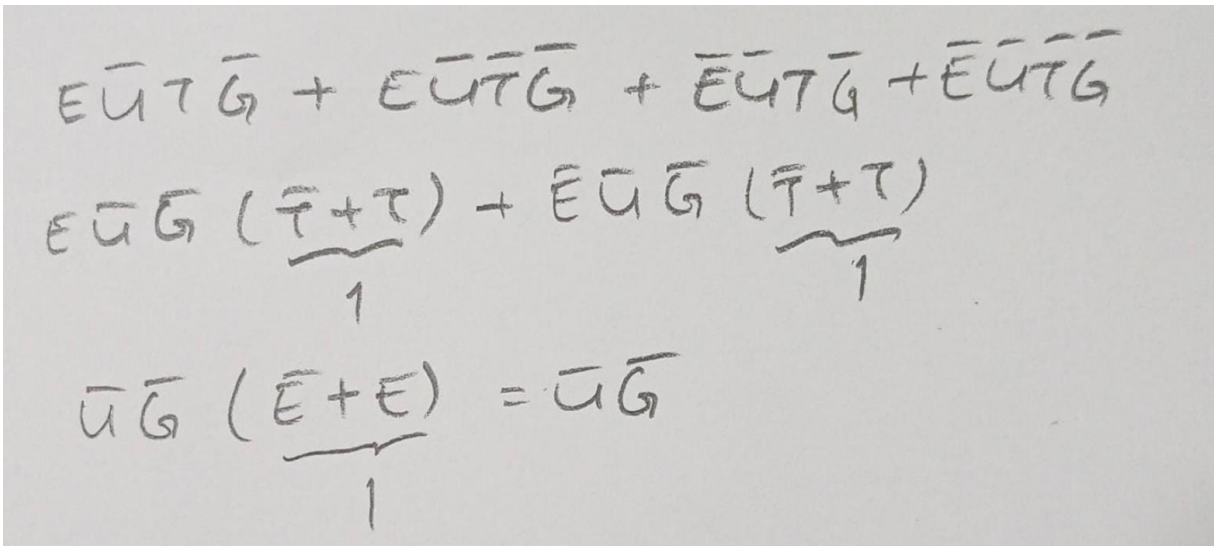
**Truth table:**

| E | U | T | G | X | Y |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

**X Sadeleştirme:**



**Y sadeleştirme:**



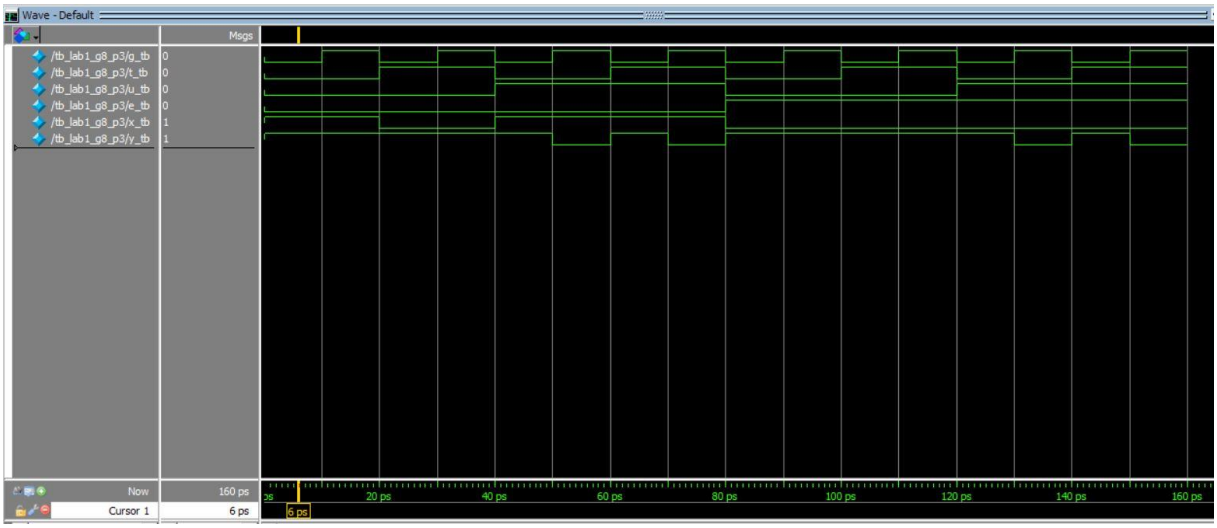

**Kod ve Çıktılar:**

D:/repos/Lojik/Lojik_Lab1/tb_lab1_g8_p3.sv (/tb_lab1_g8_p3) - Default

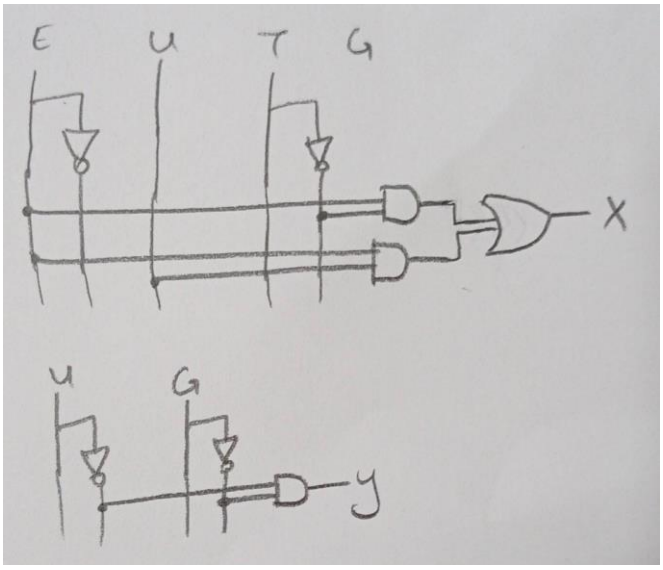
```
Ln#
 2
 3  module tb_lab1_g8_p3 ();
 4      logic g_tb, t_tb, u_tb, e_tb;
 5      logic x_tb;
 6      logic y_tb;
 7
 8  lab1_g8_p3 dut0(g_tb, t_tb, u_tb, e_tb, x_tb,y_tb);
 9  //lab1_g8_p3 dut0(g_tb, t_tb, u_tb, e_tb, y_tb);
10
11
12  initial begin
13
14      g_tb = 0; t_tb = 0; u_tb = 0; e_tb = 0;              #10
15      g_tb = 1;                                            #10
16      t_tb = 1; g_tb = 0;                                  #10
17      g_tb = 1;                                            #10
18      u_tb = 1; t_tb = 0; g_tb = 0;                        #10
19      g_tb = 1;                                            #10
20      t_tb = 1; g_tb = 0;                                  #10
21      g_tb = 1;                                            #10
22      e_tb = 1; t_tb = 0; u_tb = 0; g_tb = 0;              #10
23      g_tb = 1;                                            #10
24      t_tb = 1; g_tb = 0;                                  #10
25      g_tb = 1;                                            #10
26      t_tb = 0; u_tb = 1; g_tb = 0;                        #10
27      g_tb = 1;                                            #10
28      t_tb = 1; g_tb = 0;                                  #10
29      g_tb = 1; t_tb = 1; u_tb = 1; g_tb = 1;              #10
30
31      $stop;
32  end
```

D:/repos/Lojik/Lojik_Lab1/lab1_g8_p3.sv (/tb_lab1_g8_p3/dut0) - Default

```
Ln#
 1  // X = E'T' + E'U
 2  // Y = U' + G'
 3  module lab1_g8_p3(
 4      input logic g, t, u, e,
 5      output logic x,y
 6  );
 7
 8
 9  assign x = ~e&~t | ~e&u;
10
11  assign y = ~u | ~g;
12
13  endmodule
```




**Devre Şemaları:**



**Quartus:**

**Flow Summary**

<<Filter>>

| | |
|---|---|
| Flow Status | Successful - Fri Apr 28 01:31:38 2023 |
| Quartus Prime Version | 22.1std.1 Build 917 02/14/2023 SC Lite Edition |
| Revision Name | lab1_g8_p3 |
| Top-level Entity Name | lab1_g8_p3 |
| Family | MAX 10 |
| Device | 10M08DAF484C8G |
| Timing Models | Final |
| Total logic elements | 3 / 8,064 ( < 1 % ) |
| Total registers | 0 |
| Total pins | 6 / 250 ( 2 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 387,072 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 48 ( 0 % ) |
| Total PLLs | 0 / 2 ( 0 % ) |
| UFM blocks | 0 / 1 ( 0 % ) |
| ADC blocks | 0 / 1 ( 0 % ) |

**Analysis & Synthesis Summary**

<<Filter>>

| | |
|---|---|
| Analysis & Synthesis Status | Successful - Fri Apr 28 01:31:30 2023 |
| Quartus Prime Version | 22.1std.1 Build 917 02/14/2023 SC Lite Edition |
| Revision Name | lab1_g8_p3 |
| Top-level Entity Name | lab1_g8_p3 |
| Family | MAX 10 |
| Total logic elements | 2 |
| Total registers | 0 |
| Total pins | 6 |
| Total virtual pins | 0 |
| Total memory bits | 0 |
| Embedded Multiplier 9-bit elements | 0 |
| Total PLLs | 0 |
| UFM blocks | 0 |
| ADC blocks | 0 |

**Analysis & Synthesis Resource Usage Summary**

<<Filter>>

| | Resource | Usage |
|---|---|---|
| 1 | Estimated Total logic elements | 2 |
| 2 | | |
| 3 | Total combinational functions | 2 |
| 4 | ▼ Logic element usage by number of LUT inputs | |
| 1 | -- 4 input functions | 0 |
| 2 | -- 3 input functions | 1 |
| 3 | -- <=2 input functions | 1 |
| 5 | | |
| 6 | ▼ Logic elements by mode | |
| 1 | -- normal mode | 2 |
| 2 | -- arithmetic mode | 0 |
| 7 | | |
| 8 | ▼ Total registers | 0 |
| 1 | -- Dedicated logic registers | 0 |
| 2 | -- I/O registers | 0 |
| 9 | | |
| 10 | I/O pins | 6 |
| 11 | | |
| 12 | Embedded Multiplier 9-bit elements | 0 |
| 13 | | |
| 14 | Maximum fan-out node | u~input |
| 15 | Maximum fan-out | 2 |
| 16 | Total fan-out | 13 |
| 17 | Average fan-out | 0.93 |