UNIVERSITY of DENVER

VLSI

October 20th 2023

Due date: November 3rd 2023

Name:_____ DU ID:_____ Section:____

Lab 5 – Directions

Part 1

Draft schematics, layouts, and symbols for a 2-input NAND gate and a 2-input XOR gate using 6u/2u MOSFETs (both NMOS and PMOS)

- Ensure that your symbol views are commonly used symbols (not boxes) for these gates with your initials in the middle of the symbol
- Endure all layouts in this lab use standard cell frames that snap together end-to-end for routing vdd and gnd.
- Ensure gate inputs, outputs, vdd, and gnd are all routed in metal1
- Simulate the logic operation of the gates for all 4 possible inputs (00, 01, 10, 11).
- Comment on how timing of the input pulses can cause glitches in the output of a gate.
- DRC and NCC your designs

Part 2

Using the gates from Part 1, draft the schematic, layout, and symbol of a full adder (truth table and circuit below).

- Simulate the operation of the full adder
- Layout the full adder by placing the 5 gates end-to-end so that vdd and gnd are routed
- Full adder inputs and outputs can be on metal 2 but not metal 3
- DRC and NCC your designs

Your lab report should document the all process of building and simulating the circuits from Part 1 and Part2.

Don’t forget to include all necessary explanations to support all the decisions taken during the design of the schematics, layouts and simulations.

Good luck and have fun.

Auxiliary Pictures

a	b	cin	cout	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 1 - Full Adder Truth Table

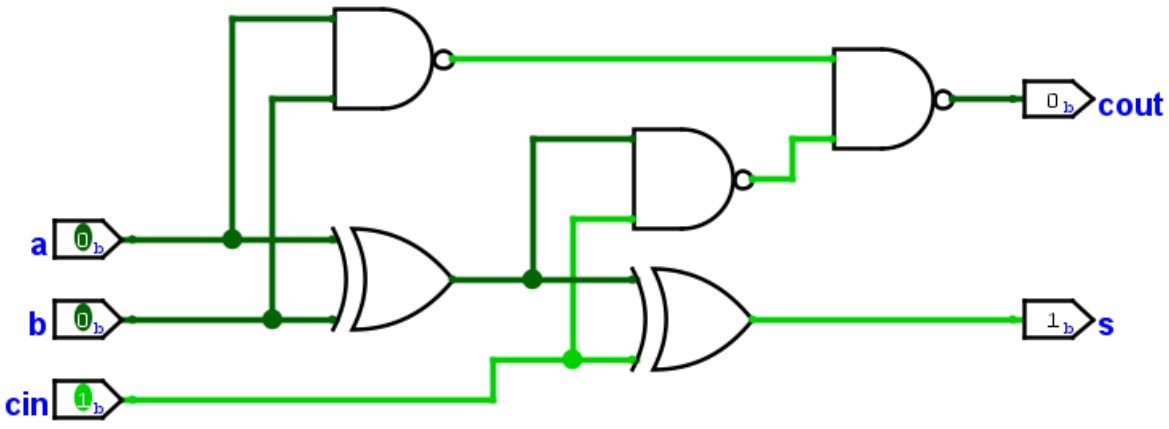

Figure 2 - Full Adder Circuit