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Size	Title:	REV
A3	ROCK 5B	
	Page Name: 01.Index and Notes	1.1
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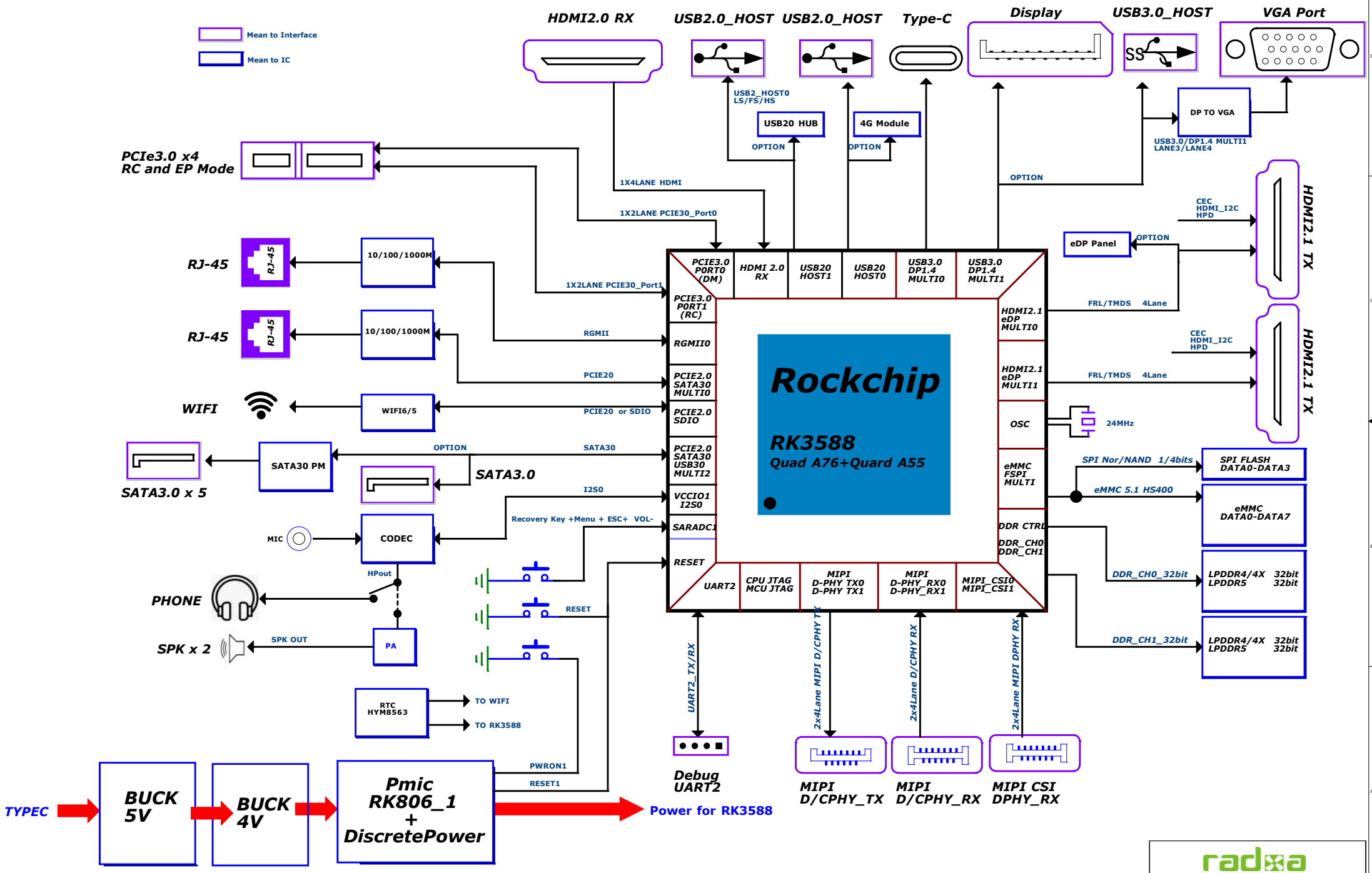

Size: A2	Title: ROCK 5B	REV: 1.1
	Page Name: 02.Block Diagram	
Date: Wednesday, June 29, 2022	Sheet 2 of 33	

Power Tree

typec 20v,15v,12v → typec

Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe

DC/DC 5000mA → VCC4V0_SYS Seq:0

DC/DC 8000mA → VCC5V0_SYS Seq:0

VCC5V0_SYS:
- FAN Max:
- TYPEC0 Max:
- USB30_HOST Max:
- USB2.0 HOST Max:
- VCC5V_HDMI_TX0/1 Max:
- 40PIN Header

RK806-1

Power on Sequence

VCC1	BUCK1 6.5A max	Seq:5	VDD_GPU_S0 Max:5926mA	VDD_GPU / VDD_GPU_MEM
VCC2	BUCK2 5.0A max	Seq:3	VDD_CPU_LIT_S0 Max:4500mA	VDD_CPU_LIT / VDD_CPU_LIT_MEM
VCC3	BUCK3 5.0A max	Seq:2	VDD_LOGIC_S0 Max:3500mA	VDD_LOGIC
VCC4	BUCK4 5.0A max	Seq:5	VDD_VDENC_S0 Max:3150mA	VDD_VDENC / VDD_VDENC_MEM
VCC5	BUCK5 2.5A max	Seq:2	VDD_DDR_S0 Max:2300mA	VDD_DDR_S0 → DDR_CH0_VDD Max:, DDR_CH0_VDD_MIF Max:, DDR_CH1_VDD Max:, DDR_CH1_VDD_MIF Max:
VCC6	BUCK6 2.5A max	Seq:4	VDD2_DDR_S3 Max:1000mA	LPDDR4_VDDQ Max:, LPDDR4/4x VDD2 Max:, LPDDR5 VDD2H Max:, DDR_CH0/1_VDDQ_CKE Max:
VCC7	BUCK7 2.5A max	Seq:1	VCC_2V0_PLDO_S3 Max:	
VCC8	BUCK8 2.5A max	Seq:6	VCC_3V3_S3	VCC_3V3_S3 → MOS → VCC_3V3_S0 → VGA IC Max:, LCD Max:, RGMII Max:; Typec CC IC Max:, WIFI_BATT Max:, eMMC VCC Max:, VCC_RTC Max:, Hall IC Max:, Camera Input Max:, IR Receiver Max:, Debug Max:, PMUIO2 Max:, VCCIO5&VCCIO6 Max:
VCC9	BUCK9 2.5A max	Seq:6	VDDQ_DDR_S0 Max:500mA	VDDQ_DDR_S0 → LPDDR4x/LPDDR5 VDDQ Max:, DDR_CH1_VDDQ_CK Max:, DDR_CH0_VDDQ_CK Max:, DDR_CH1_VDDQ Max:, DDR_CH0_VDDQ Max:
VCC10	BUCK10 2.5A max	Seq:3	VCC_1V8_S3	VCC_1V8_S3 → VDD1_1V8_DDR Max:, WIFI_VDDIO Max:, eMMC VCCQ Max:, EMMCIO_1V8 Max:, PMUIO1_1V8 Max:, PMUIO2_1V8 Max:
	PLDO1 500mA max	Seq:3	VCCA_1V8_S0	VCCA_1V8_S0 → OSC_1V8 Max:, PLL_AVDD1V8 Max:, USB20_AVDD_1V8 Max:, SARADC_AVDD_1V8 Max:, DDR_CH0_PLL_AVDD1V8 Max:, DDR_CH1_PLL_AVDD1V8 Max:, TYPEC0_DP0_VDDH_1V8 Max:, TYPEC0_DP1_VDDH_1V8 Max:, PCIE20_SATA30_0_AVDD_1V8 Max:, PCIE20_SATA30_1_AVDD_1V8 Max:, PCIE20_SATA30_USB30_2_AVDD_1V8 Max:, PCIE30_PORT0_AVDD1V8 Max:, PCIE30_PORT1_AVDD1V8 Max:
VCC11	PLDO2 300mA max	Seq:3	VCC_1V8_S0	VCC_1V8_S0 → MIPI_CSI0_AVCC1V8 Max:, MIPI_CSI1_AVCC1V8 Max:, HDMI/EDP_TX0_VDD_IO_1V8 Max:, HDMI/EDP_TX0_VDD_CMN_1V8 Max:, HDMI/EDP_TX1_VDD_IO_1V8 Max:, HDMI/EDP_TX1_VDD_CMN_1V8 Max:, MIPI_D/C_PHY0_VDD_1V8 Max:, MIPI_D/C_PHY1_VDD_1V8 Max:, VCCIO1-6_VDD_1V8 Max:, AVCC_1V8_CODEC Max:, RGMII Max:
	PLDO3 300mA max	Seq:4	VDDA_1V2_S0	MIPI_D/C_PHY0_VDD_1V2 Max:, MIPI_D/C_PHY1_VDD_1V2 Max:
VCC12	PLDO4 500mA max	Seq:6	VCCA_3V3_S0	Sensor Max:, CODEC_VCCA3V3 Max:, USB20_AVDD_3V3 Max:, HDMIRX_VPH3V3 Max:, HDMIRX_DVDD3V3 Max:
	PLDO5 300mA max	Seq:6	VCCIO_SD_S0	VCCIO_SD Max:
VCCA	PLDO6 300mA max	Seq:3	VCC_1V8_S3_PLDO6	
	NLDO1 300mA max	Seq:2	VDD_0V75_S3	VDD_0V75_S3 → PMU_0V75 Max:, USB20_DVDD_0V75 Max:, HDMI/EDP_TX0_VDD/AVDD_0V75 Max:, HDMI/EDP_TX1_VDD/AVDD_0V75 Max:, HDMI_RX_AVDD0V75 Max:
VCC13	NLDO2 300mA max	Seq:2	VDDA_DDR_PLL_S0	DDR_CH0_PLL_DVDD Max:, DDR_CH1_PLL_DVDD Max:
	NLDO3 500mA max	Seq:2	VDDA_0V75_S0	VDDA_0V75_S0 → PLL_DVDD0V75 Max:, OTP_VDDOTP_0V75 Max:, MIPI_CSI0_AVCC0V75 Max:, MIPI_CSI1_AVCC0V75 Max:, PCIE30_PORT0_AVDD0V75 Max:, PCIE30_PORT1_AVDD0V75 Max:, MIPI_D/C_PHY0_VDD Max:, MIPI_D/C_PHY1_VDD Max:
VCC14	NLDO4 500mA max	Seq:2	VDDA_0V85_S0	VDDA_0V85_S0 → TYPEC0_DP0_VDD_0V85 Max:, TYPEC0_DP0_VDDA_0V85 Max:, TYPEC0_DP1_VDD_0V85 Max:, TYPEC0_DP1_VDDA_0V85 Max:, PCIE20_SATA30_0_AVDD_0V85 Max:, PCIE20_SATA30_1_AVDD_0V85 Max:, PCIE20_SATA30_USB30_2_AVDD_0V85 Max:
	NLDO5 300mA max	Seq:2	VDD_0V75_S0	VDD_0V75_S0 → (PLL_DVDD0V75, OTP_VDDOTP_0V75, MIPI_CSI0_AVCC0V75, MIPI_CSI1_AVCC0V75, PCIE30_PORT0_AVDD0V75, PCIE30_PORT1_AVDD0V75, MIPI_D/C_PHY0_VDD, MIPI_D/C_PHY1_VDD)

VCC_2V0_PLDO_S3 → VCC11

VCC_1V1_NLDO_S3 → VCC13

VCC_1V1_NLDO_S3 → VCC14

RK860-2 ,6A	Seq:6A	VDD_CPU_BIG0_S0 Max:5100mA	VDDCPU_BIG0 / VDDCPU_BIG0_MEM
RK860-3 ,6A	Seq:6A	VDD_CPU_BIG1_S0 Max:5100mA	VDDCPU_BIG1 / VDDCPU_BIG1_MEM
RK860-2 ,6A	Seq:6A	VDD_NPU_S0 Max:3832mA	VDD_NPU / VDD_NPU_MEM
EXT DC/DC ,2A	Seq:0A	VCC_1V1_NLDO_S3 Max:	VCC_3V3_S3 → LDO or BUCK → VCC_1V2_CAM Max:, VCC_1V8_CAM Max:, VCC_2V8_CAM Max:
EXT DC/DC ,2A	Seq:0A	VDD2L_DDR_S3 Max:	LPDDR5 VDD2L Max:

VCC_3V3_S3 → MOS → VCC3V3_SD_S0 Max:

VCC_3V3_S3 → EN; PMIC_EXT_EN_OUT

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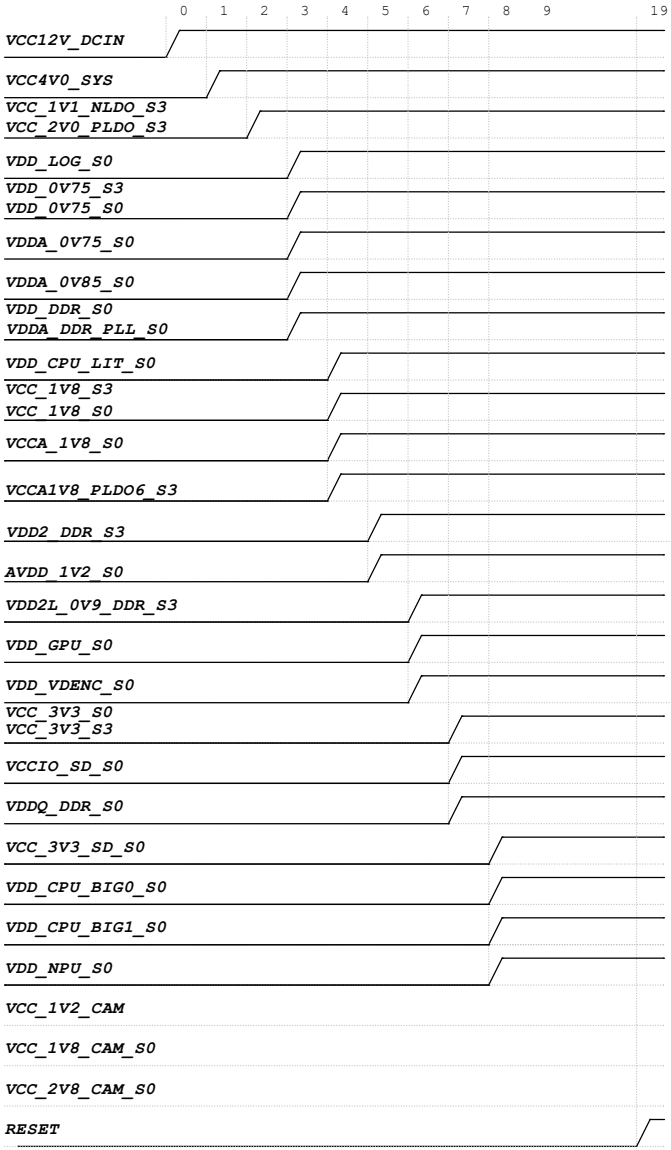
Size	Title:	ROCK 5B				REV
A2	Page Name:	03.Power Tree				1.1
Date:	Wednesday, June 29, 2022	Sheet	3	of	33	

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

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Size	Title:	REV
A3	ROCK 5B	1.1
	Page Name: 04.System Power Sequence	
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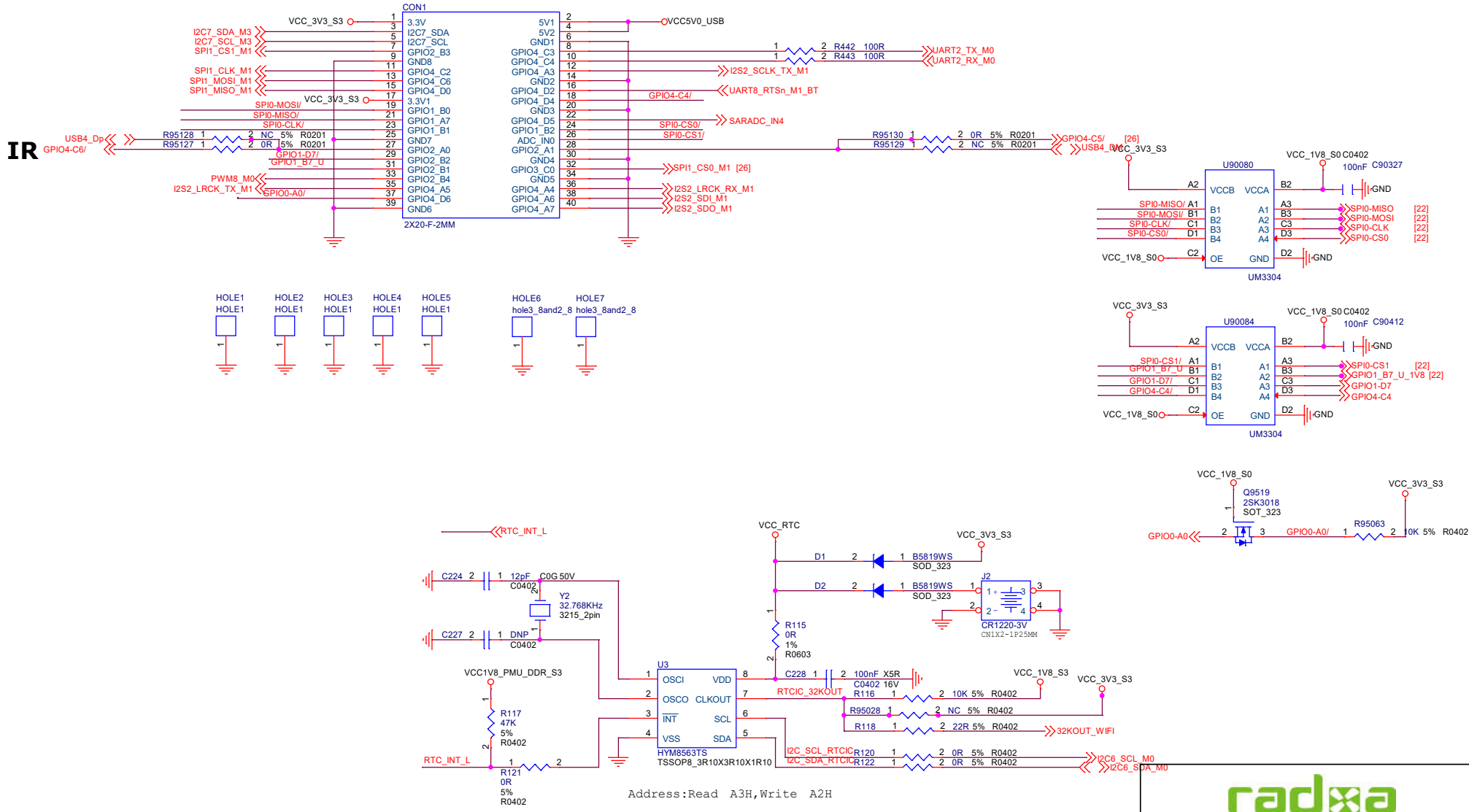
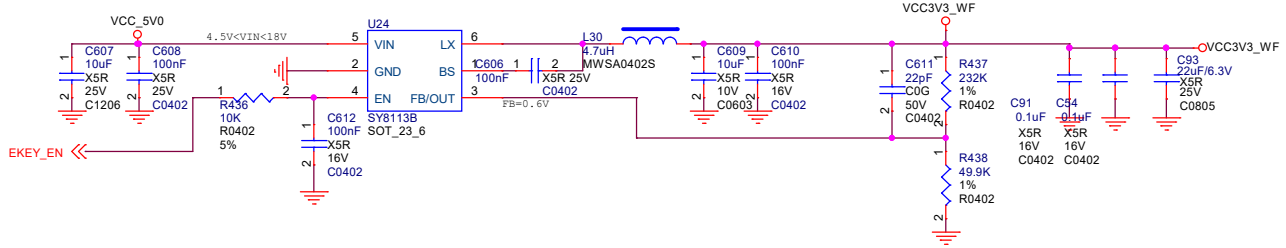
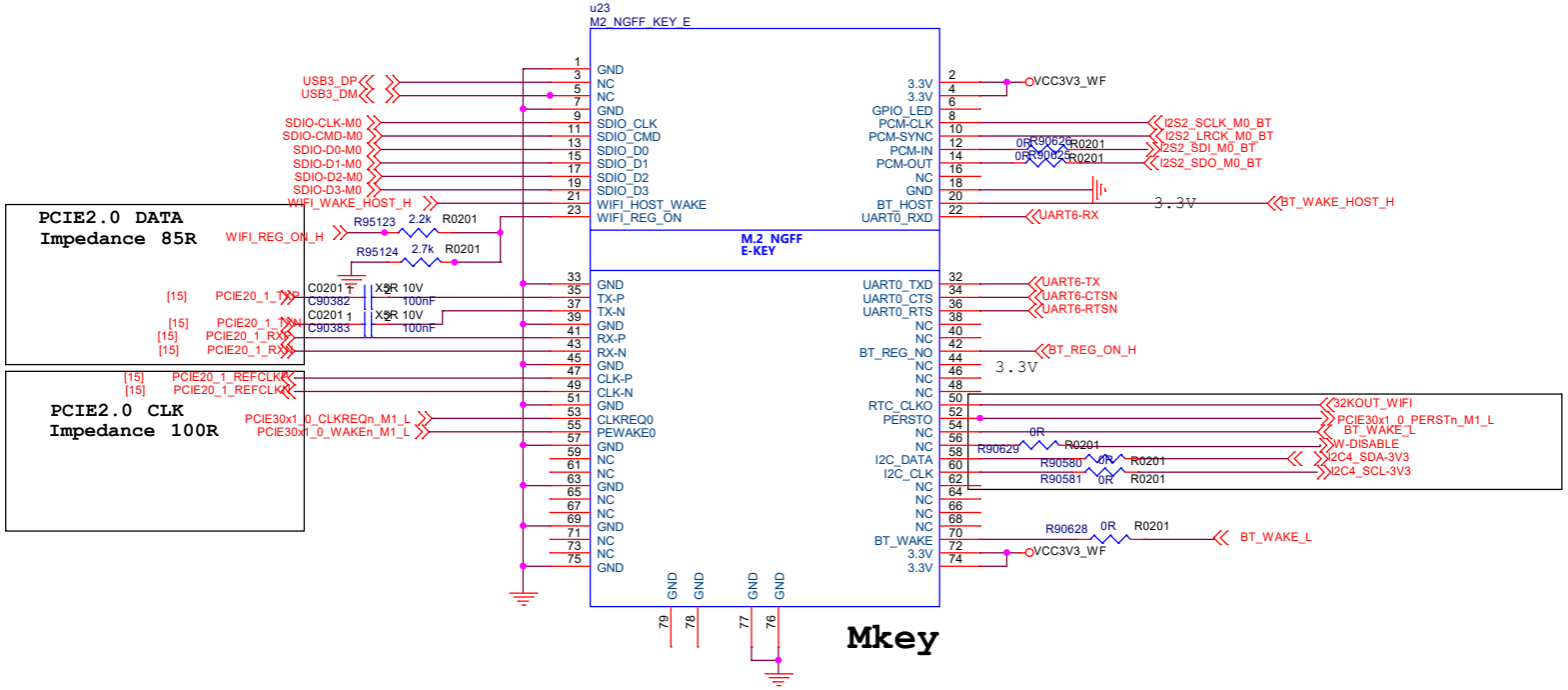
UART TO USB (DEBUG)



Size	Title:	REV
A3	ROCK 5B	1.1
	Page Name: 05.CONNECT	
Date:	Wednesday, June 29, 2022	Sheet 5 of 33



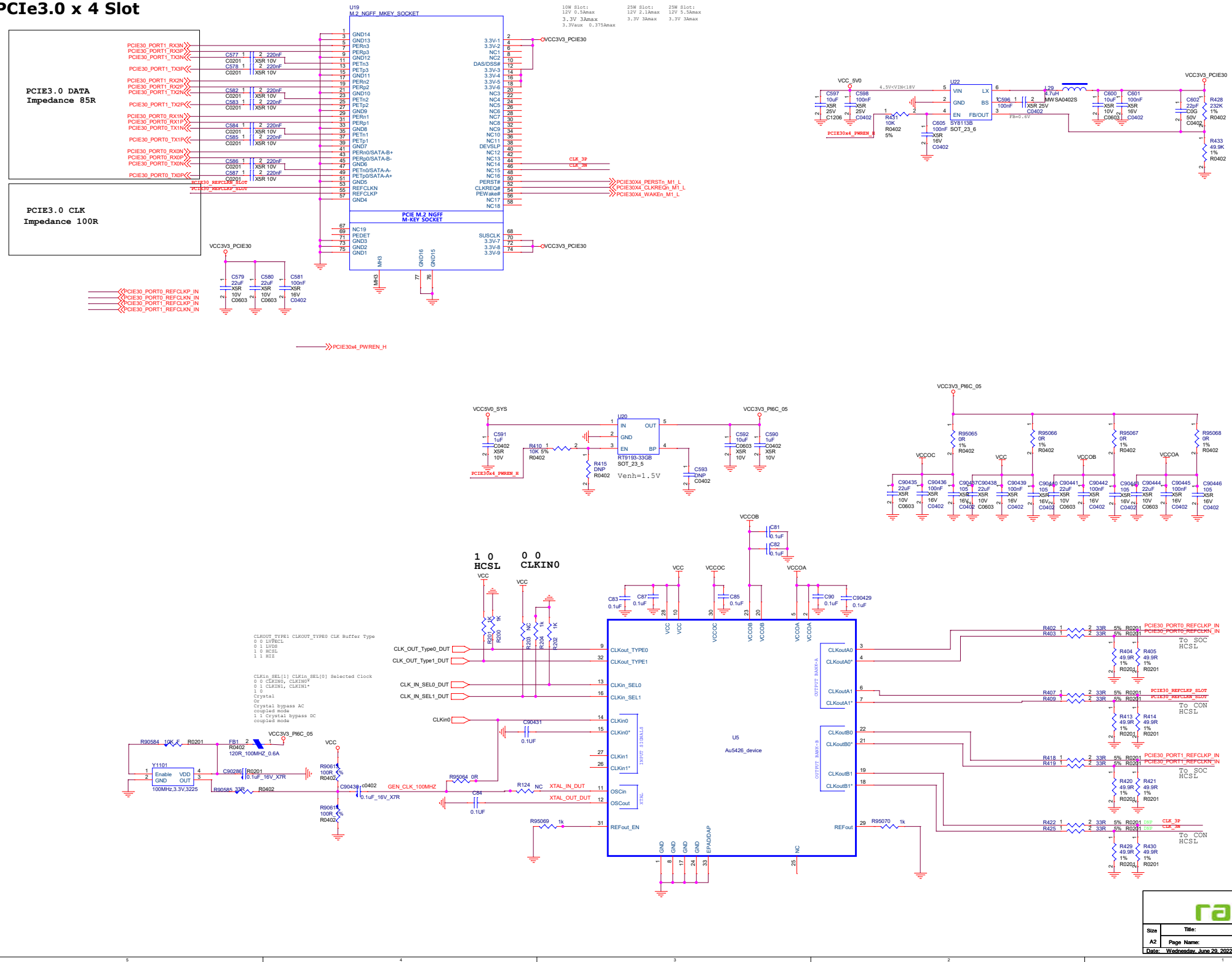


Size	Title:	ROCK 5B	REV
A3	Page Name:	06.PCIE-PCIE2.0_Slot-Ekey	1.1
Date:	Wednesday, June 29, 2022	Sheet 6 of 33	

PCIe3.0 x 4 Slot

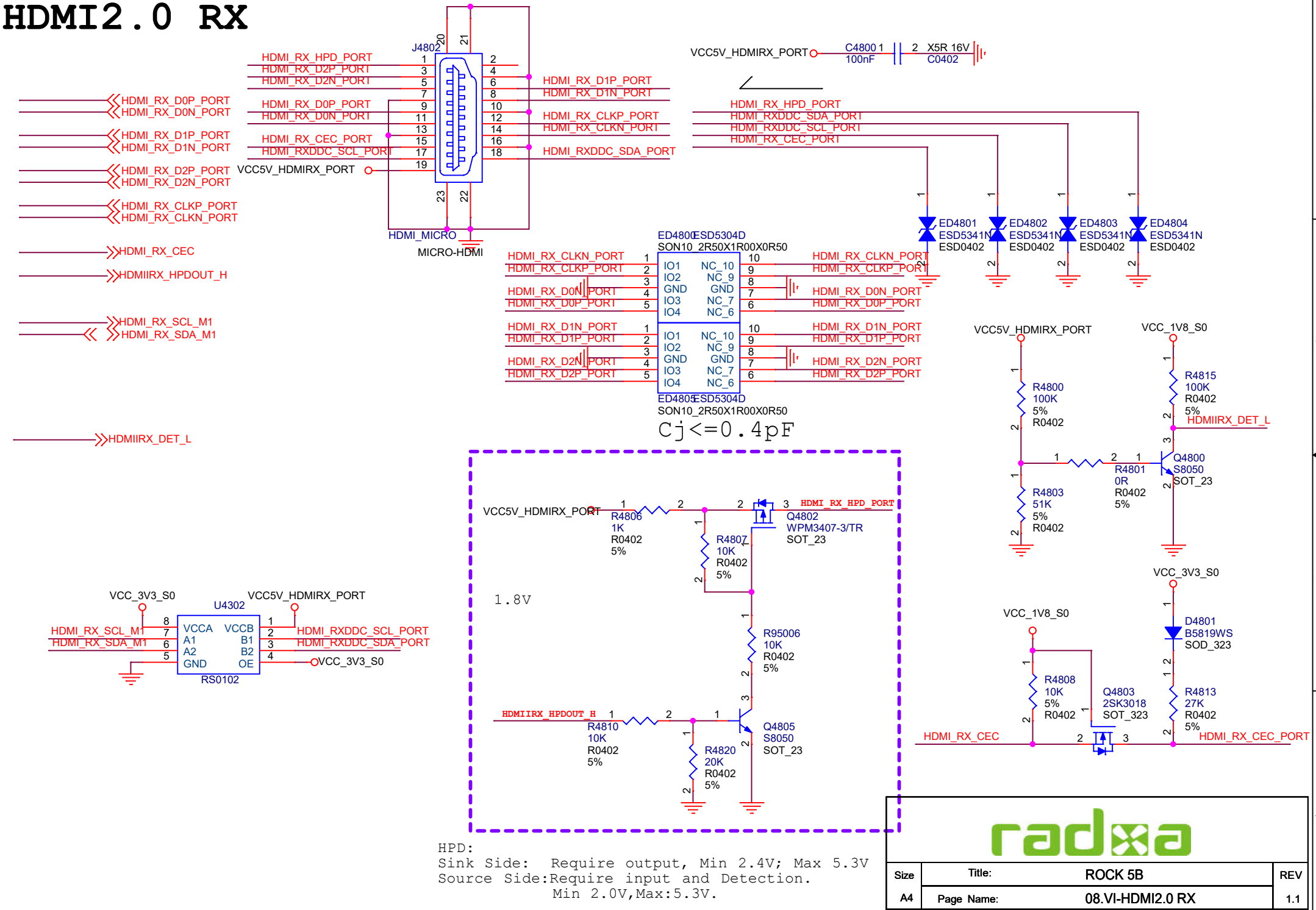
PCIE3.0 DATA
Impedance 85R

PCIE3.0 CLK
Impedance 100R



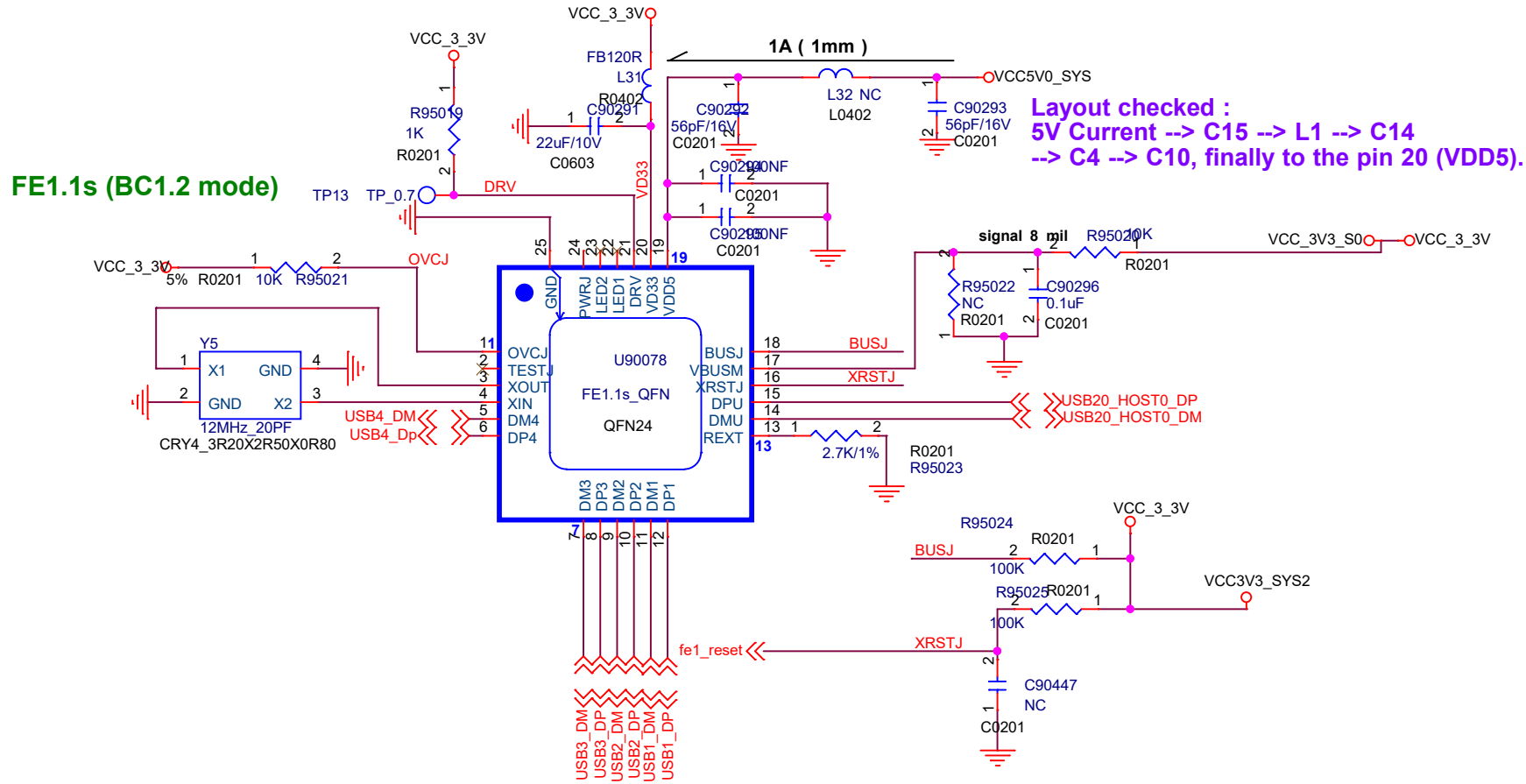
Size	Title: ROCK 5B		REV
A2	Page Name: 07.PCIE-PCIE3.0_Slot-Mkey		1.1
Date: Wednesday, June 29, 2022	Sheet 7 of 33		

HDMI2.0 RX

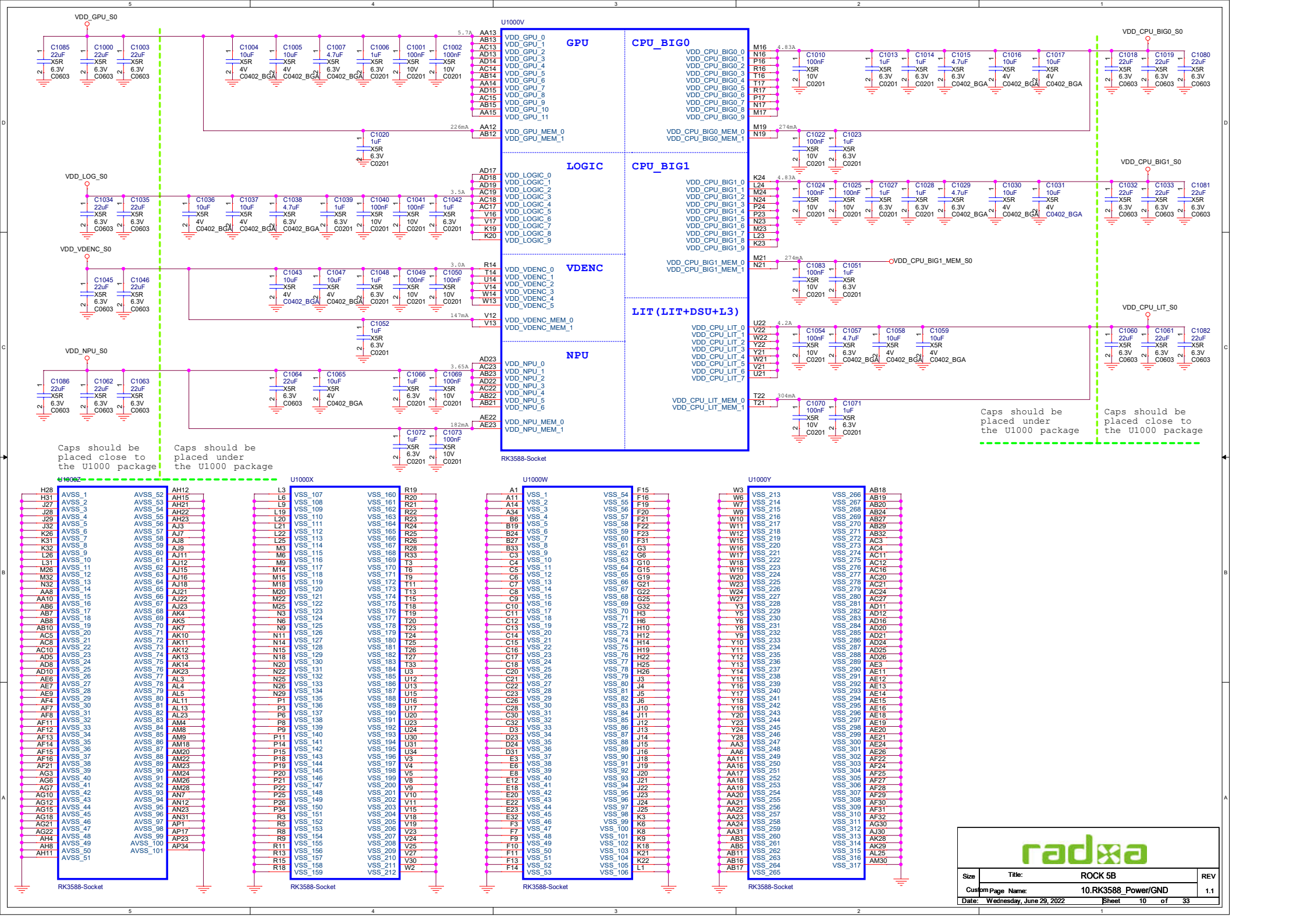


HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V.

Size	Title:	ROCK 5B	REV
A4	Page Name:	08.VI-HDMI2.0 RX	1.1
Date:	Wednesday, June 29, 2022	Sheet 8 of 33	



Size	Title: ROCK 5B	REV
A4	Page Name: 09.USB2HUB	1.1
Date: Wednesday, June 29, 2022	Sheet 9 of 33	


VDD_GPU_S0
U1000V
GPU
LOGIC
VDENC
NPU
CPU_BIG0
CPU_BIG1
LIT(LIT+DSU+L3)
VDD_CPU_BIG0_S0
VDD_CPU_BIG1_S0
VDD_CPU_LIT_S0
VDD_LOG_S0
VDD_VDENC_S0
VDD_NPU_S0
VDD_CPU_BIG1_MEM_S0
Caps should be placed close to the U1000 package
Caps should be placed under the U1000 package
Caps should be placed under the U1000 package
Caps should be placed close to the U1000 package
RK3588-Socket
U1000Z
U1000X
U1000W
U1000Y
RK3588-Socket
RK3588-Socket
RK3588-Socket
RK3588-Socket
radxa
Size
Title: ROCK 5B
REV
Custom
Page Name: 10.RK3588_Power/GND
1.1
Date: Wednesday, June 29, 2022
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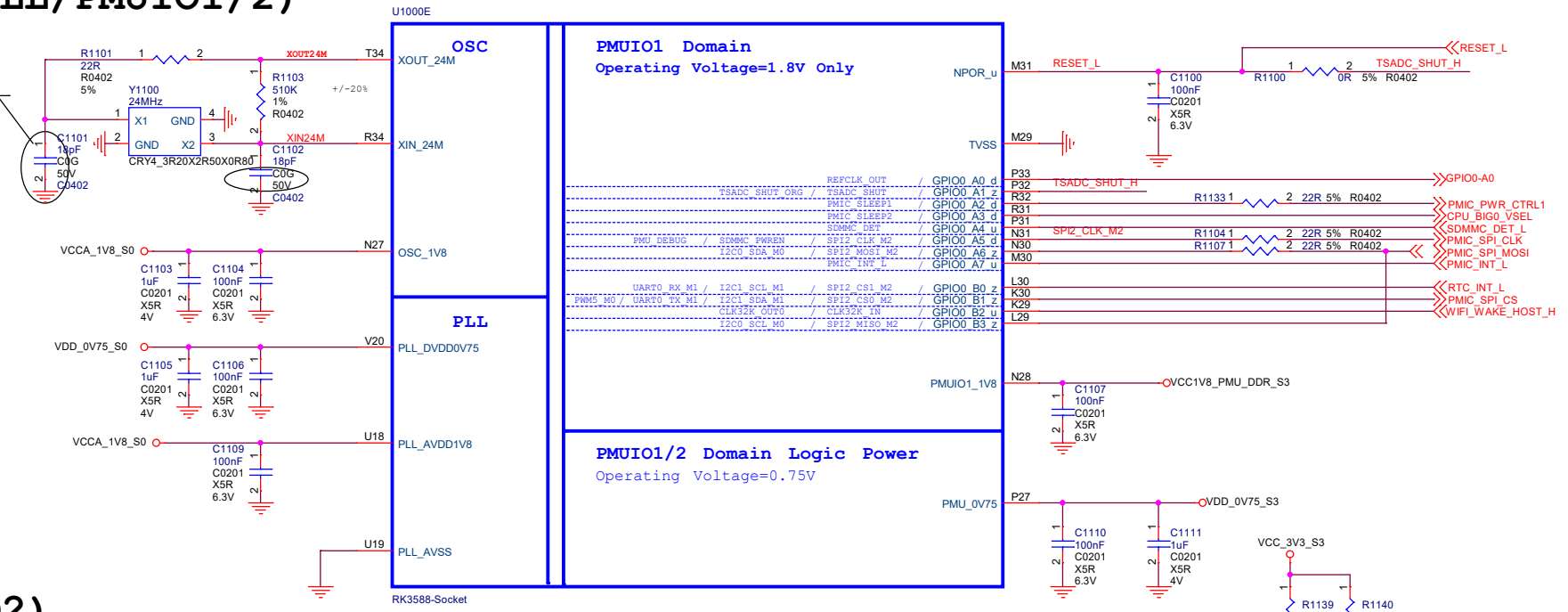
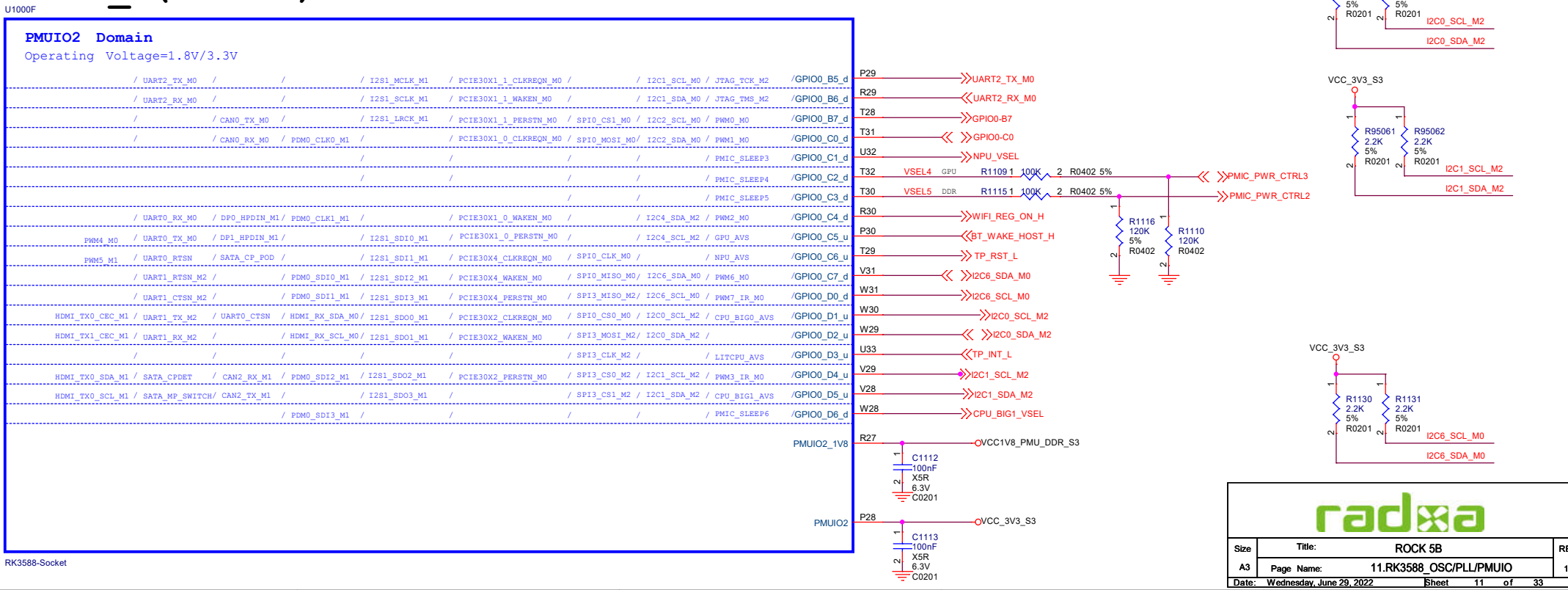
RK3588_E(OSC/PLL/PMUIO1/2)

Note:
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

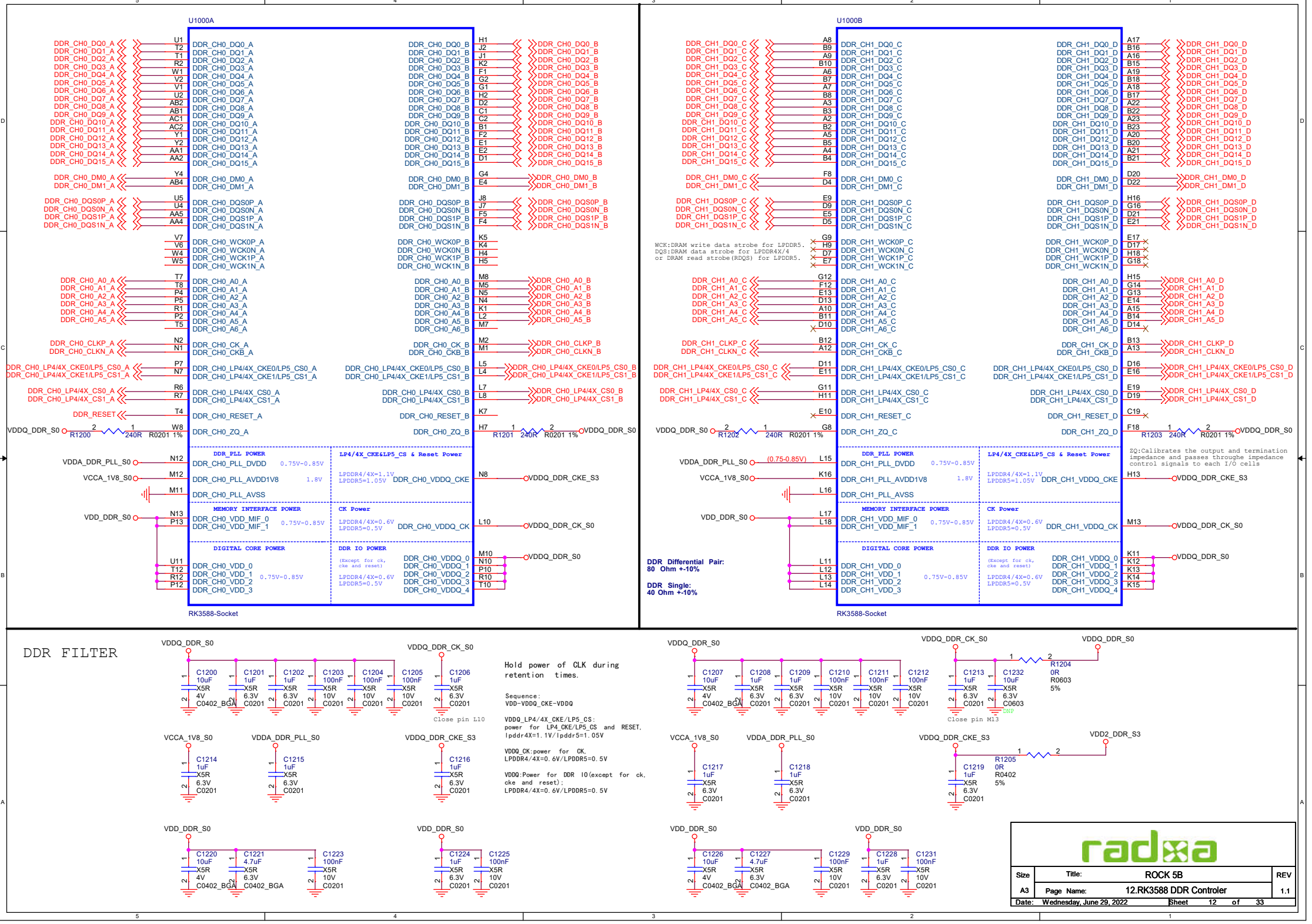
CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<12pF



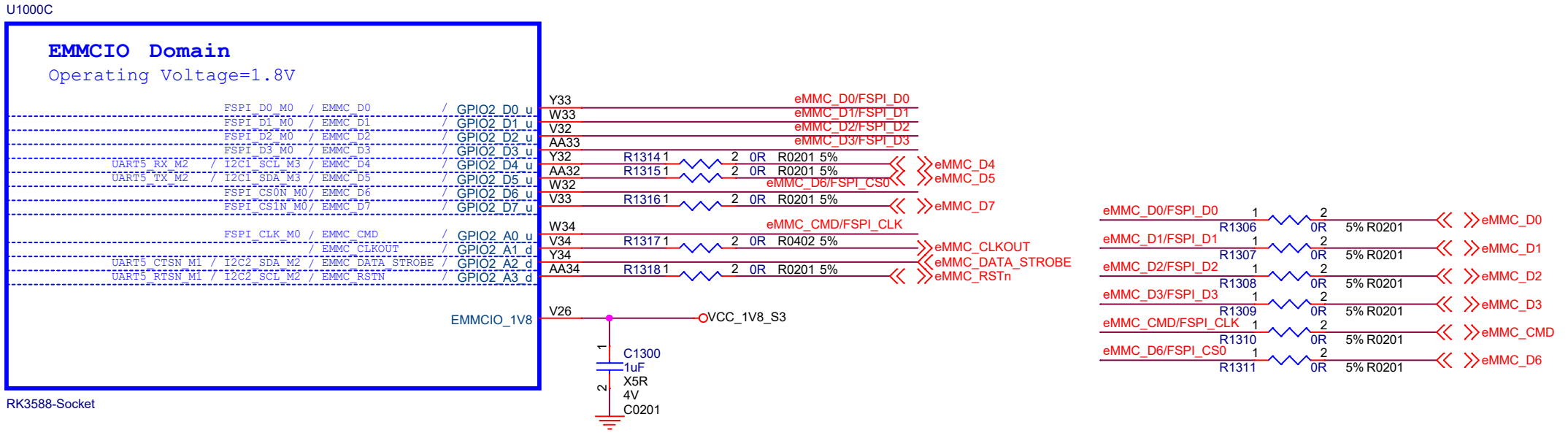
RK3588_F(PMUIO2)



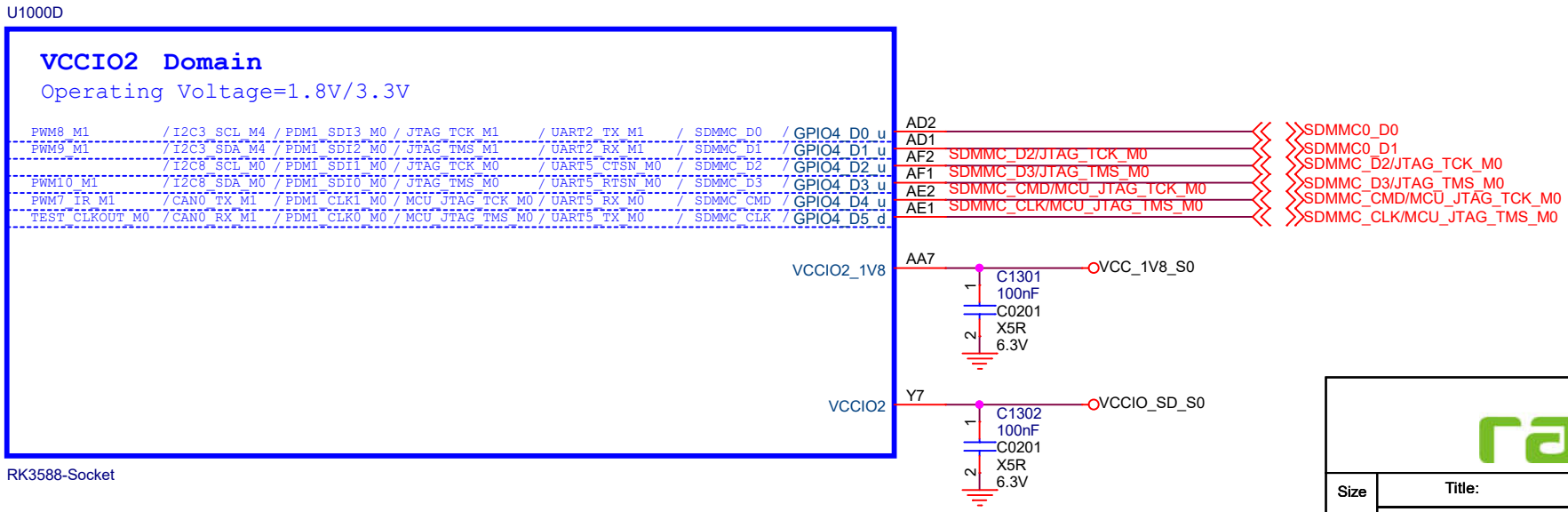
Size: A3	Title: ROCK 5B	REV: 1.1
	Page Name: 11.RK3588_OSC/PLL/PMUIO	
Date: Wednesday, June 29, 2022	Sheet 11 of 33	


U1000A
U1000B
RK3588-Socket
DDR FILTER
DDR Differential Pair:
80 Ohm +-10%
DDR Single:
40 Ohm +-10%
Hold power of CLK during retention times.
Sequence:
VDD-VDDQ_CKE-VDDQ
VDDQ_LP4/4X_CKE/LP5_CS: power for LP4_CKE/LP5_CS and RESET, lpddr4X=1.1V/lpddr5=1.05V
VDDQ_CK:power for CK, LPDDR4/4X=0.6V/LPDDR5=0.5V
VDDQ:Power for DDR IO(except for ck, cke and reset); LPDDR4/4X=0.6V/LPDDR5=0.5V
ZQ:Calibrates the output and termination impedance and passes throughe impedance control signals to each I/O cells
WCK:DRAM write data strobe for LPDDR5.
DQS:DRAM data strobe for LPDDR4X/4
or DRAM read strobe(RDQS) for LPDDR5.
Close pin L10
Close pin M13
Size A3
Title: ROCK 5B
REV 1.1
Page Name: 12.RK3588 DDR Controler
Date: Wednesday, June 29, 2022
Sheet 12 of 33

RK3588_C(EMMCIO Domain)

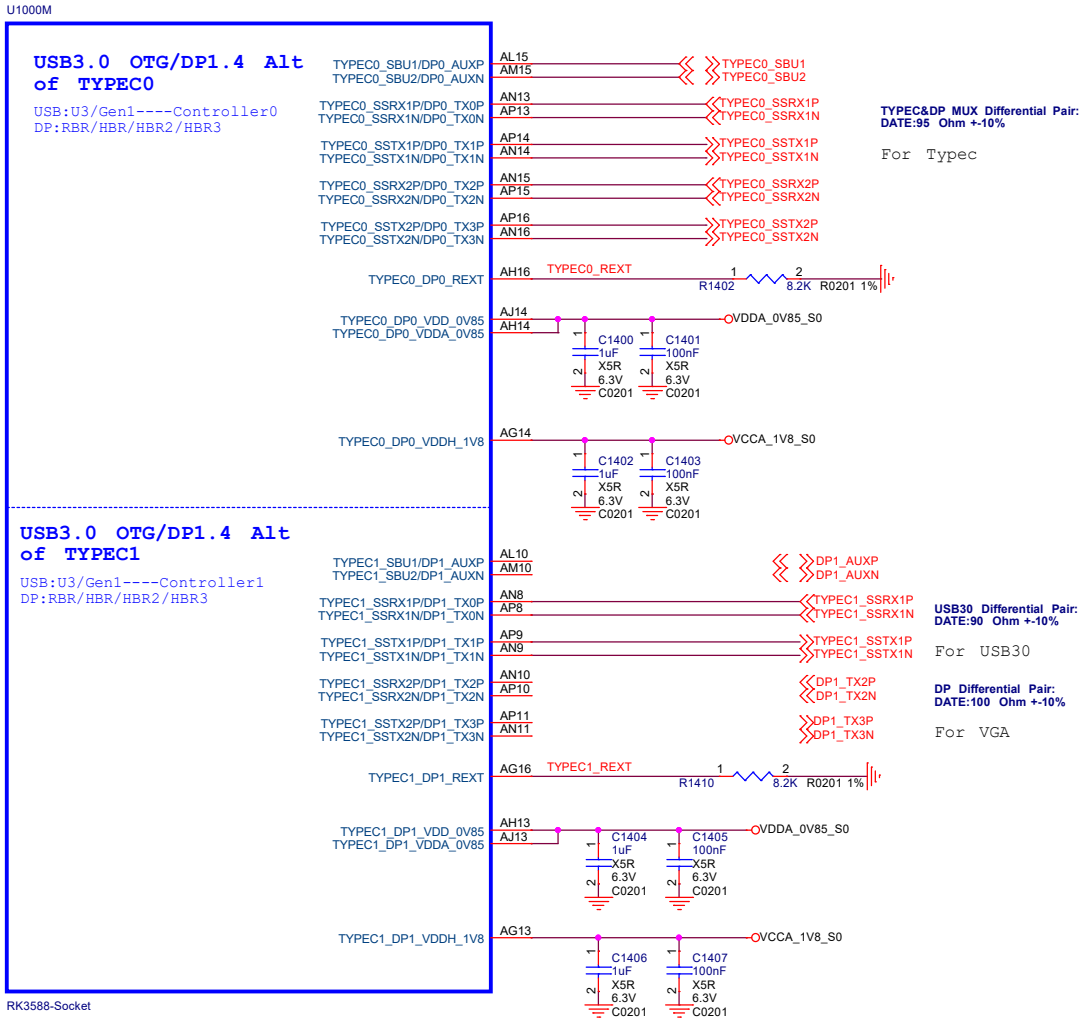


RK3588_D(VCCIO2 Domain)



Size	Title: ROCK 5B	REV
A4	Page Name: 13.RK3588_Flash/SD Controller	1.1
Date: Wednesday, June 29, 2022	Sheet 13 of 33	

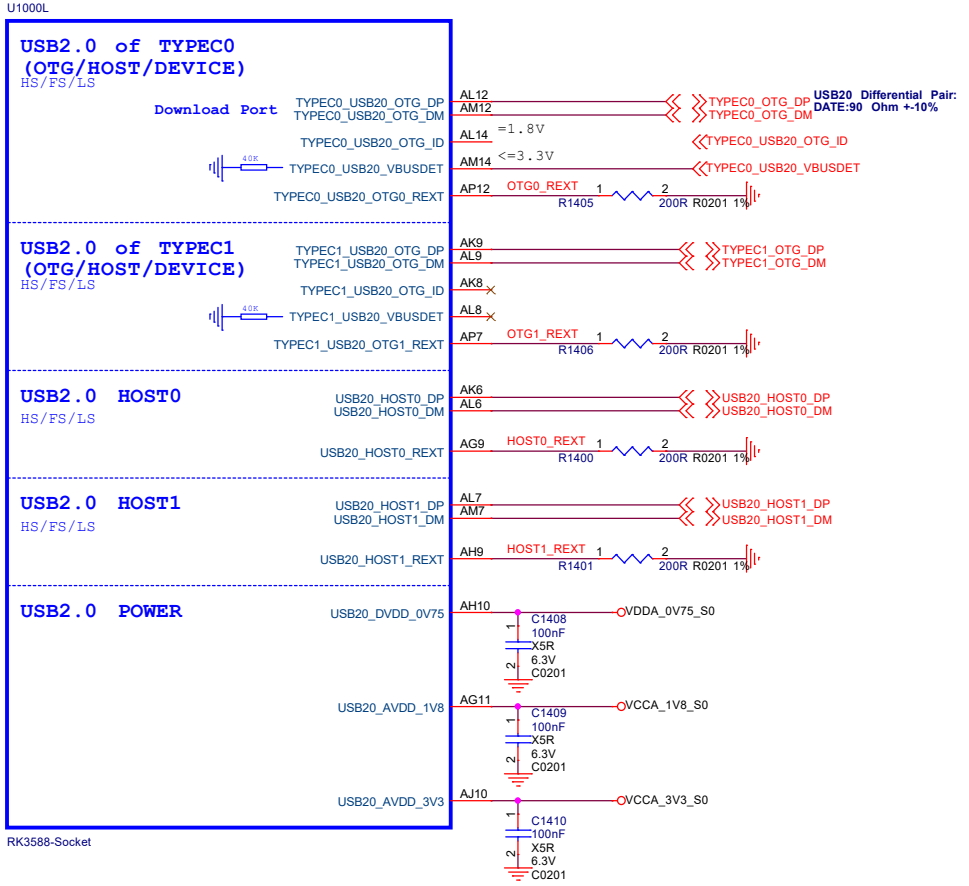
RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Size	Title:	REV
A3	ROCK 5B	1.1
	Page Name: 14.RK3588_USB30/USB20_Ctrl	
Date: Wednesday, June 29, 2022	Sheet 14 of 33	

RK3588_G(VCCIO1 Domain)

U1000G

VCCIO1 Domain

Operating Voltage=1.8V

SPI4_MISO_M0	UART3_RX_M0		I2C3_SDA_M0		GPIO1_C0_z
SPI4_MOSI_M0	UART3_TX_M0		I2C3_SCL_M0		GPIO1_C1_z
SPI4_CLK_M0	UART3_RTSN	PWM3_IR_M2	I2C6_SDA_M1	I2S0_MCLK	GPIO1_C2_d
SPI4_CS0_M0	UART3_CTSN	PWM7_IR_M2	I2C6_SCL_M1	I2S0_SCLK	GPIO1_C3_d
SPI4_CS1_M0		PWM11_IR_M2	I2C2_SDA_M3	PDM0_CLK1_M0	GPIO1_C4_d
	UART4_RTSN		I2C2_SCL_M3	I2S0_LRCK	GPIO1_C5_d
		PWM15_IR_M2	I2C4_SDA_M4	PDM0_CLK0_M0	GPIO1_C6_d
	UART4_CTSN		I2C4_SCL_M4	I2S0_SDO0	GPIO1_C7_d
SPI1_MISO_M2	UART6_TX_M2		I2C7_SCL_M0	I2S0_SDO1	GPIO1_D0_d
SPI1_MOSI_M2	UART6_RX_M2		I2C7_SDA_M0	PDM0_SDI1_M0	I2S0_SDO2/I2S0_SDI3 GPIO1_D1_d
SPI1_CLK_M2	UART4_TX_M0	PWM0_M1	I2C1_SCL_M4	PDM0_SDI2_M0	I2S0_SDO3/I2S0_SDI2 GPIO1_D2_d
SPI1_CS0_M2	UART4_RX_M0	PWM1_M1	I2C1_SDA_M4	PDM0_SDI3_M0	I2S0_SDI1 GPIO1_D3_d
					I2S0_SDI0 GPIO1_D4_d
SPI1_CS1_M2				PDM0_SDI0_M0	GPIO1_D5_d

G29 I2C3_SDA_M0_MIPI
G27 I2C3_SCL_M0_MIPI
F30 I2S0_MCLK
E31 I2S0_SCLK_TX
E30 LCD_PWREN_H
D30 I2S0_LRCK_TX
D29 HDMIIRX_DET_L
E29 I2S0_SDO0

F26 I2C7_SCL_M0_CODEC
F27 I2C7_SDA_M0_CODEC
F28 EKEY_EN
E28 HP_INT
D28 I2S0_SDI0
G26 HP_DETECT

VCCIO1_1V8 G20 VCC_1V8_S0

C1502 100nF X5R 6.3V C0201

RK3588-Socket

VCC_1V8_S0
R1506 2.2K 5% R0201
R1507 2.2K 5% R0201
I2C3_SCL_M0_MIPI
I2C3_SDA_M0_MIPI

VCC_1V8_S0
R1501 2.2K 5% R0201
R1502 2.2K 5% R0201
I2C7_SCL_M0_CODEC
I2C7_SDA_M0_CODEC

RK3588_H(VCCIO3 Domain)

VCC_1V8_S0
R95029 10K R0402 I2C4_SDA
VCC_1V8_S0
R95030 10K R0402 I2C4_SCL

U1000H

VCCIO3 Domain

Operating Voltage=1.8V

	UART6_RX_M0	FSPI_D0_M1	SDIO_D0_M0	GMAC0_RXD2	GPIO2_A6_u
	UART6_TX_M0	FSPI_D1_M1	SDIO_D1_M0	GMAC0_RXD3	GPIO2_A7_u
I2C8_SCL_M1	UART6_RTSN_M0	FSPI_D2_M1	SDIO_D2_M0	GMAC0_RXCLK	GPIO2_B0_u
I2C8_SDA_M1	UART6_CTSN_M0	FSPI_D3_M1	SDIO_D3_M0	GMAC0_RXD2	GPIO2_B1_u
I2C3_SCL_M3			SDIO_CMD_M0	GMAC0_TXD3	GPIO2_B2_u
I2C3_SDA_M3		FSPI_CLK_M1	SDIO_CLK_M0	GMAC0_TXCLK	GPIO2_B3_d
I2C4_SDA_M1	UART7_RX_M0	FSPI_CSON_M1	HDMI_TX1_SDA_M0	GMAC0_PTP_REFCLK	GPIO2_B4_u
I2C4_SCL_M1	UART7_TX_M0	FSPI_CS1N_M1	HDMI_TX1_SCL_M0	GMAC0_PPSTRIG	GPIO2_B5_u
I2C5_SCL_M4	UART1_RX_M0		I2S2_MCLK_M0	GMAC0_TXD0	GPIO2_B6_d
I2C5_SDA_M4	UART1_TX_M0		I2S2_SCLK_M0	GMAC0_TXD1	GPIO2_B7_d
I2C2_SDA_M1	UART1_RTSN_M0	SPI1_CLK_M0	I2S2_LRCK_M0	GMAC0_TXEN	GPIO2_C0_d
I2C2_SCL_M1	UART1_CTSN_M0	SPI1_MISO_M0		GMAC0_RXD0	GPIO2_C1_d
I2C6_SDA_M2	UART9_TX_M0	SPI1_MOSI_M0		GMAC0_RXD1	GPIO2_C2_d
I2C6_SCL_M2		SPI1_CS0_M0	I2S2_SDI_M0	ETH0_REFCLKO_25M	GPIO2_C3_d
TEST_CLKOUT_M1	UART9_RX_M0	SPI1_CS1_M0	HDMI_TX1_CEC_M0	GMAC0_PPSCLK	GPIO2_C4_d
				CLK32K_OUT1	GPIO2_C5_d
	UART7_RTSN_M0	SPI3_CS0_M0	PWM2_M2	GMAC0_RXDV_CRS	GPIO4_C2_d
I2C7_SCL_M1	PWM4_M1	SPI3_CS1_M0	I2S2_SDO_M0	GMAC0_MCLKINOUT	GPIO4_C3_d
I2C7_SDA_M1	UART9_RTSN_M0	SPI3_MISO_M0	PWM5_M2	GMAC0_MDC	GPIO4_C4_d
I2C0_SCL_M1	UART9_CTSN_M0	SPI3_MOSI_M0	PWM6_M2	GMAC0_MDIO	GPIO4_C5_d
I2C0_SDA_M1	UART7_CTSN_M0	SPI3_CLK_M0	PWM7_IR_M3	GMAC0_TXER	GPIO4_C6_d

AC32 SDIO-D0-M0
AC31 SDIO-D1-M0

AE32 SDIO-D2-M0
AC33 SDIO-D3-M0
AC34 SDIO-CMD-M0
AE33 SDIO-CLK-M0

AB31 I2C4_SDA
AB30 I2C4_SCL

AD33 TYPEC5V_PWREN_H
AD34 I2S2_SCLK_M0_BT

AE34 I2S2_LRCK_M0_BT
AD32 LCD_RESET
AD31 LCD_light_EN
AD30 I2S2_SDI_M0_BT
AC30 HDMITX1_CEC_M2
AE30 R119 NC R0402 5% fe1_reset

AE31 LCD_PWM
AF34 I2S2_SDO_M0_BT
AB34 GPIO4-C4
AB33 GPIO4-C5
AF33 GPIO4-C6

VCCIO3_1V8 Y26 VCC_1V8_S0

C1503 100nF X5R 6.3V C0201

RK3588-Socket

C0402 VCC_1V8_S0
C90407 100nF GND

U90081 UM3204

[26] I2C4_SDA	B2 VCCA	VCCB A2	I2C4_SDA-3V3 [26]
[26] I2C4_SCL	A3 B3	A1 B1	I2C4_SCL-3V3 [26]
[26] GPIO4-C5	B3 A2	B2 C1	GPIO4-C5/ [26]
[26] GPIO4-C6	C3 A3	B3 D1	GPIO4-C6/ [26]
	D3 A4	B4	
GND D2	GND OE	C2 VCCA_1V8_S0	

VCC_3V3_S0

RK3588_U(SARADC/OTP)

U1000U

SARADC
12-bit 1MS/s

SARADC_IN0_BOOT Recovery/	AM16	BOOT_SARADC_IN0
SARADC_IN1	AL16	SARADC_VIN1_KEY/RECOVERY
SARADC_IN2	AK16	SARADC_VIN2_LCD_ID
SARADC_IN3	AN17	SARADC_VIN3_HP_HOOK
SARADC_IN4	AM17	SARADC_VIN7_EVB_HW_ID
SARADC_IN5	AK15	
SARADC_IN6	AL17	SARADC_VIN6_dcin
SARADC_IN7	AK17	

R95027 210K R0402 1%
R1500 210K R0402 1% VCCA_1V8_S0

C1510 1nF C0402 X5R 50V
C1511 1nF C0402 X5R 50V
C1512 1nF C0402 X5R 50V
C1513 1nF C0402 X5R 50V

SARADC_AVDD_1V8 AH18 VCCA_1V8_S0

C1501 100nF X5R 6.3V C0201

SARADC_IN4

OTP

NC AD4

SARADC_VIN1_KEY/RECOVERY

OTP_VDDOTP_0V75 AD3 VDD_0V75_S0

C1505 100nF X5R 6.3V C0201

KEY

TSADC

TSADC_TEST_OUT_TS AF18

BOOT_SARADC_IN0 J9510

SW9208 TS018B TS018B

BOOT_SARADC_IN0
SARADC_VIN1_KEY/RECOVERY
SARADC_VIN3_HP_HOOK
SARADC_VIN7_LCD_ID0
SARADC_VIN2_LCD_ID1

RK3588-Socket

BOOT MODE CONFIG

VCCA_1V8_S0
R1511 100K 1% R0402
BOOT_SARADC_IN0
R1509 DNP R0402

TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

VCCA_1V8_S0
R1508 NC R0402
SARADC_VIN5_HW_ID
R1510 100K 1% R0402

TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	A
LEVEL2	100K	20K	682	0.3V	B
LEVEL3	100K	51K	1365	0.6V	C
LEVEL4	100K	100K	2047	0.9V	D
LEVEL5	100K	200K	2730	1.2V	E
LEVEL6	100K	499K	3412	1.5V	F
LEVEL7	100K	DNP	4095	1.8V	H

radxa

Size	Title:	REV
A3	ROCK 5B	1.1
	Page Name: 15.RK3588_SARADC/1.8V Only GPIO	
Date: Wednesday, June 29, 2022	Sheet 15 of 33	

RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	AN26	MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	AP26	MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	AN24	MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	AP24	MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	AN25	MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	AP25	MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	AN27	MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	AP27	MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P/NO_USE	AN28	MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	AP28	MIPI_DPHY0_TX_D3N

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	AN32	MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	AP31	MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	AN29	MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	AP29	MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	AN30	MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AP30	MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AN33	MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	AP32	MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P/NO_USE	AN34	MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AP33	MIPI_DPHY0_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG	AF20	C1600 2.2nF X7R 6.3V C0201	
MIPI_D/C_PHY0_VDD	AG20	C1602 100nF X5R 6.3V C0201; C1601 1uF X5R 6.3V C0201	VDD_0V75_S0
MIPI_D/C_PHY0_VDD_1V2	AH20	C1603 1uF X5R 6.3V C0201	VDDA_1V2_S0
MIPI_D/C_PHY0_VDD_1V8	AJ20	C1605 100nF X5R 10V C0201	VCC_1V8_S0

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

RK3588-Socket

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	AN20	MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	AP20	MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	AN18	MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	AP18	MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	AN19	MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	AP19	MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	AN21	MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	AP21	MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P/NO_USE	AN22	MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	AP22	MIPI_DPHY1_TX_D3N

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	AK20	MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	AL20	MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	AK18	MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	AL18	MIPI_DPHY1_RX_D0N
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	AK19	MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	AL19	MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	AK21	MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	AL21	MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_D3P/NO_USE	AK22	MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	AL22	MIPI_DPHY1_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG	AF19	C1608 2.2nF X7R 6.3V C0201	
MIPI_D/C_PHY1_VDD	AG19	C1609 1uF X5R 6.3V C0201	VDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2	AH19	C1611 100nF X5R 6.3V C0201	VDDA_1V2_S0
MIPI_D/C_PHY1_VDD_1V8	AJ19	C1613 1uF X5R 6.3V C0201	VCC_1V8_S0

RK3588-Socket

Note:
These Caps should be placed under the U1000 package.

RK3588_P(MIPI_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N	AJ33/AJ34	MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P/MIPI_CSI0_D0N	AG33/AG34	MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P/MIPI_CSI0_D1N	AH33/AH34	MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N	AM33/AM34	MIPI_CSI0_RX_CLK1P/MIPI_CSI0_RX_CLK1N
MIPI_CSI0_D2P/MIPI_CSI0_D2N	AK33/AK34	MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P/MIPI_CSI0_D3N	AL33/AL34	MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N
MIPI_CSI0_AVCC0V75	AB25	VDD_0V75_S0 (C1616 100nF X5R 6.3V C0201; C1615 1uF X5R 6.3V C0201)
MIPI_CSI0_AVCC1V8	AB26	VCC_1V8_S0 (C1617 1uF X5R 6.3V C0201)

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N	AJ31/AJ32	MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N
MIPI_CSI1_D0P/MIPI_CSI1_D0N	AG31/AG32	MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N
MIPI_CSI1_D1P/MIPI_CSI1_D1N	AH31/AH32	MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N	AM31/AM32	MIPI_CSI1_RX_CLK1P/MIPI_CSI1_RX_CLK1N
MIPI_CSI1_D2P/MIPI_CSI1_D2N	AK31/AK32	MIPI_CSI1_RX_D2P/MIPI_CSI1_RX_D2N
MIPI_CSI1_D3P/MIPI_CSI1_D3N	AL31/AL32	MIPI_CSI1_RX_D3P/MIPI_CSI1_RX_D3N
MIPI_CSI1_AVCC0V75	AA25	VDD_0V75_S0 (C1619 1uF X5R 6.3V C0201)
MIPI_CSI1_AVCC1V8	AA26	VCC_1V8_S0 (C1621 100nF X5R 6.3V C0201)

RK3588-Socket

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

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RK3588_S(HDMI2.1 TX)

U1000S

HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_SBDP/EDP_TX0_AUXP
HDMI_TX0_SBDN/EDP_TX0_AUXN
HDMI_TX0_D0P/EDP_TX0_D0P
HDMI_TX0_D0N/EDP_TX0_D0N
HDMI_TX0_D1P/EDP_TX0_D1P
HDMI_TX0_D1N/EDP_TX0_D1N
HDMI_TX0_D2P/EDP_TX0_D2P
HDMI_TX0_D2N/EDP_TX0_D2N
HDMI_TX0_D3P/EDP_TX0_D3P
HDMI_TX0_D3N/EDP_TX0_D3N
HDMI/EDP_TX0_REXT
HDMI/EDP_TX0_VDD_0V75
HDMI/EDP_TX0_AVDD_0V75
HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8

AG2 HDMI0_TX_SBDP/eDP0_TX_AUXP
AG1 HDMI0_TX_SBDN/eDP0_TX_AUXN
AJ2 HDMI0_TX0P_PORT/eDP0_TX_D0P
AJ1 HDMI0_TX0N_PORT/eDP0_TX_D0N
AK3 HDMI0_TX1P_PORT/eDP0_TX_D1P
AK2 HDMI0_TX1N_PORT/eDP0_TX_D1N
AL2 HDMI0_TX2P_PORT/eDP0_TX_D2P
AL1 HDMI0_TX2N_PORT/eDP0_TX_D2N
AH3 HDMI0_TX3P_PORT/eDP0_TX_D3P
AH2 HDMI0_TX3N_PORT/eDP0_TX_D3N
AM2 HDMI_TX0_REXT — R1708 1 2 8.2K R0201 1%
AA9 <260mA — C1715 4.7uF X5R 10V C0402_BGA — C1751 4.7uF X5R 10V C0402 — VDDA_0V75_S0
VDD_IO<77mA
VDD_CMN<71mA
AB9 <1mA — C1714 1uF X5R 6.3V C0201
AC7 AC6 — C1716 1uF X5R 6.3V C0201 — C1717 100nF X5R 6.3V C0201 — C1742 4.7uF X5R 10V C0402 — VCC_1V8_S0

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX1_SBDP/EDP_TX1_AUXP
HDMI_TX1_SBDN/EDP_TX1_AUXN
HDMI_TX1_D0P/EDP_TX1_D0P
HDMI_TX1_D0N/EDP_TX1_D0N
HDMI_TX1_D1P/EDP_TX1_D1P
HDMI_TX1_D1N/EDP_TX1_D1N
HDMI_TX1_D2P/EDP_TX1_D2P
HDMI_TX1_D2N/EDP_TX1_D2N
HDMI_TX1_D3P/EDP_TX1_D3P
HDMI_TX1_D3N/EDP_TX1_D3N
HDMI/EDP_TX1_REXT
HDMI/EDP_TX1_VDD_0V75
HDMI/EDP_TX1_AVDD_0V75
HDMI/EDP_TX1_VDD_IO_1V8
HDMI/EDP_TX1_VDD_CMN_1V8

AN2 HDMI1_TX_SBDP/eDP1_TX_AUXP
AP2 HDMI1_TX_SBDN/eDP1_TX_AUXN
AN4 HDMI1_TX0P_PORT/eDP1_TX_D0P
AP4 HDMI1_TX0N_PORT/eDP1_TX_D0N
AM5 HDMI1_TX1P_PORT/eDP1_TX_D1P
AN5 HDMI1_TX1N_PORT/eDP1_TX_D1N
AN6 HDMI1_TX2P_PORT/eDP1_TX_D2P
AP6 HDMI1_TX2N_PORT/eDP1_TX_D2N
AM3 HDMI1_TX3P_PORT/eDP1_TX_D3P
AN3 HDMI1_TX3N_PORT/eDP1_TX_D3N
AN1 HDMI_TX1_REXT — R1719 1 2 8.2K 1% R0201
AD9 <260mA — C1735 1uF X5R 6.3V C0201 — C1752 100nF X5R 10V C0201 — C1730 4.7uF X5R 10V C0402 — VDDA_0V75_S0
AC9 <1mA — C1729 1uF X5R 6.3V C0201
AD7 AD6 — C1731 1uF X5R 6.3V C0201 — C1732 100nF X5R 6.3V C0201 — C1733 4.7uF X5R 10V C0402 — VCC_1V8_S0

RK3588-Socket

RK3588_T(HDMI20 RX)

U1000T

HDMI RX

HDMI:V2.0

HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D2P
HDMI_RX_D2N
HDMI_RX_CLKP
HDMI_RX_CLKN
HDMI_RX_REXT
HDMI_RX_AVDD0V75
HDMI_RX_VPH3V3
HDMI_RX_DVDD3V3

AG5 HDMI_RX_D0P — HDMI_RX_D0P_PORT
AG4 HDMI_RX_D0N — HDMI_RX_D0N_PORT
AH6 HDMI_RX_D1P — HDMI_RX_D1P_PORT
AH5 HDMI_RX_D1N — HDMI_RX_D1N_PORT
AJ5 HDMI_RX_D2P — HDMI_RX_D2P_PORT
AJ4 HDMI_RX_D2N — HDMI_RX_D2N_PORT
AF6 HDMI_RX_CLKP — HDMI_RX_CLKP_PORT
AF5 HDMI_RX_CLKN — HDMI_RX_CLKN_PORT
AF3 — R1730 1 2 200R R0201 1%
AE8 — C1738 1uF X5R 6.3V C0201 — <40mA — VDDA_0V75_S0
AE4 — C1740 100nF X5R 6.3V C0201 — C1741 1uF X5R 6.3V C0201 — <80mA — VCCA_3V3_S0
AE5

RK3588-Socket

HDMI0_TX_SBDP/eDP0_TX_AUXP ↔ HDMI0_TX_SBDP/eDP0_TX_AUXP
HDMI0_TX_SBDN/eDP0_TX_AUXN ↔ HDMI0_TX_SBDN/eDP0_TX_AUXN
HDMI0_TX0P_PORT/eDP0_TX_D0P ↔ HDMI0_TX0P_PORT/eDP0_TX_D0P
HDMI0_TX0N_PORT/eDP0_TX_D0N ↔ HDMI0_TX0N_PORT/eDP0_TX_D0N
HDMI0_TX1P_PORT/eDP0_TX_D1P ↔ HDMI0_TX1P_PORT/eDP0_TX_D1P
HDMI0_TX1N_PORT/eDP0_TX_D1N ↔ HDMI0_TX1N_PORT/eDP0_TX_D1N
HDMI0_TX2P_PORT/eDP0_TX_D2P ↔ HDMI0_TX2P_PORT/eDP0_TX_D2P
HDMI0_TX2N_PORT/eDP0_TX_D2N ↔ HDMI0_TX2N_PORT/eDP0_TX_D2N
HDMI0_TX3P_PORT/eDP0_TX_D3P ↔ HDMI0_TX3P_PORT/eDP0_TX_D3P
HDMI0_TX3N_PORT/eDP0_TX_D3N ↔ HDMI0_TX3N_PORT/eDP0_TX_D3N

HDMI1_TX_SBDP/eDP1_TX_AUXP ↔ HDMI1_TX_SBDP/eDP1_TX_AUXP
HDMI1_TX_SBDN/eDP1_TX_AUXN ↔ HDMI1_TX_SBDN/eDP1_TX_AUXN
HDMI1_TX0P_PORT/eDP1_TX_D0P ↔ HDMI1_TX0P_PORT/eDP1_TX_D0P
HDMI1_TX0N_PORT/eDP1_TX_D0N ↔ HDMI1_TX0N_PORT/eDP1_TX_D0N
HDMI1_TX1P_PORT/eDP1_TX_D1P ↔ HDMI1_TX1P_PORT/eDP1_TX_D1P
HDMI1_TX1N_PORT/eDP1_TX_D1N ↔ HDMI1_TX1N_PORT/eDP1_TX_D1N
HDMI1_TX2P_PORT/eDP1_TX_D2P ↔ HDMI1_TX2P_PORT/eDP1_TX_D2P
HDMI1_TX2N_PORT/eDP1_TX_D2N ↔ HDMI1_TX2N_PORT/eDP1_TX_D2N
HDMI1_TX3P_PORT/eDP1_TX_D3P ↔ HDMI1_TX3P_PORT/eDP1_TX_D3P
HDMI1_TX3N_PORT/eDP1_TX_D3N ↔ HDMI1_TX3N_PORT/eDP1_TX_D3N

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RK3588_N(PCIE20)

CLK Differential Pair:
100 Ohm± 10 %
DATA Differential Pair:
PCIE20: 85 Ohm ± 10 %
SATA30: 100 Ohm ± 10 %
USB30: 90ohm ± 10 %

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN

L32 L33 → PCIE20_0_REFCLKP PCIE20_0_REFCLKN
M34 M33 → PCIE20_0_TXP PCIE20_0_TXN
N33 N34 → PCIE20_0_RXP PCIE20_0_RXN

PCIE20_SATA30_0_AVDD_0V85 — M28 — C1810 10uF X5R 4V C0402_BGA — VDDA_0V85_S0

PCIE20X1_2-CTL

PCIE20_SATA30_0_AVDD_1V8 — M27 — C1808 1uF X5R 4V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN

H32 H33 → PCIE20_1_REFCLKP PCIE20_1_REFCLKN
K33 K34 → PCIE20_1_TXP PCIE20_1_TXN
J33 J34 → PCIE20_1_RXP PCIE20_1_RXN

PCIE30X1_0-CTL

PCIE20_SATA30_1_AVDD_0V85 — L28 — C1818 100nF X5R 6.3V C0201 — VDDA_0V85_S0

PCIE20_SATA30_1_AVDD_1V8 — L27 — C1816 100nF X5R 6.3V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN

G31 G30 → PCIE20_2_REFCLKP PCIE20_2_REFCLKN
H30 H29 → USB30_2_SSTXP USB30_2_SSTXN
J31 J30 → USB30_2_SSRXP USB30_2_SSRXN

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — C1806 1uF X5R 4V C0201 — VDDA_0V85_S0

PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — C1804 1uF X5R 4V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

For RJ45

RK3588-Socket

PCIE30_PORT0 + PCIE30X4_CTL--- MKEY
PCIE20_0 + PCIEX1_0CTL--- RTL8125B
PCIE20_1 + PCIE20_1_2CTL --- EKEY
PCIE20_2 + XXXCC --- USB3.0

RK3588_O(PCIE30)

Note:
Only PCIE30 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input
PCIE30_PORT0_REF_CLKP
PCIE30_PORT0_REF_CLKN

Lane0
PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N

Lane1
PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N

E33 E34 → PCIE30_PORT0_REFCLKP_IN PCIE30_PORT0_REFCLKN_IN
D32 D33 → PCIE30_PORT0_TX0P PCIE30_PORT0_TX0N
G33 G34 → PCIE30_PORT0_RX0P PCIE30_PORT0_RX0N
C33 C34 → PCIE30_PORT0_TX1P PCIE30_PORT0_TX1N
F32 F33 → PCIE30_PORT0_RX1P PCIE30_PORT0_RX1N

CLK Differential Pair:
100 Ohm ± 10 %
DATA Differential Pair:
PCIE30: 85 Ohm ± 10 %

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1801 1 2 200R 1% R0201

PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
C1802 1uF X5R 6.3V C0201
C1803 4.7uF X5R 10V C0402

PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
C1800 1uF X5R 6.3V C0201
C1801 4.7uF X5R 10V C0402

PCIE30 PORT1

input
PCIE30_PORT1_REF_CLKP
PCIE30_PORT1_REF_CLKN

Lane0
PCIE30_PORT1_TX0P
PCIE30_PORT1_TX0N
PCIE30_PORT1_RX0P
PCIE30_PORT1_RX0N

Lane1
PCIE30_PORT1_TX1P
PCIE30_PORT1_TX1N
PCIE30_PORT1_RX1P
PCIE30_PORT1_RX1N

A28 B28 → PCIE30_PORT1_REFCLKP_IN PCIE30_PORT1_REFCLKN_IN
B30 A30 → PCIE30_PORT1_TX2P PCIE30_PORT1_TX2N
B32 A32 → PCIE30_PORT1_RX2P PCIE30_PORT1_RX2N
C29 B29 → PCIE30_PORT1_TX3P PCIE30_PORT1_TX3N
C31 B31 → PCIE30_PORT1_RX3P PCIE30_PORT1_RX3N

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1807 1 2 200R 1% R0201

PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
C1814 1uF X5R 6.3V C0201
C1815 4.7uF X5R C0402 10V

PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
C1812 100nF X5R 6.3V C0201
C1813 4.7uF X5R 10V C0402

RK3588-Socket

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

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RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u	AA29 FSPI-D0
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u	AA30 FSPI-D1
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u	AD27 FSPI-D2
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u	AE27 FSPI-D3
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d	AD28 UART8_RTSn_M1_BT
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d	AH30 FSPI-CLK
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d	AH27 BT_REG_ON_H
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u	AG29 PWM8_M0 PWM8_M0 TP6802 TP_2.0
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u	AG28 PCIE_PERST_L
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d	AH29 I2S2_LRCK_RX_M1
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d	AE28 I2S2_SDI_M1
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u	AC28 I2S2_SDO_M1
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u	AC29 CC_INT_L
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u	AD29 I2S2_SCLK_TX_M1
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d	AE29 I2S2_LRCK_TX_M1
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d	AA28 SPI1_MOSI_M1
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d	Y29 SPI1_MISO_M1
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d	Y27 SPI1_CLK_M1
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d	Y31 SPI1_CS0_M1
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d	Y30 SPI1_CS1_M1
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u	AH26 FSPI-CS0
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u	AH25 HDMITX1_SDA_M1
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u	AG26 HDMITX1_SCL_M1
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u	AJ24 PCIE20_1_2_CLKREQn_M1_L
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u	AH24 PCIE20_1_2_WAKEn_M1_L
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d	AG23 HDMI_RX_CEC
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d	AG25 HDMI_RX_SCL_M1
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d	AG24 HDMI_RX_SDA_M1
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d	AA27 HDMIIRX_HPDOUT_H
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d	AB28 BT_WAKE_L

VCCIO5_1V8 — W25 — C1903 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO5 — W26 — C1902 100nF X5R 6.3V C0201 — VCC_3V3_S0

RK3588-Socket

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1			I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1				I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2				PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2			PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3		I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3		I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3		I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1			I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1			HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1		HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI3_CLK_M1		I2C5_SDA_M1		HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3		HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3		HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

VCC_3V3_S0

R95032 2.2K 5% R0201 — R95033 2.2K 5% R0201 — I2C7_SCL_M3, I2C7_SDA_M3

AK30 CM_RST_L
AL30 HDMI1_TX_ON_H
AM29 W-DISABLE
AL29 PCIE30x1_0_CLKREQn_M1_L
AL28 PCIE30x1_0_WAKEn_M1_L
AK27 PCIE30x1_0_PERSTn_M1_L
AL27 TYPEC0_SBU1_DC
AM27 TYPEC0_SBU2_DC
AK26 USB_HOST_PWREN_H
AL24 HDMI0_TX_ON_H
AK25 I2C7_SCL_M3
AM25 I2C7_SDA_M3
AL26 PCIE30X4_CLKREQn_M1_L
AJ26 PCIE30X4_WAKEn_M1_L
AJ27 PCIE30X4_PERSTn_M1_L
AJ28 HDMITX0_SCL_M0
AJ25 HDMITX0_SDA_M0
AK24 HDMITX0_CEC_M0

VCCIO6_1V8 — AC25 — C1909 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO6 — AC26 — C1908 100nF X5R 6.3V C0201 — VCC_3V3_S0

RK3588-Socket

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d	A24 UART6-RX
SATA1_ACT_LED_M1		SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d	A25 UART6-TX
	PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY		I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d	A26 UART6-RTSN
	PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2		I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d	A27 UART6-CTSN
		SPI2_MISO_M0		HDMI_TX1_SCL_M2				GPIO1_A4_d	B25 PCIE30x4_PWREN_H
		SPI2_MOSI_M0		HDMI_TX0_HPD_M0				GPIO1_A5_d	B26 HDMITX0_HPDIN_M1
		SPI2_CLK_M0		HDMI_TX1_HPD_M0				GPIO1_A6_d	C24 HDMITX1_HPDIN_M1
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2			PDM1_SDI0_M1		GPIO1_A7_u	C25 MIPI_CSI0_PDN1_H
		SPI2_CS1_M0	PCIE30X4_CLKREQN_M3			PDM1_SDI1_M1		GPIO1_B0_u	C27 MIPI_CSI0_PDN0_H
		SPI0_MISO_M2	PCIE30X4_WAKEN_M3			PDM1_SDI2_M1		GPIO1_B1_d	D25 SPI0-MISO
		SPI0_MOSI_M2	PCIE30X4_PERSTN_M3			PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d	D26 SPI0-MOSI
SATA0_ACT_LED_M1		SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2			PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d	D27 SPI0-CLK
		SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2			PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u	E24 SPI0-CS0
		SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2				UART7_TX_M2	GPIO1_B5_u	E25 SPI0-CS1
	HDMI_RX_HPDOUT_M2	SPDIF0_TX_M3	PCIE30X2_WAKEN_M3		MIPI_CAMERA1_CLK_M3	I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u	E26 MIPI_CAM1_CLKOUT
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM3_M2	SPDIF1_TX_M3	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M3	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u	E27 GPIO1_B7_U_1V8
	HDMI_RX_SCL_M2	PWM14_M2			MIPI_CAMERA3_CLK_M3	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u	F24 MIPI_CAM3_CLKOUT
	HDMI_RX_SDA_M2	PWM15_IR_M3	PCIE30X2_CLKREQN_M3		MIPI_CAMERA4_CLK_M3	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u	F25 GPIO1-D7

VCCIO4_1V8 — H20 — C1907 100nF X5R 6.3V C0201 — VCC_1V8_S0

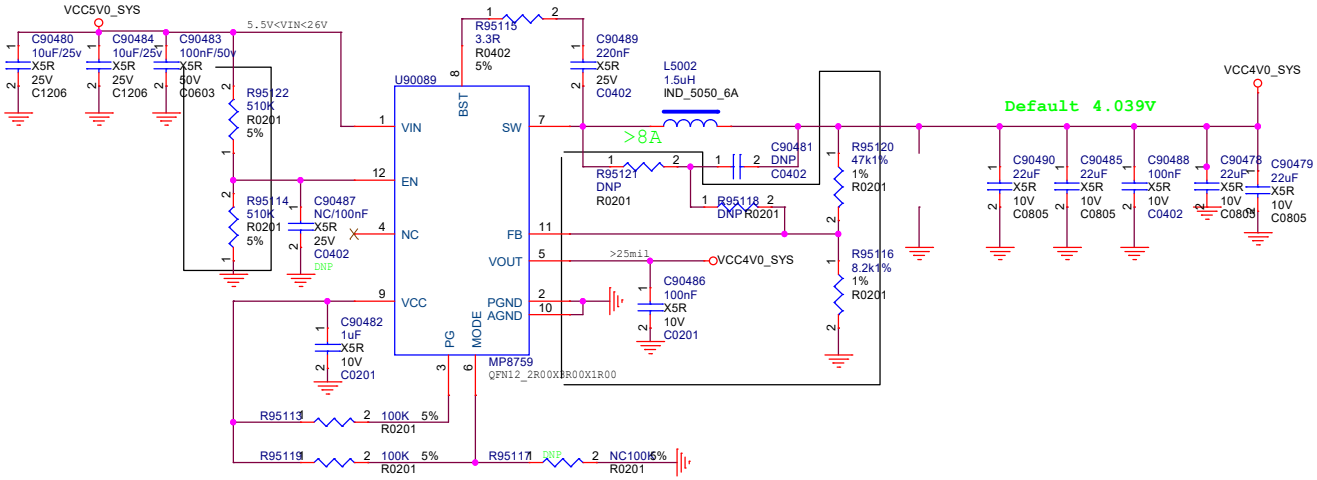
VCCIO4 — H21

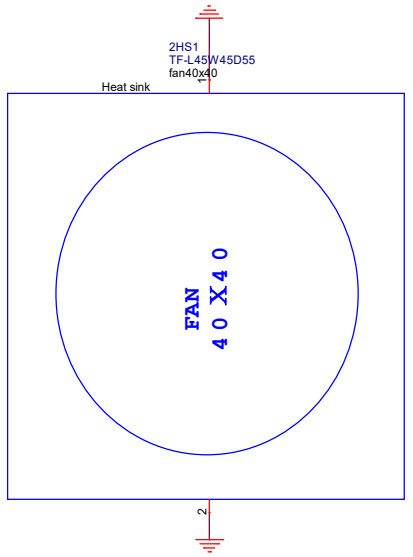
RK3588-Socket

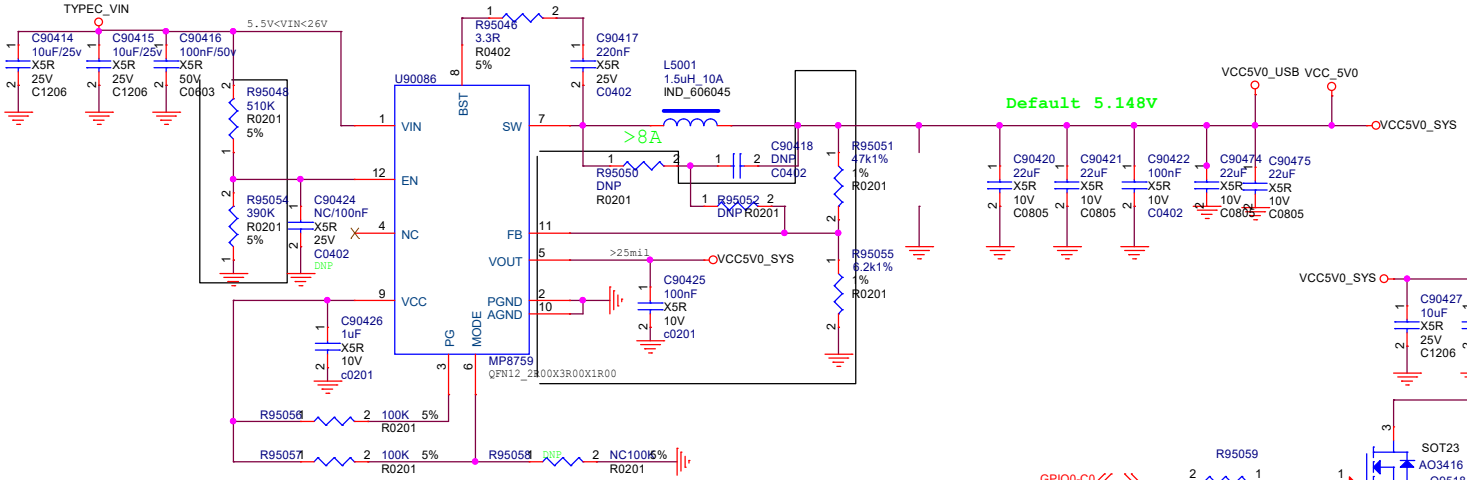
radxa

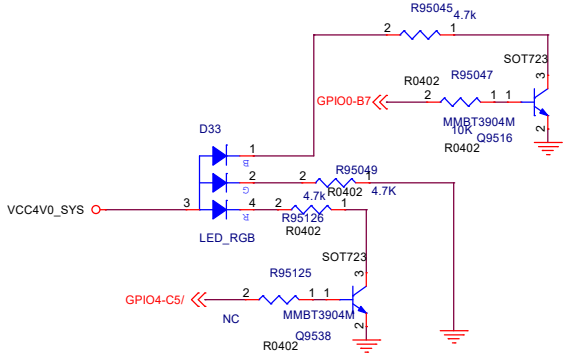
Size	Title:	ROCK 5B	REV
A2	Page Name:	19.RK3588_1.8V/ 3.3V GPIO	1.1
Date:	Wednesday, June 29, 2022	Sheet 19 of 33	

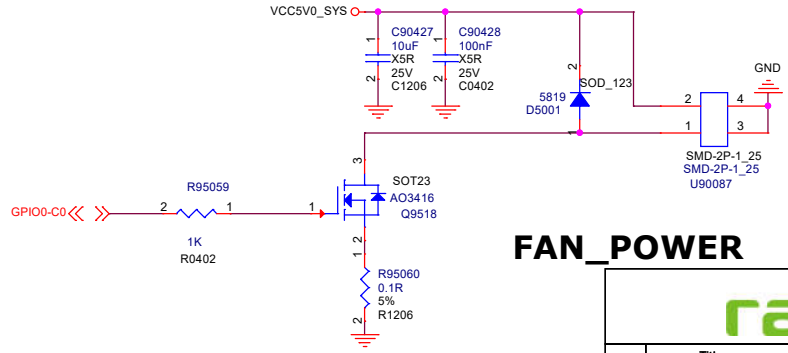
TYPEC-IN ----> MP8759 DCDC 5.148V ----> USB
----> ~~VCC5V0~~ -> MP8759 DCDC 4.039V ----> PMU
----> 40PIN







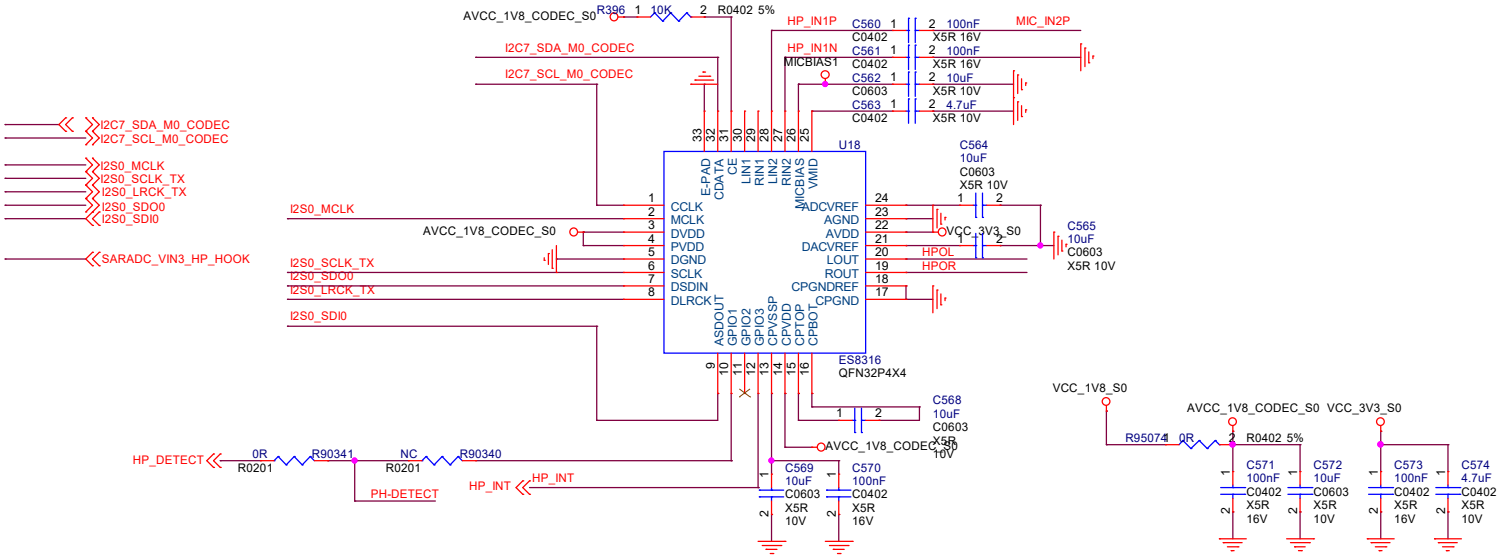


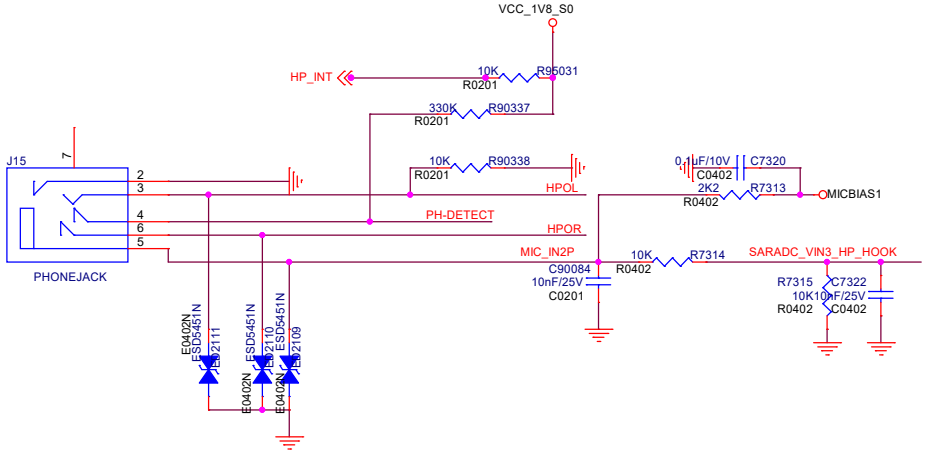


FAN_POWER

Size: A3	Title: ROCK 5B	REV: 1.1
	Page Name: 20.Power_DC IN	
Date: Wednesday, June 29, 2022	Sheet 20 of 33	

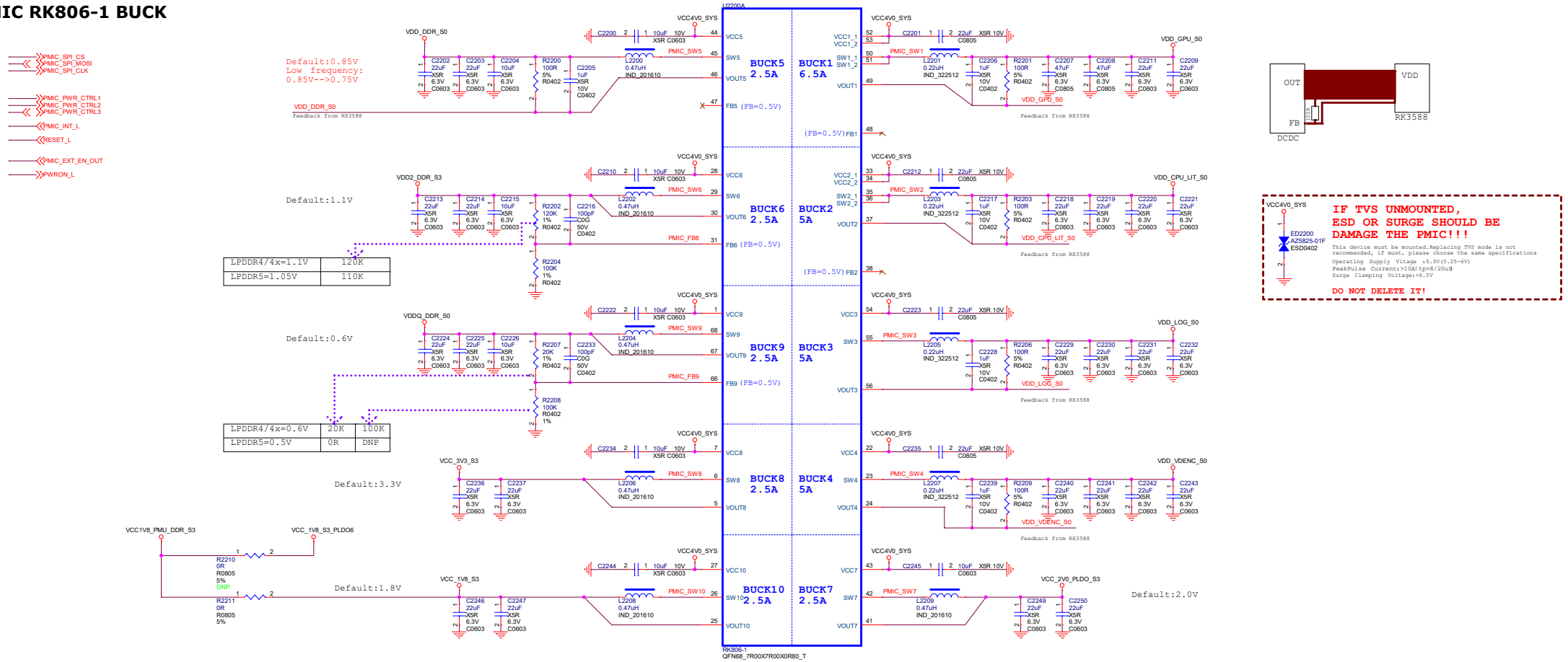
CODEC ES8316



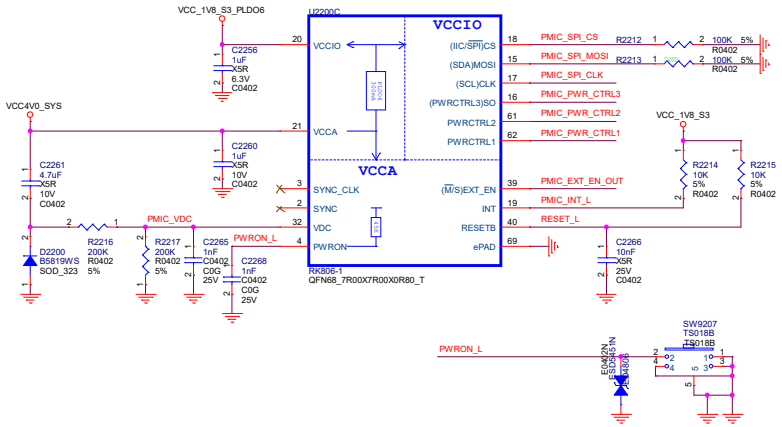


Size	Title: ROCK 5B	REV
A3	Page Name: 21.Audio Codec-ES8316	1.1
Date: Wednesday, June 29, 2022	Sheet 21 of 33	

PMIC RK806-1 BUCK



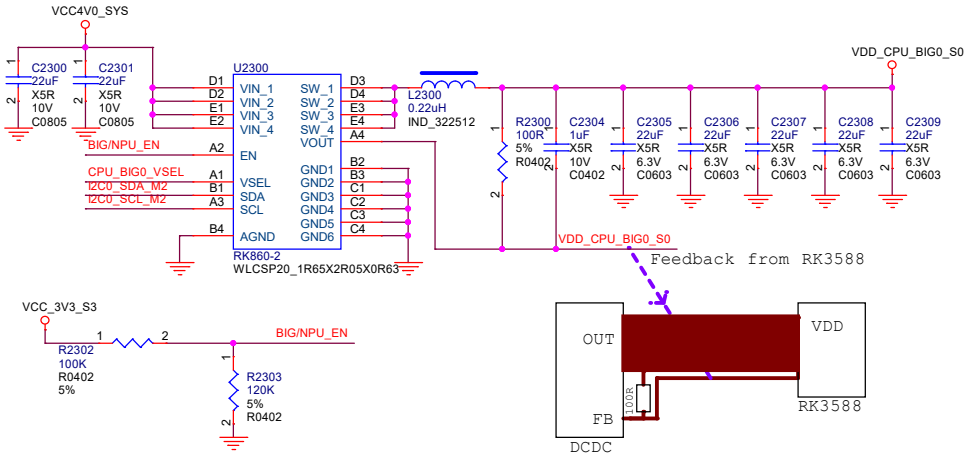
PMIC RK806-1 Managerment



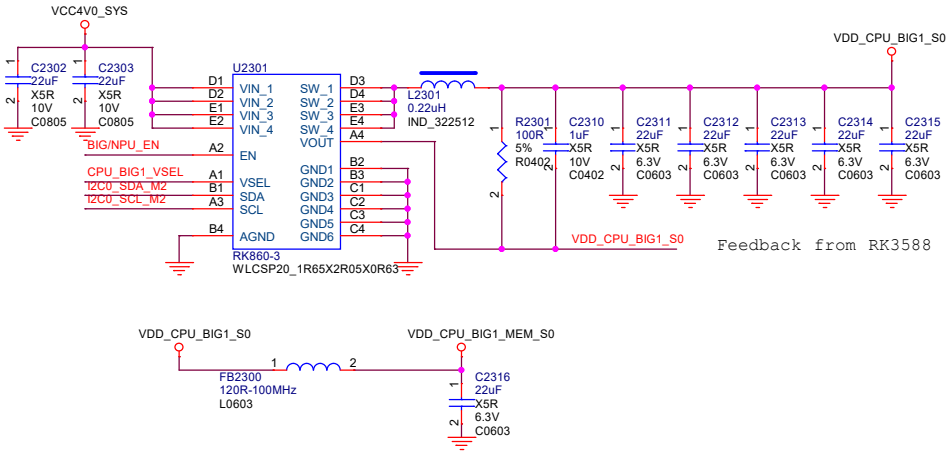
PMIC RK806-1 LDO

Size	Title: ROCK 5B		REV
A2	Page Name: 22.Power-PMIC_RK806-1		1.1
Date: Wednesday, June 29, 2022	Sheet 22 of 33		

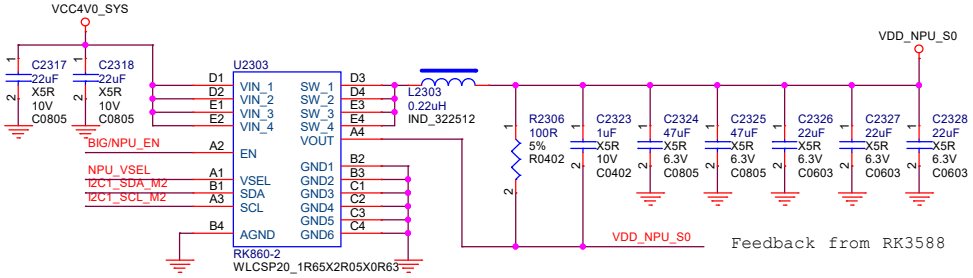
VDD_CPU_BIG0



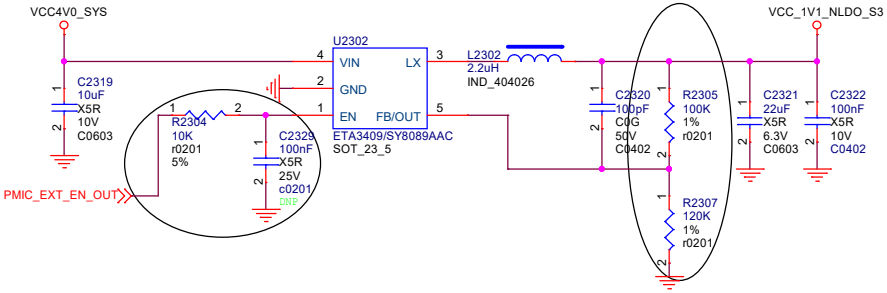
VDD_CPU_BIG1

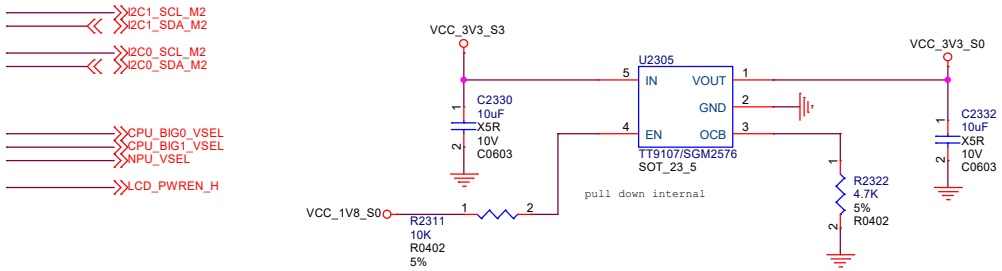


VDD_NPU



VCC_1V1_NLDO_S3





Size	Title: ROCK 5B		REV
A3	Page Name: 23.Power_Ext Discrete		1.1
Date: Wednesday, June 29, 2022	Sheet 23 of 33		

RTL8125B(S)_BG 0.95V
RTL8111K 1.0V

LAN_EXT_CORE

PCIE2.0 DATA Impedance 85R

PCIE2.0 CLK Impedance 100R

R9 and R59 for RTL8125B(S)_BG only

For RTL8125B(S)_BG
* Place C3, C4 2.2uF close to AVDD33 pin -- 19, 33
For RTL8111K
* Place C2 0.1uF close to AVDD33 pin -- 19
* Place C4 4.7uF close to AVDD33 pin -- 19

For RTL8125B(S)_BG
L6 =33ohm Bead
For RTL8111K
L6=0R,C51=NC

20191112
R86 stuff bead

For RTL8125B(S)_BG
* Place C14 to C15 close to DVDD33 pin -- 29, 46
For RTL8111K
* Place C14 close to DVDD33 pin -- 29
* Leave C15 NC

20191112
Add C75 C76

Reserved

RTL8111K 1.0V source @ SWR mode

RTL8125BS 0.95V source

For RTL8111K:
STUFF 0.1uF,UNSTUFF 4.7uF

For RTL8125B(S)_BG Only
* Place C25 close to AVDD33_XTAL pin -- 34

For RTL8125B(S)_BG
* Place C6 to C8 2.2uF close to AVDD09 pin -- 11, 16, 22
For RTL8111K
* Place C6 to C8 0.1uF close to AVDD10 pin -- 11, 16, 22

For RTL8125B(S)
* Place C12 1uF to C13 close to EVDD09 pin -- 37
For RTL8115K
* Place C12 0.1uF to C13 close to EVDD10 pin -- 37

20191112
C913 Unstuff

20191112
C916 stuff 1uF

NC for RTL8111K

For RTL8125B(S)_BG
* Leave R2 NC and connect R3
* Place C17 1uF close to EVDD33 pin -- 43
For RTL8111K
* Leave R3 NC and connect R2
* Place C17 0.1uF close to DVDD10 pin -- 43

For RTL8125B(S)_BG
* Place C9 to C10 10uF close to DVDD09 pin -- 8, 28
* Place C11 2.2uF close to DVDD09 pin -- 47
For RTL8111K
* Place C9 0.1uF close to DVDD10 pin -- 8
* Leave C10 to C11 NC

For RTL8111K only
* Place C16 close to DVDD10 pin -- 40

20191112
C911 Unstuff

For RTL8125B(S)_BG
* Leave R17 to R18 NC
For RTL8125BS
* R17 for Enable SWR
* R18 for Disable SWR
For RTL8111K
* R17 for SWR mode
* R18 for LDO mode

Reserved

RTL8111K 1.0V source @ LDO mode

RTL8125BS leave R4 and C22 NC

RTL8111K 1.0V source @ SWR mode

RTL8125BS 0.95V source

Remove when NOT using switching regulator

VDD09/VDD10

LAN_EXT_CORE

RTL8125B(S)
RTL8125BG
(RTL8111K)

RTL8125B(S)_BG Only
R29 PU for normal application

For RTL8125B(S)_BG & RTL8111K
*. R26 is needed for ensuring IC latch to normal operation mode.

for External Clock Source

EEPROM Option

For RTL8125B(S)_BG & RTL8111K

TWSI
EEPROM

93C56/66
93C46

For RTL8125B(S)_BG
* R48 for TWSI
R49 for EEROM
For RTL8111K
* Connect R49 and leave R48 NC

Noise Isolation

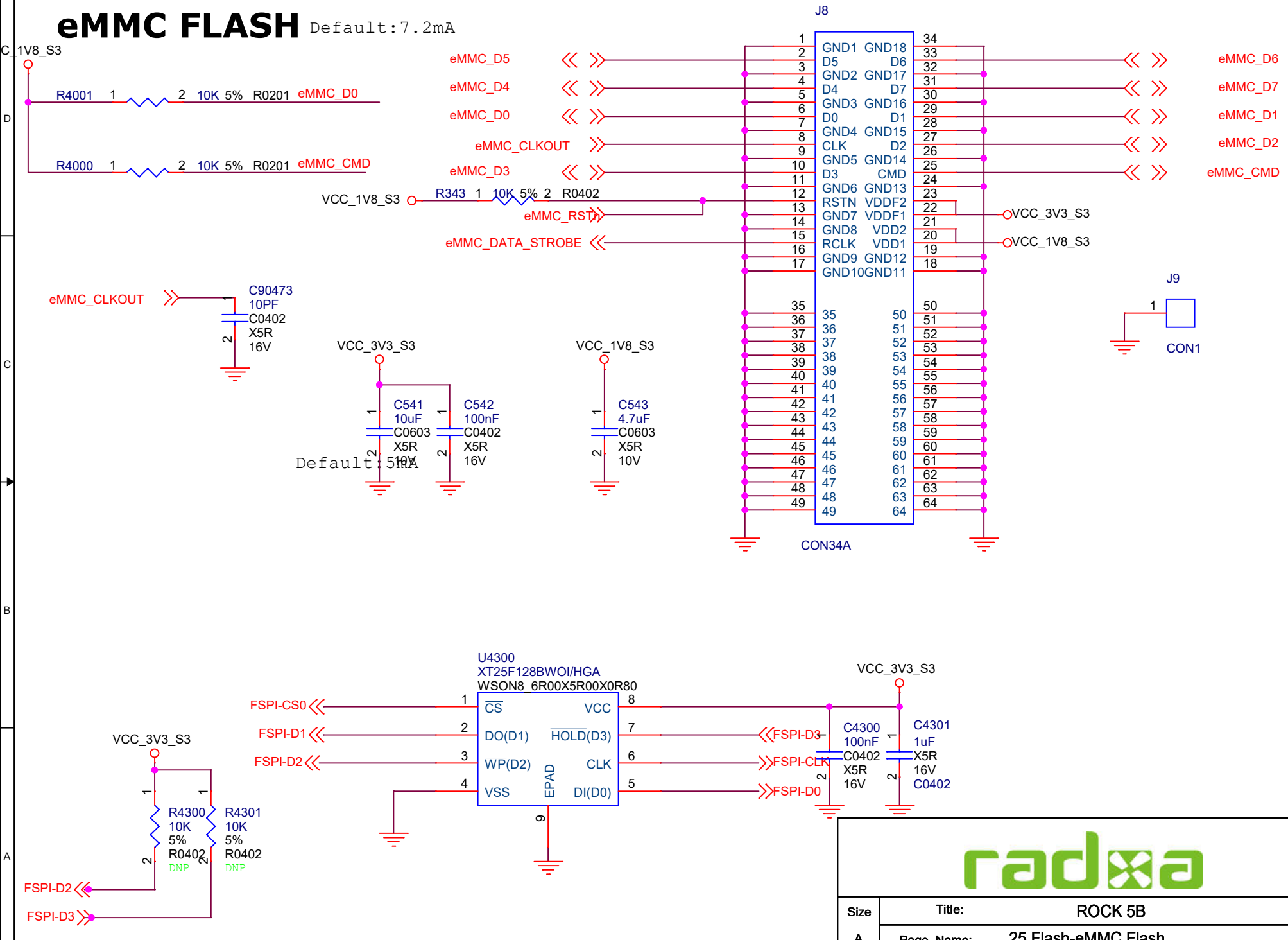
Clock Source

must be use SMD type XTAL for RTL8125B(S)

For RTL8125B(S)_BG
* R27 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R25 on CKXTAL1 patch.
For RTL8111K
* R25 is based on the XTAL drive level spec to choose the appropriate resistor. Do not cascade R27 on CKXTAL2 patch.

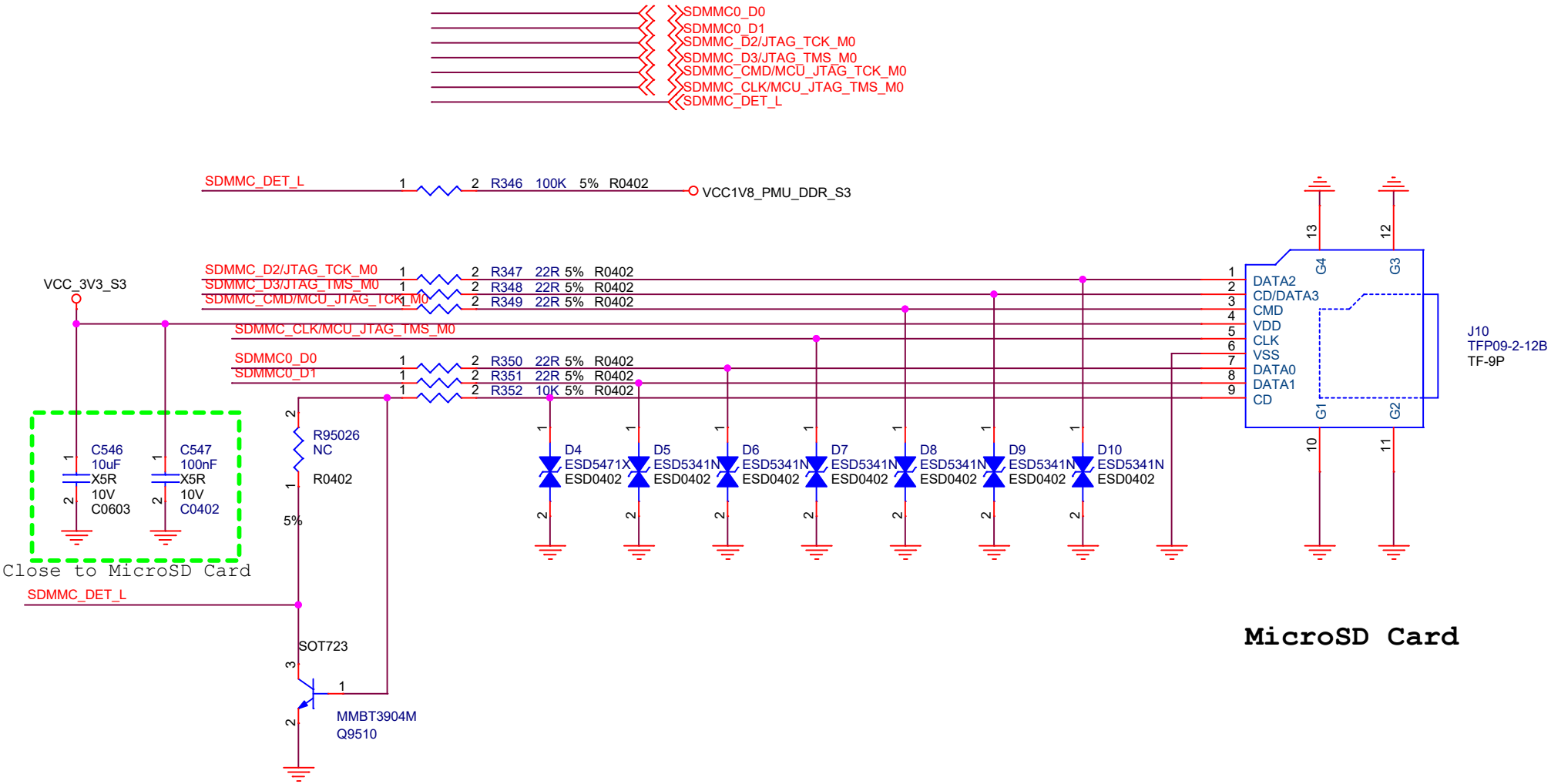
Size	Title: ROCK 5B		REV
Custom	Page Name: 24.PCIE TO RJ45_RTL8125B		1.1
Date: Wednesday, June 29, 2022	Sheet 24 of 33		

eMMC FLASH Default:7.2mA



Size	Title: ROCK 5B	REV
A	Page Name: 25.Flash-eMMC Flash	1.1
Date: Wednesday, June 29, 2022	Sheet 25 of 33	

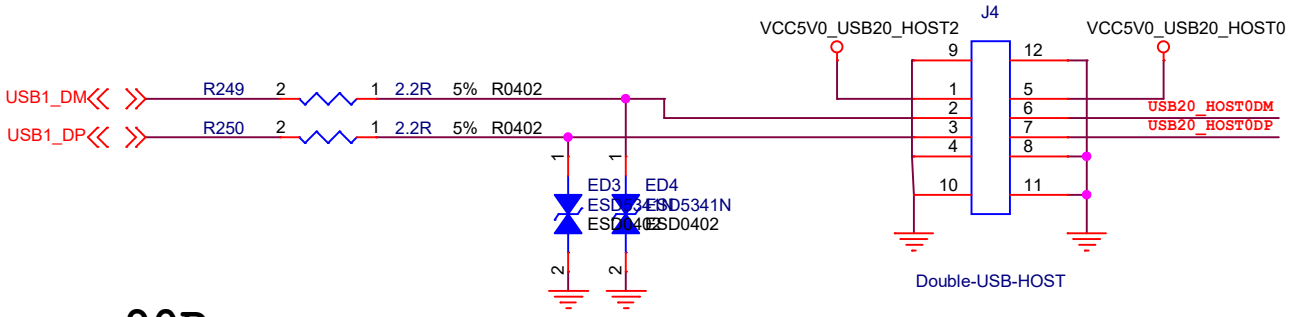
TF CARD



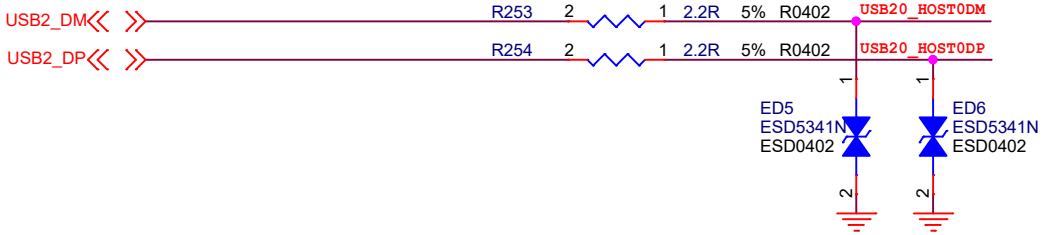
Size	Title:	ROCK 5B	REV
A4	Page Name:	26.TF Card	1.1
Date:	Wednesday, June 29, 2022	Sheet 26 of 33	

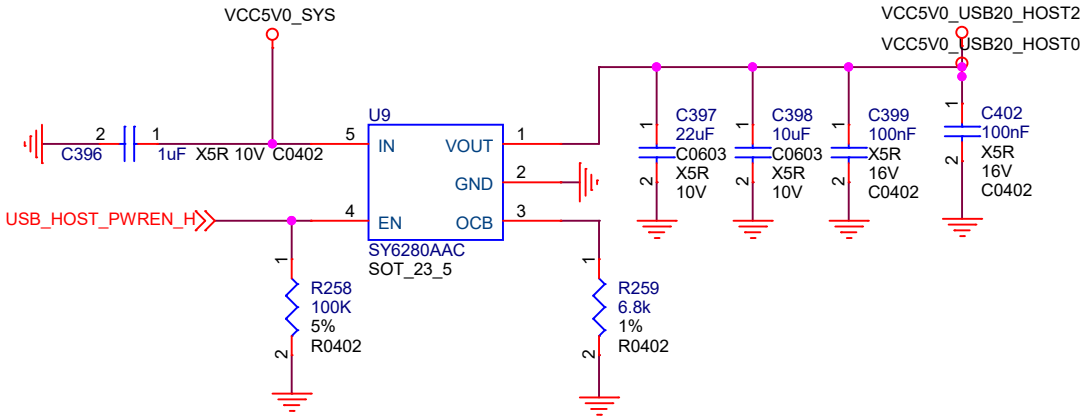
Rockchip Confidential

USB2.0



USB Impedance 90R

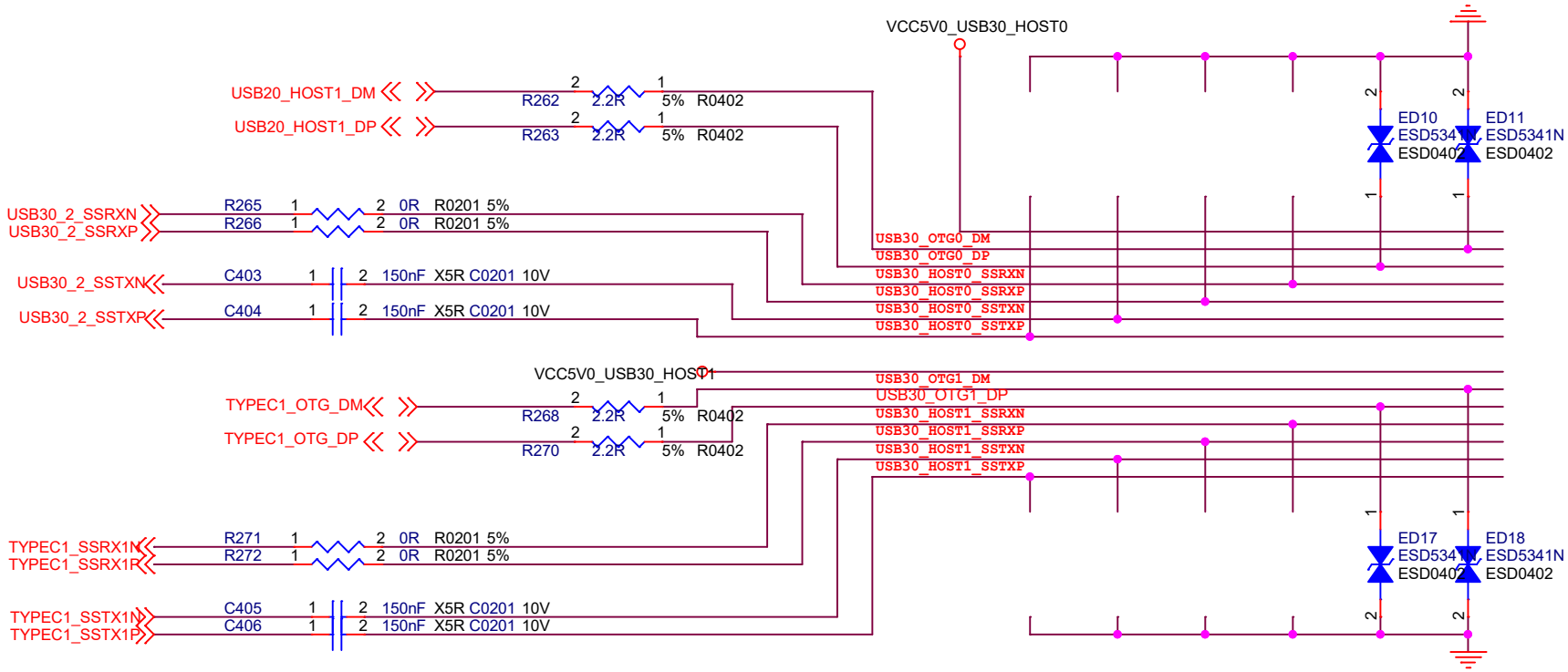


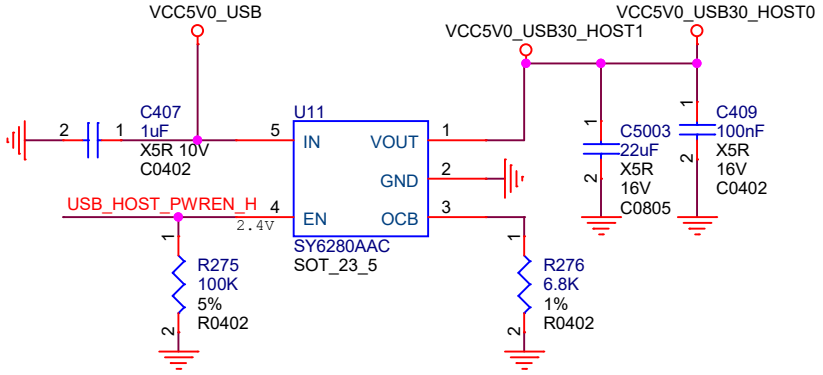


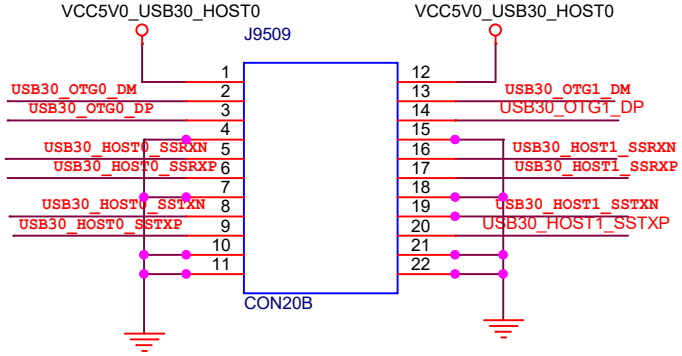
Ilim(A)=6800/Rset(ohm)

Size	Title:	ROCK 5B	REV
A4	Page Name:	27.USB20x2 Double Port	1.1
Date:	Wednesday, June 29, 2022	Sheet 27 of 33	

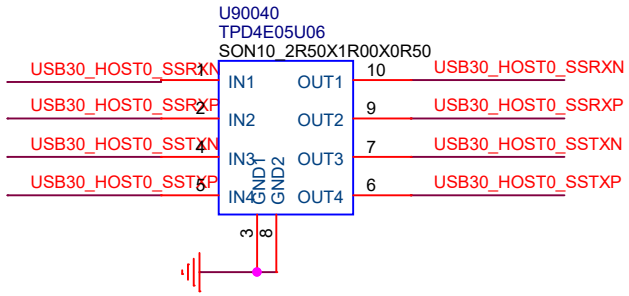
USB3.0 HOST PORT

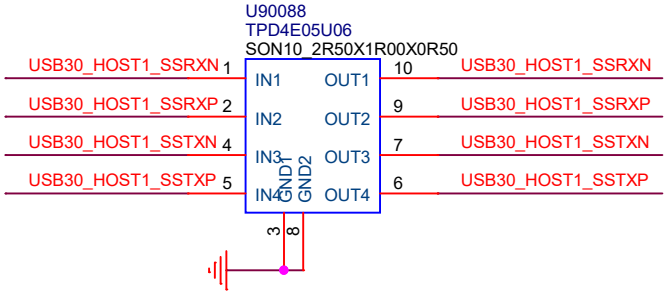






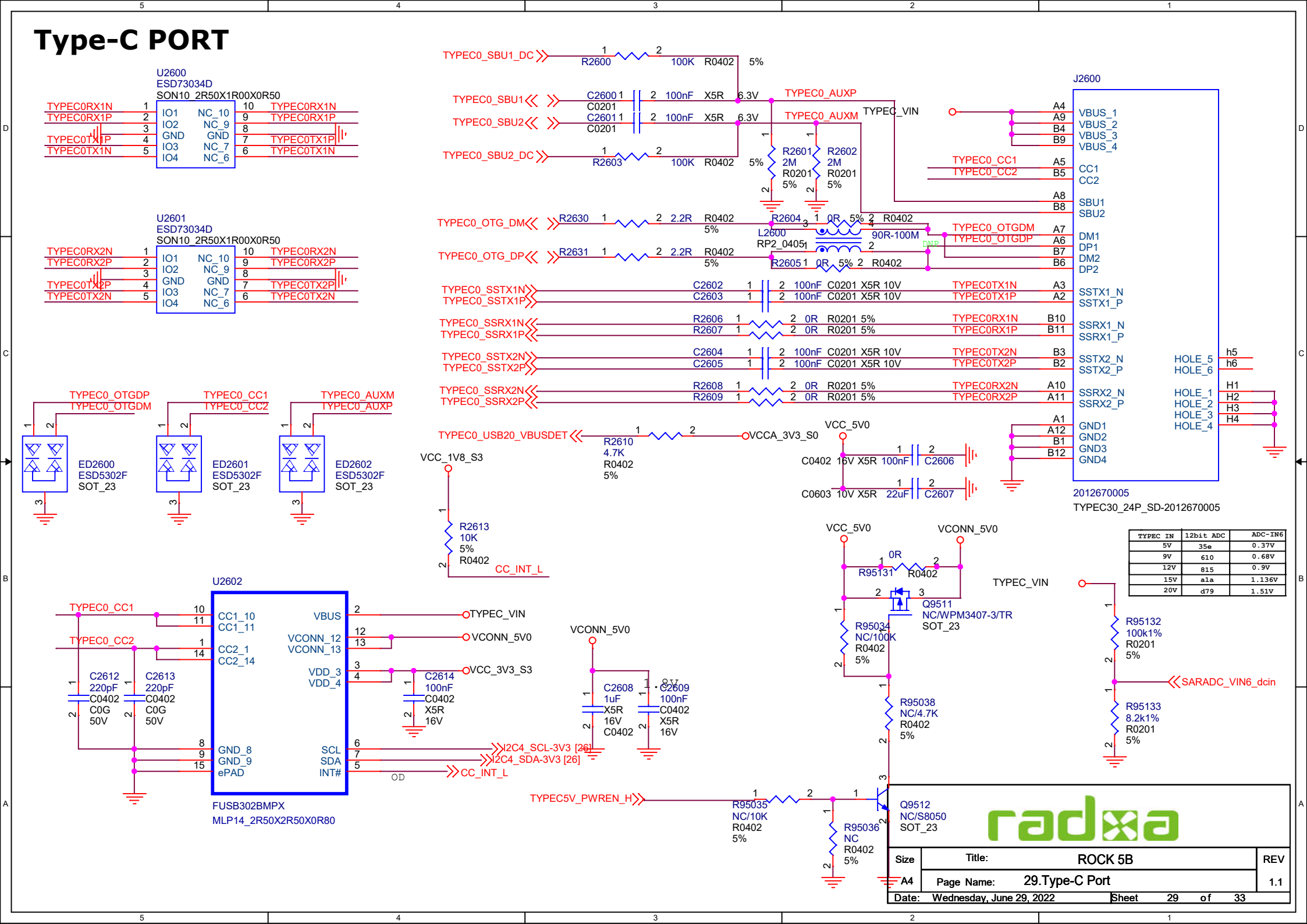
USB Impedance 90R





Size	Title:	ROCK 5B	REV
A4	Page Name:	28.USB30x2 Double Port	1.1
Date:	Wednesday, June 29, 2022	Sheet 28 of 33	

Type-C PORT



TYPEC IN	12bit ADC	ADC-IN6
5V	35e	0.37V
9V	610	0.68V
12V	815	0.9V
15V	a1a	1.136V
20V	d79	1.51V

Size: A4	Title: ROCK 5B	REV: 1.1
	Page Name: 29.Type-C Port	
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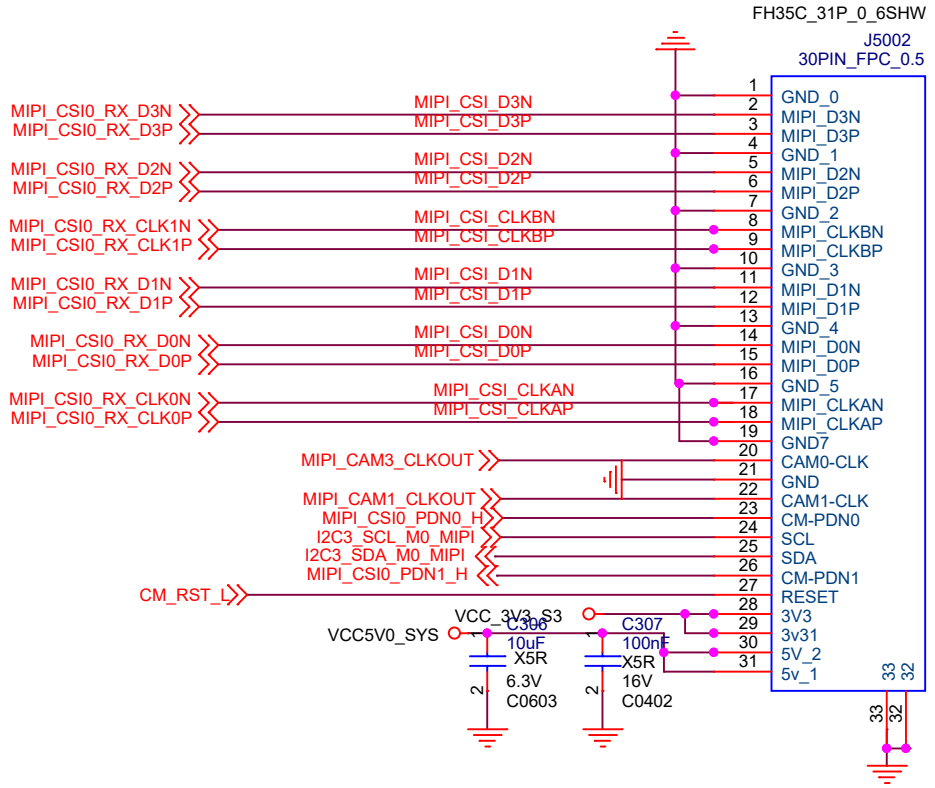
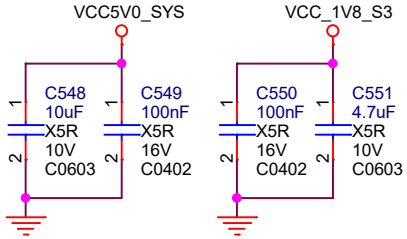
CAM



IMX334:
AVDD=2.8V-3.0V; I=97mA
DVDD=1.1V-1.3V;I=405mA
DOVDD=1.7V-1.9V;I=1mA

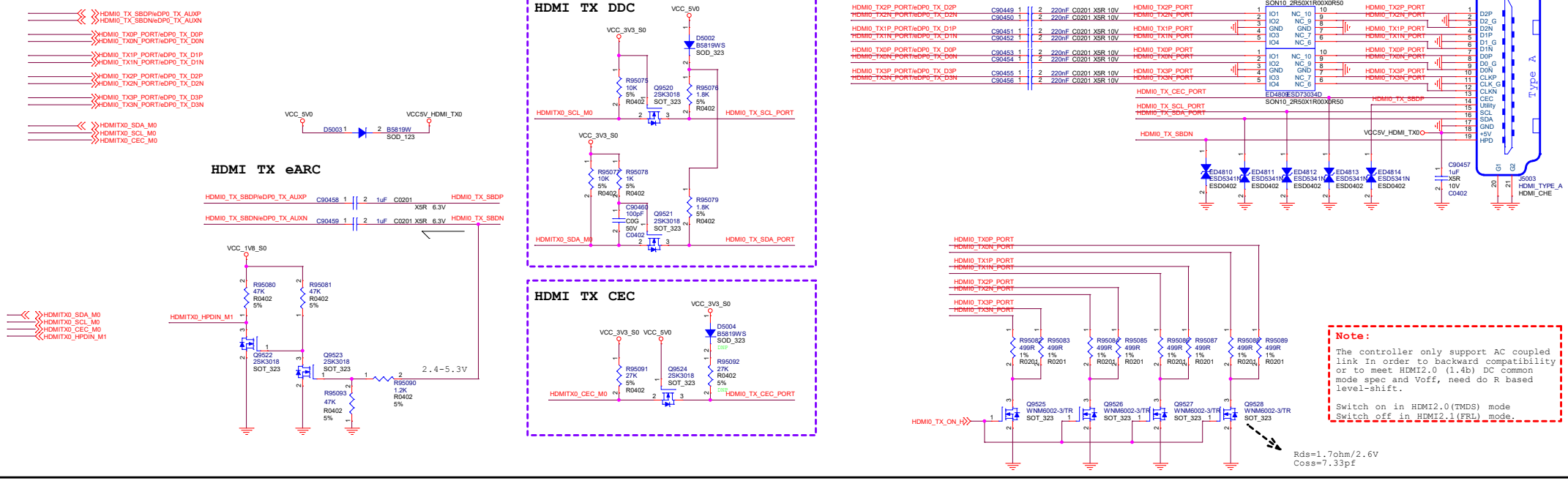
Note:
As below pin is for Array-MIC board

Pin39:I2C_SCL; Pin40:I2C_SDA;
Pin45:PWREN; Pin49:PDM_SDI0;
Pin50:PDM_SDI1; Pin51:PDM_CLK1;
Piin52:PDM_CLK0;Pin65:PDM1_SDI2;
Pin66:PDM1_SDI3

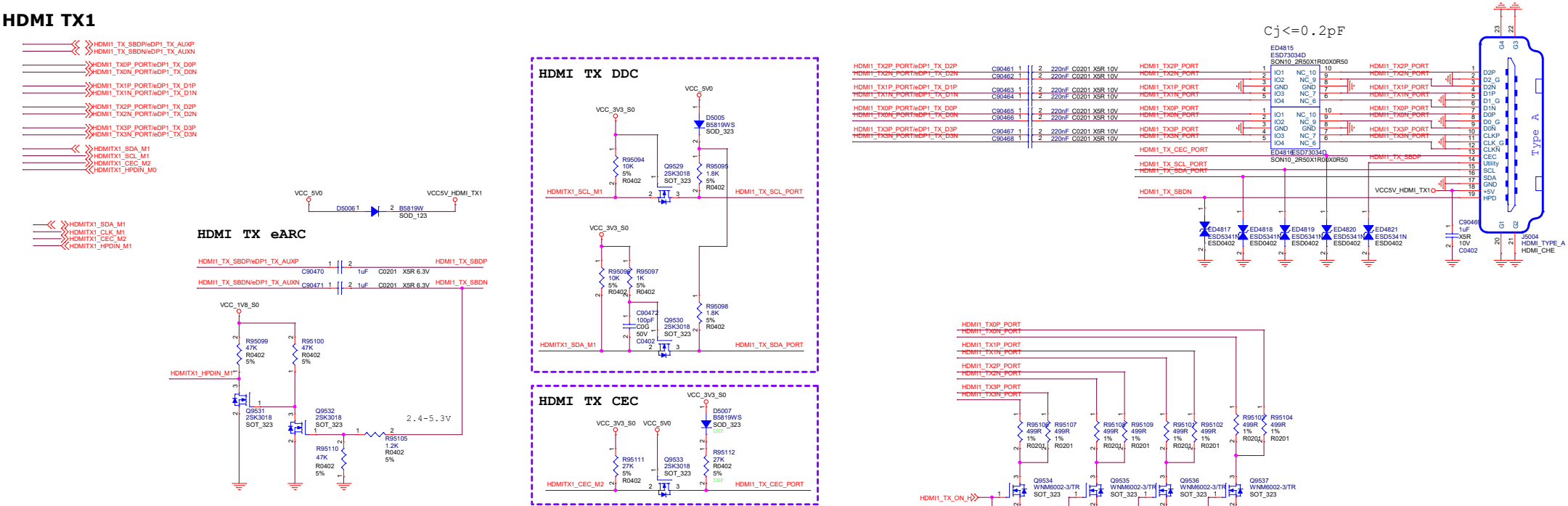


Size: A4	Title: ROCK 5B	REV: 1.1
	Page Name: 30.VI-Camera_MIPI-CSI	
Date: Wednesday, June 29, 2022	Sheet 30 of 33	

HDMI TX0

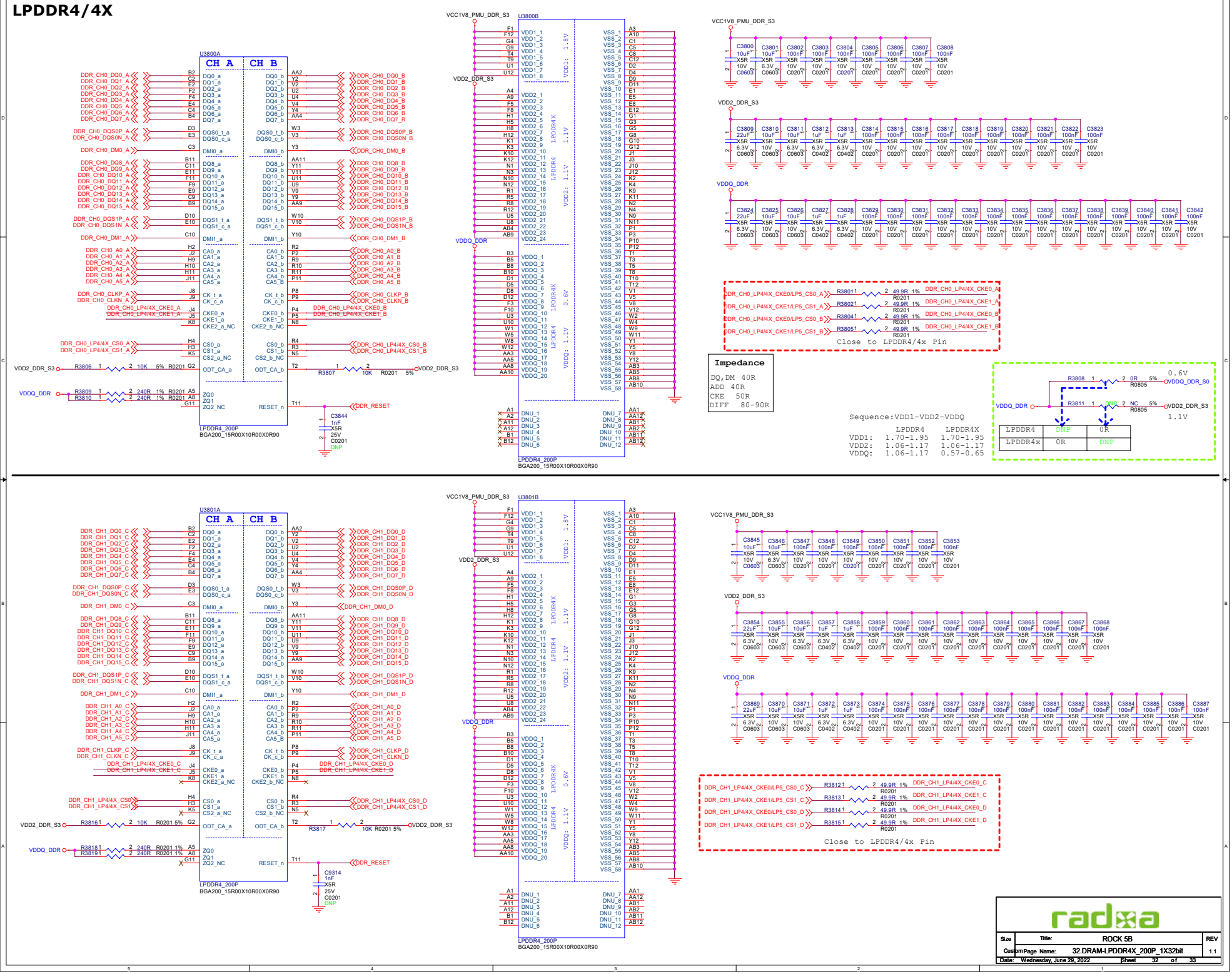


HDMI TX1



Size: A2	Title: ROCK 5B		REV: 1.1
	Page Name: 31.VO-HDMI2.1 TX		
Date: Wednesday, June 29, 2022	Sheet 31 of 33		

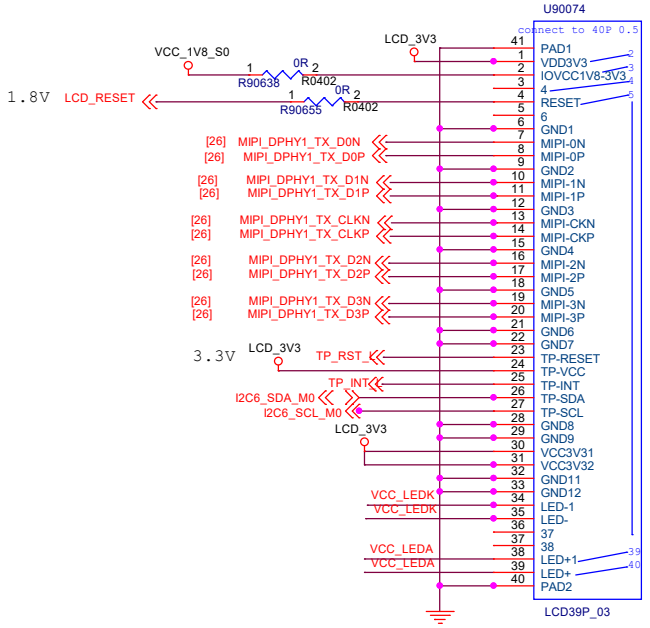
LPDDR4/4X

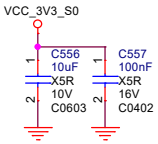


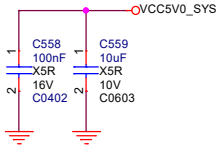
radxa

Size	Title:	ROCK 5B	REV
Custom	Page Name:	32.DRAM-LPDDR4X_200P_1X32bit	1.1
Date:	Wednesday, June 29, 2022	Sheet 32 of 33	

MIPI DPHY1 TX



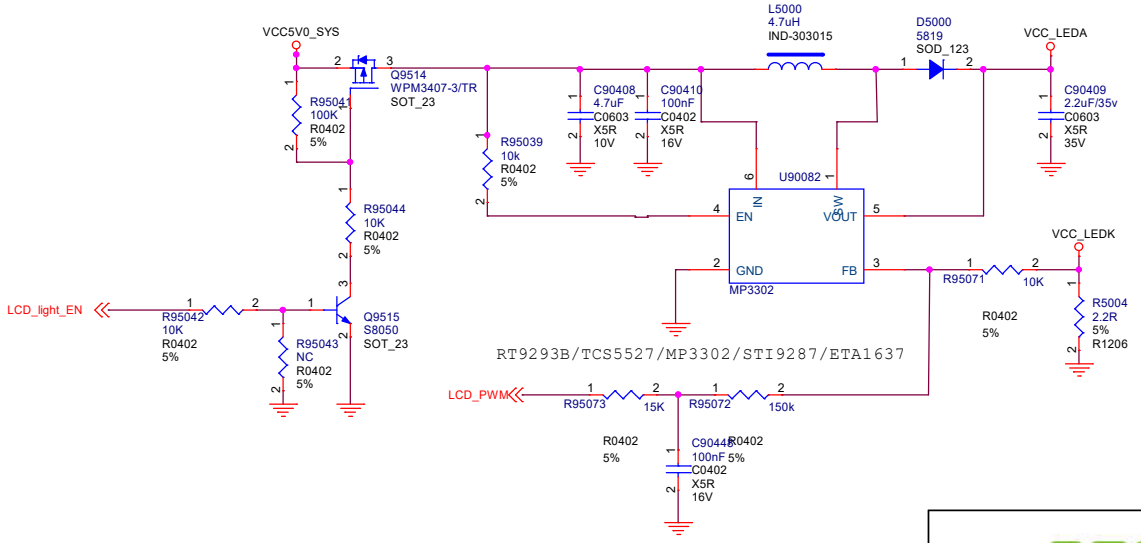




Note:
Mipi lcd and edp lcd can't be used at the same time.

LCD

RT9293B: L5000=22UH
MP3302 : L5000=4.7UH
ETZ1637: L5000=10UH R5004=NC



MIPI FPC Pin List

Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN
Pin9 :CLKP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL(3.3V)
Pin18:NO USE
Pin19:VCC_LCD(3.3V)
Pin20:LCD_RST 0.3V
Pin21:HW ID
Pin22:LCD_BL_EN(1.8V/3.3V)
Pin23:TP_I2C_SCL(3.3V)
Pin24:TP_I2C_SDA(3.3V)
Pin25:TP_INT(3.3V)
Pin26:TP_RST(3.3V)
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0

Size	Title: ROCK 5B	REV
A3	Page Name: 33.VO-LCM_MIPI	1.1
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